THE IBL READOUT SYSTEM

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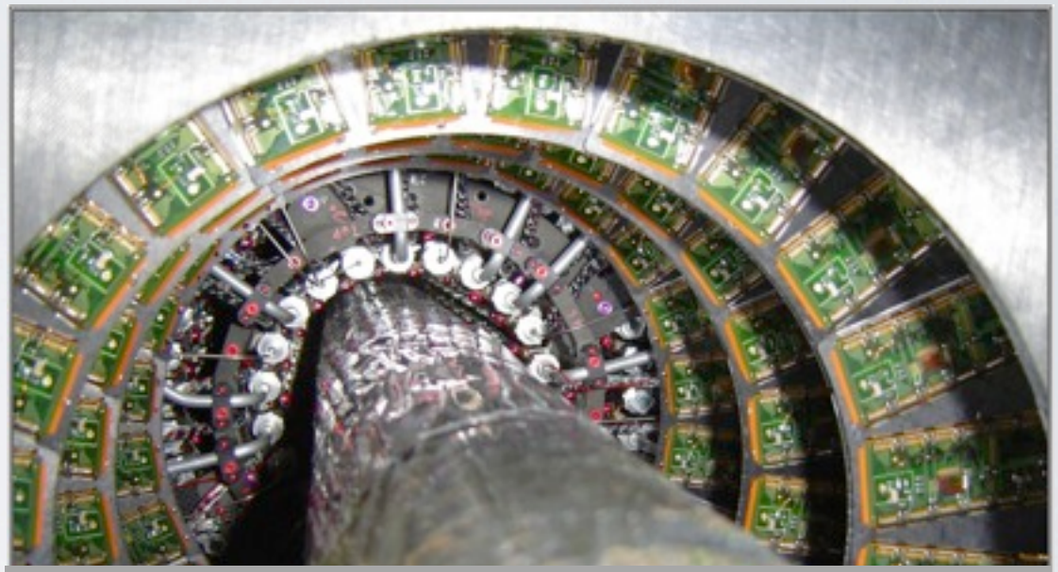
OUTLINE

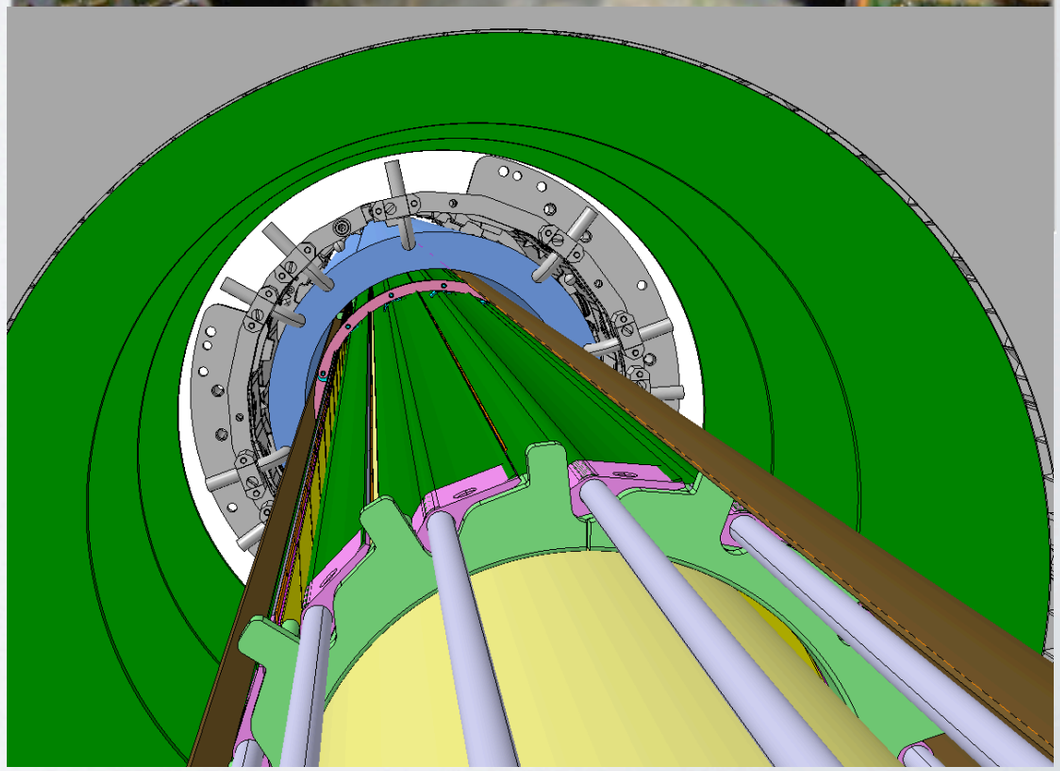
- IBL Introduction
- Towards the IBL readout system
  - Building Block Layout
- Summary

IBL INTRO

- In the frame of the ATLAS phase I upgrade, the pixel detector will start being inefficient, mostly due to large pileup/higher occupancy

- An Insertable B-Layer (IBL) is to deliver a fourth spacepoint, with higher z-resolution and better readout efficiencies, allowing to separate primary vertices, hence raising the total efficiency and increasing total resolution





IBL INTRO

- The IBL will be constructed in 14 Staves, carrying modules at a ~3.3cm radius
  - Due to the IBL being at smaller radius the occupancy will increase
- Each Module contains two frontends
  - Both are served with the same TTC supply, an addressing scheme helps configuring each frontend individually
  - Compression of hit pairs into a single hit word decreases bandwidth need
  - Each frontend is given an individual readout link

➡ All in all the IBL can be read out at 160 Mbit/s including balancing of data using an 8b/10b encoding scheme

READOUT SYSTEM FRAME

- The IBL is to be read out as part of the recent Pixel detector

  ➡ VME basis will stay, such that the general software infrastructure can stay untouched

- Pin compatibility will be served, but functional compatibility will be up to firmware and not given in a first version

- The bandwidth per building block will increase from 1.3 to ~5 Gb/s

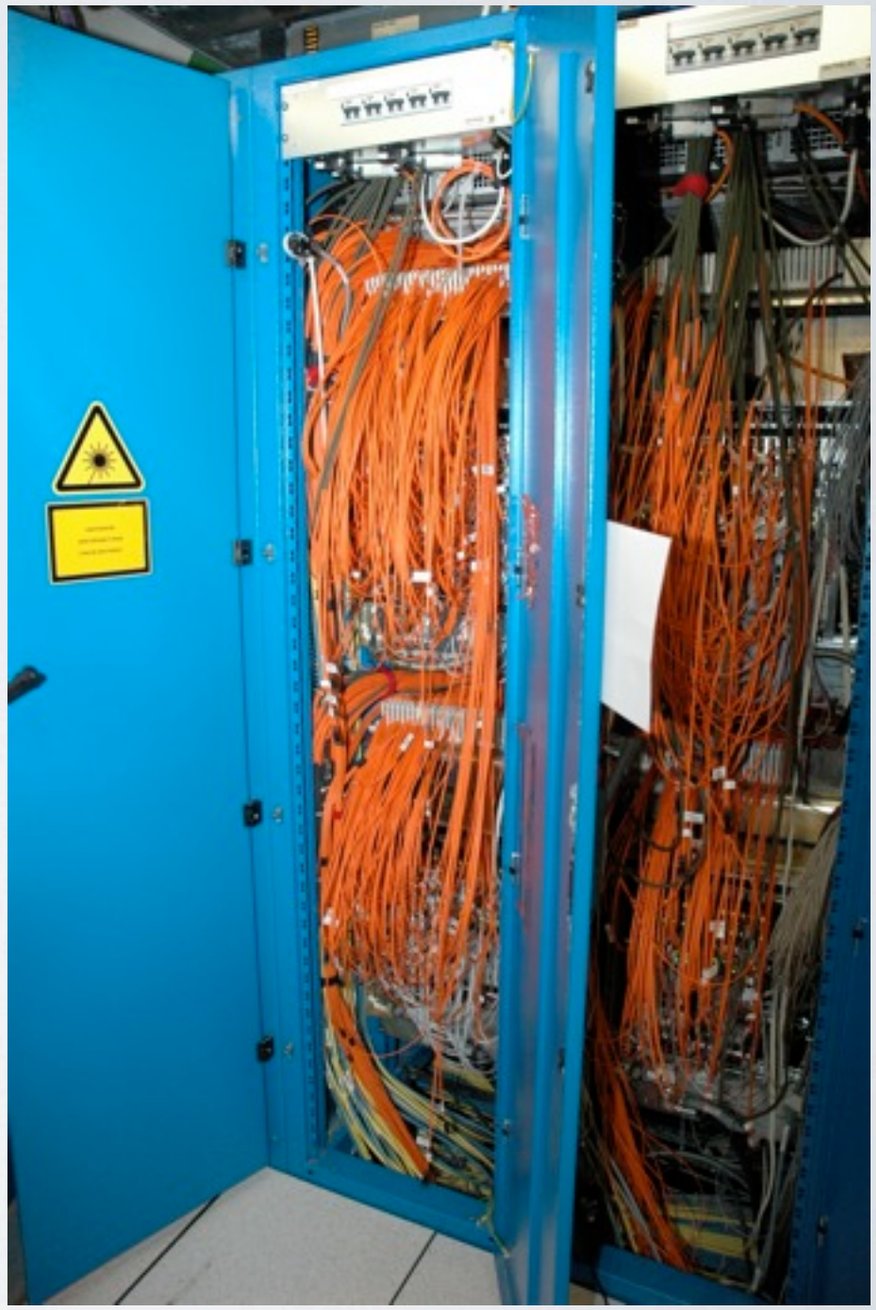
- General hardware infrastructure will stay: TTC crate, TTC Interface Module (TIM)

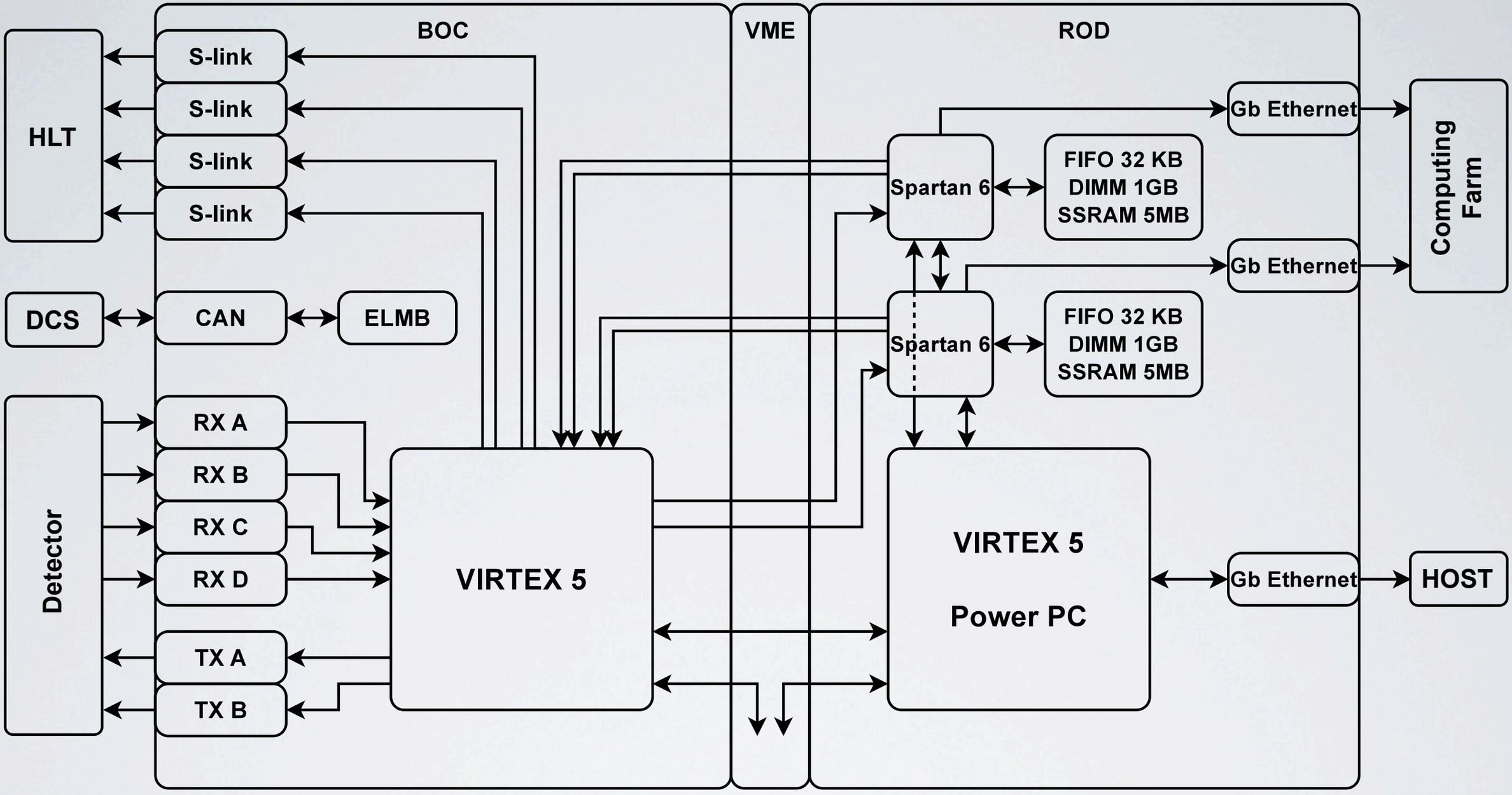
READOUT BUILDING BLOCK

- Crate Concept:
  - Smart Object on the frontside - VME bus connection, visible status indicators
  - I/O object on the backside - detector side I/O, as well as higher level trigger interface: "untouchables" →

➡ Pixel and IBL Building blocks are built from:

  - A readout driver (ROD)
  - A Back of Crate (BOC) card




BOC
VME
ROD
HLT
S-link
S-link
S-link
S-link
DCS
CAN
ELMB
Detector
RX A
RX B
RX C
RX D
TX A
TX B
VIRTEX 5
Spartan 6
FIFO 32 KB
DIMM 1GB
SSRAM 5MB
Spartan 6
FIFO 32 KB
DIMM 1GB
SSRAM 5MB
VIRTEX 5
Power PC
Gb Ethernet
Gb Ethernet
Gb Ethernet
HOST
Computing
Farm

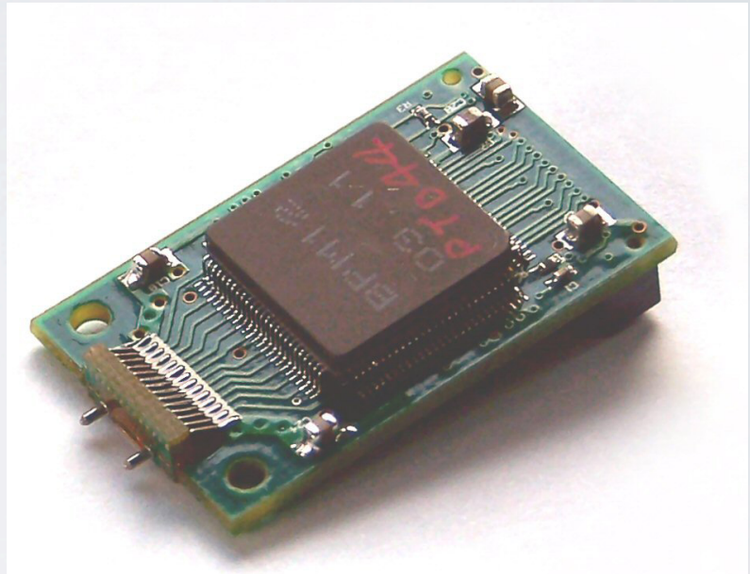
BACK & FRONT

BACK OF CRATE CARD

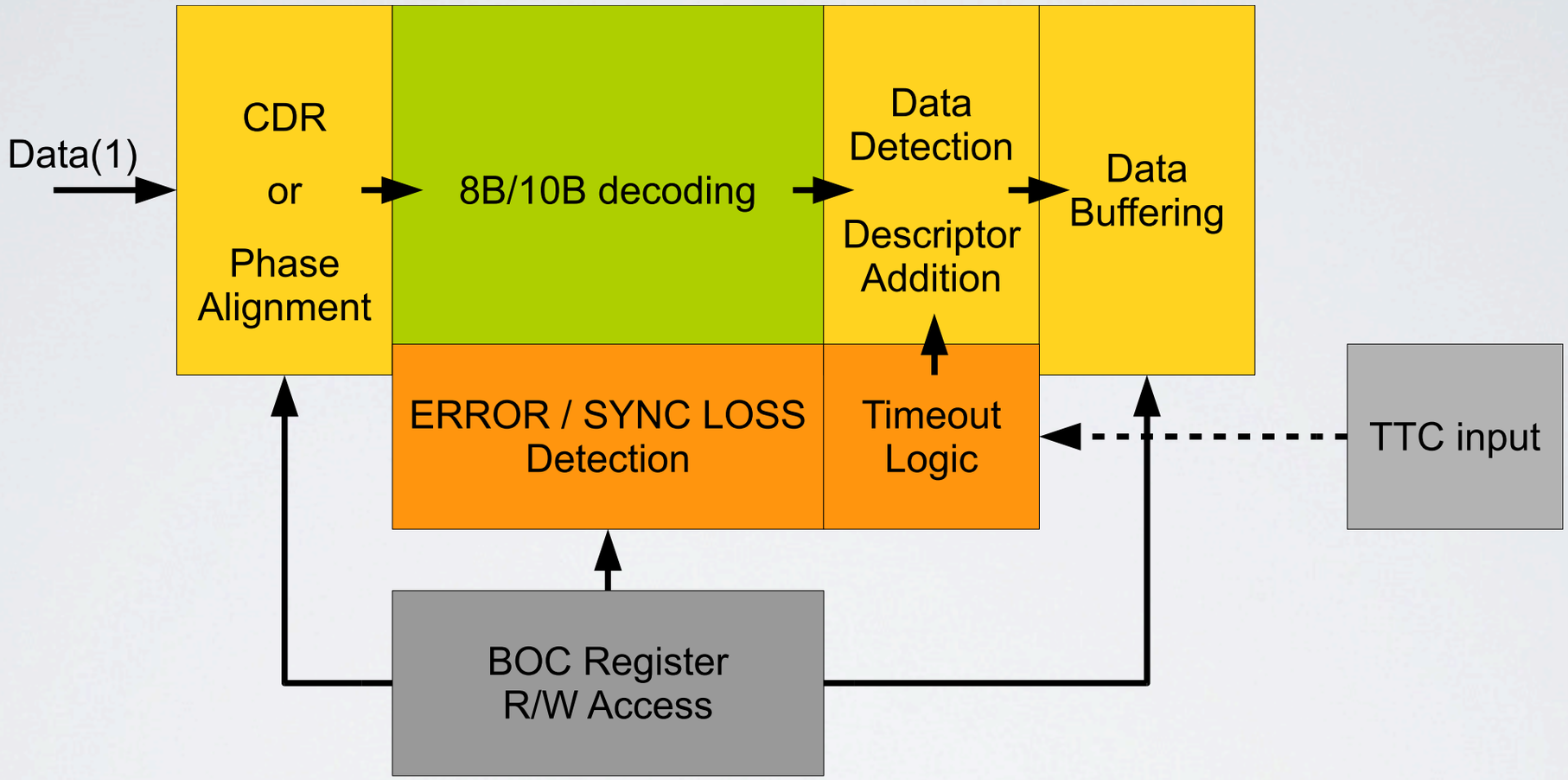
- Optical Interfaces towards the detector:
  - TTC: 40 Mbit/s BiPhase Mark encoded - 1 link for two FEs combined CLK & Data
  - Data: 160 Mbit/s 8B10B encoded - 1 link per FE
- Interfaces towards HLT - S-Link (160 MB/s)
- Timing:
  - Adjustment of TTC phases in sub-ns steps, to allow for detector timing adjustment with respect to the LHC bunch crossing
  - Automatic sampling of the returned data and synchronisation with the off-detector clock

BOC - SOFT CODEC FRONTEND

- Former Plugins have serious lifetime issues
- An optical component including laser and driver can be bought off-the shelve
  - ➡ Reliability known and exchange in case of failure possible
- Codec (BPM) and Timing functions have been embedded into FPGA firmware and deliver a working replacement



BOC - DATA RECEIVER



- The IBL BOC will serve a receiver that:
  - Synchronises, deserializes and eventually decodes data
  - Flags errors and fills in timeout data
  - Buffers output data for processing by the ROD

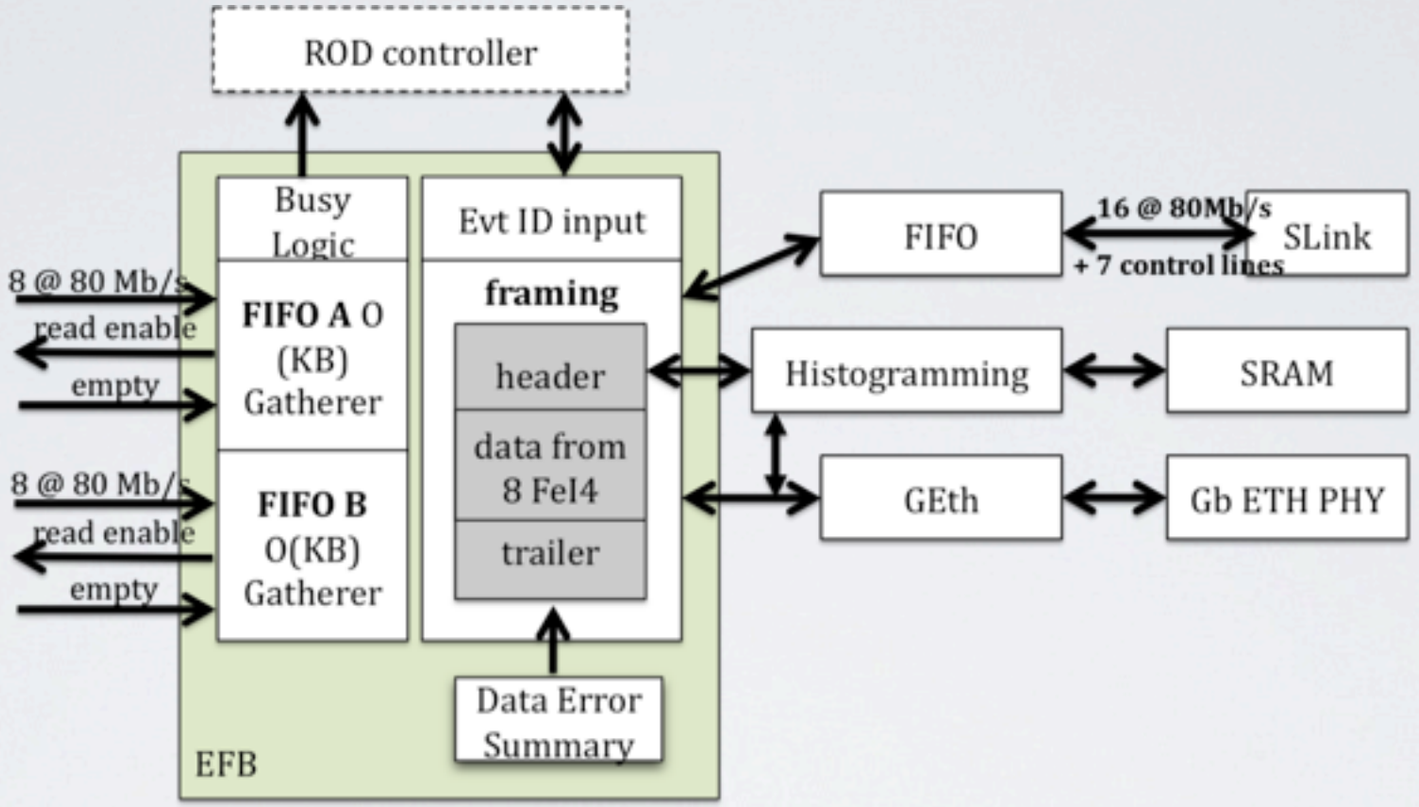
BOC - EMBEDDED S-LINK

- The HLT Interface will advance from a previous HOLA mezzanine to an FPGA embedded S-Link solution delivering:
  - Higher data density per board space
    - ★4 x HOLA delivering the total bandwidth would occupy the full board
  - Firmware based upgrade ability (up to 3.75 Gb/s & link)
  - FTK readiness (copied S-Link output including backpressure)

READOUT DRIVER

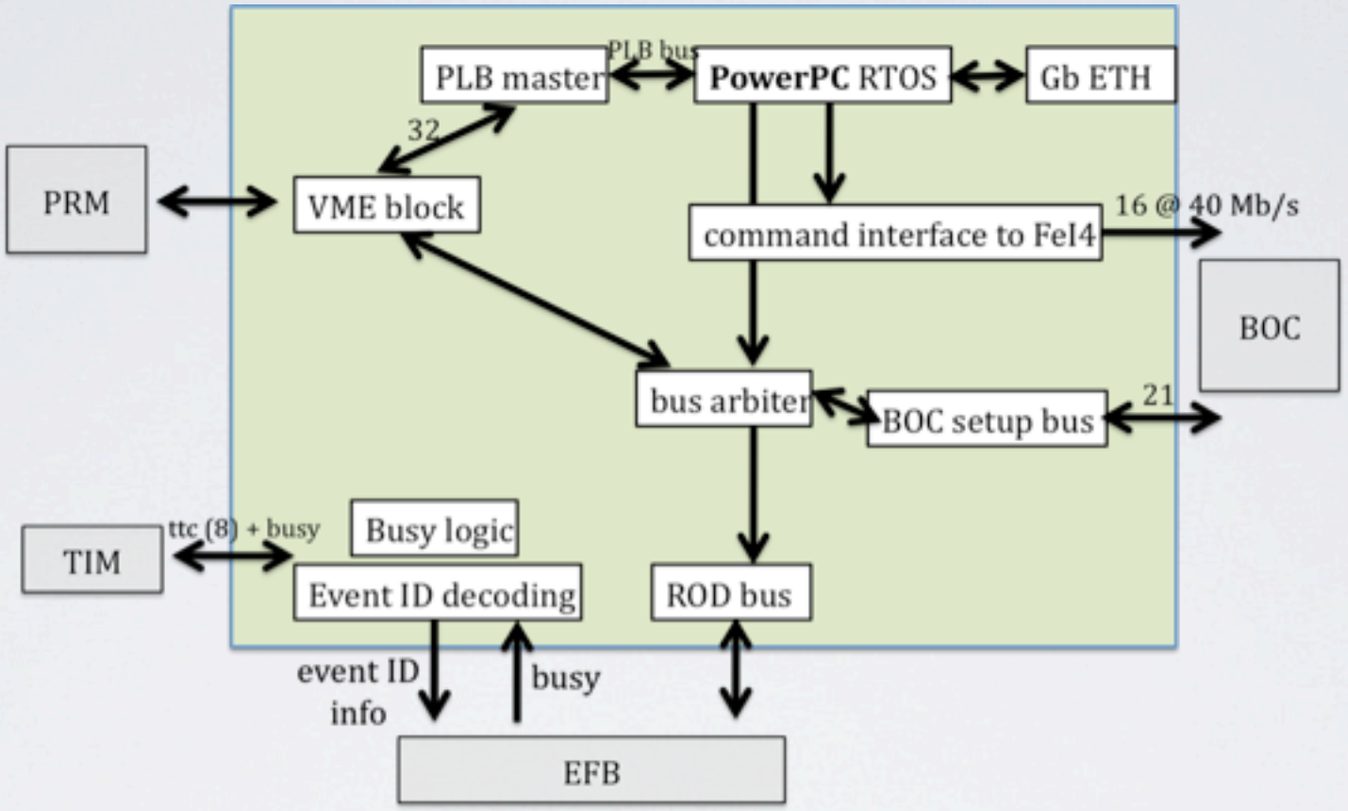
- Command and Configuration Interface
- Event framing of data from multiple receivers on the BOC
- Calibration:
  - Automated control of calibration scans
  - Data histogramming
- Host control interfaces:
  - via VME for compatibility
  - via GEth for Speed...

ROD LOGIC BLOCKS: EFB



- Event Fragment Builder (EFB)
  - Gathering data from two 4-way receiver blocks
  - Summarizing errors within the event fragment
- Output to a local histogramming engine for calibration, an S-Link for data taking or the a GEth port for debugging

ROD LOGIC BLOCKS: RCF



- ROD Controller FPGA (RCF)
  - Delivers host interface for control/configuration of ROD and BOC
  - Reads data from TTC Interface Module, receiving triggers and event IDs
- Internal PowerPC enables to run iterative code executing scans locally without host interaction/control

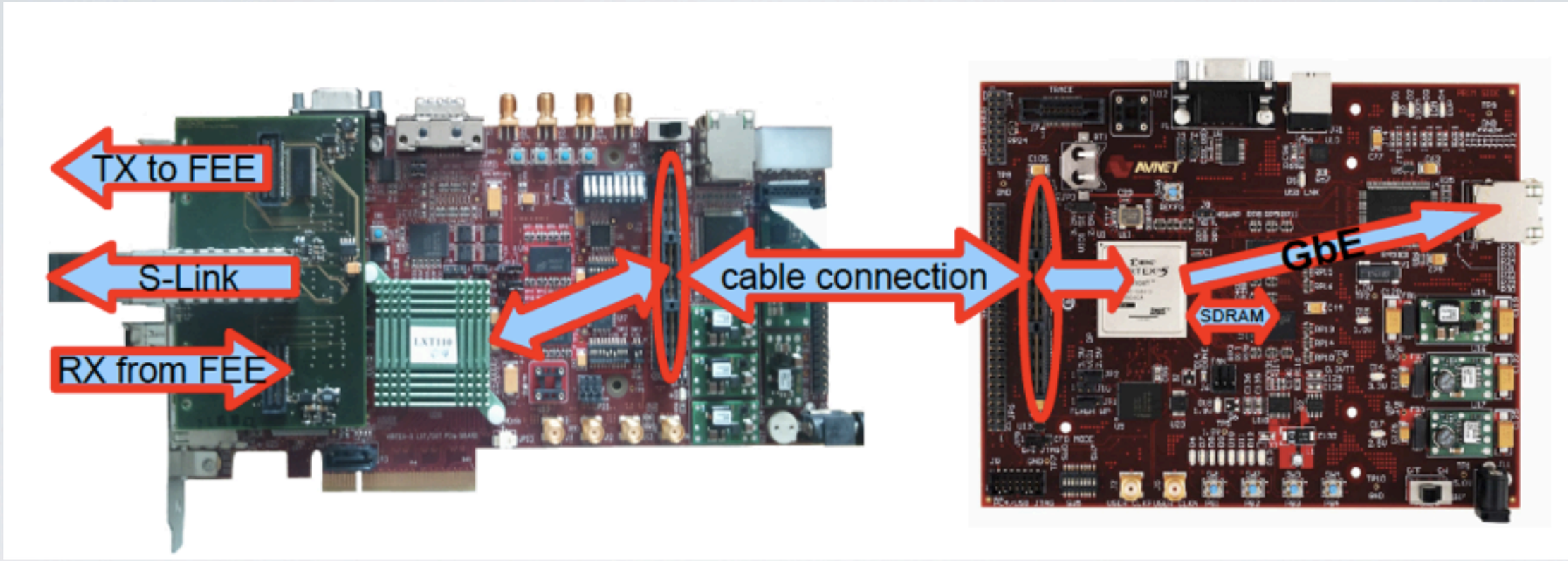
HISTOGRAMMING

The new ROD is to feature an embedded histogramming unit:

- Will run at full readout speed, main limitation is memory
- Delivers histograms for Occupancy, Time Over Threshold and Time Over Threshold^2
- All processing of histograms is outsourced to a PC farm, delivering an easier programming environment than embedded processors

➡Calibration speed won't be limited by IBL

TESTBED



- Using evaluation boards existing in both development fields (ROD and BOC), it is planned to set up a testbed within this year
- Firmware blocks are partly ready to be used and will serve for an initial setup - e.g. error flags will move in later...

SUMMARY

- The readout system for the ATLAS IBL is under development
- Self-Adjusting data path within IBL, based on balanced signal transmission
- Industrial components will replace the custom-made components, recently failing within ATLAS pixel and SCT
- Embedded histogramming and an external processing will replace full, but slow, internal processing of the ATLAS pixel system
  - New histogram readout path via GEth will increase the calibration speed
- Total bandwidth of building blocks increases, leading to smaller size systems (IBL readout fits in a single crate)
- A first testbed is waiting for a firmware set to be tested

ADDITIONAL INFORMATION @ THE POSTER SESSION

POSTER # 50:

ATLAS IBL: INTEGRATION OF NEW HW/SW READOUT FEATURES FOR THE ADDITIONAL LAYER OF PIXELS