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Charge Sensitive Amplifier (CSA) in cold gas of Liquid Argon (LAr) Time Projection Chamber (TPC)

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The common channel of this 8-channel chip is made of a Low noise Charge Sensitive Amplifier (CSA) with respectively 250fF and 4MΩ feedback capacitance and resistance. The CSA is followed by a bandpass filter centred at 1µs and a buffer line driver. An 'i2c-like'protocol serial link allows slow control of registers, giving multiple configuration features to the circuit. The input referred noise of 1500 e- rms had been measured at -100℃ with an input detector capacitance of 250pC. Thanks to those performances, the minimal signal of 18000e- (2.88fC) will be correctly measured.

Summary

This development was performed for a Liquid Argon TPC detector proposed for the T2K experiment (Tokaï to Kamiokande). The physics requirements for cold readout of LAr TPC detectors imply that the circuit should be able to measure an input charge of about 3fC distributed over 500ns with as low noise as possible; with the least power consumption possible; and the circuit should work at a temperature around -120℃. Rather than costly characterising the chosen technology (Austria-Microsystems C35B4) for cryogenic temperature, we checked successive test-chips performances and stability in liquid nitrogen. Stability is an important issue when the models are not fully fitted to the temperature fluctuations.

For such reasons, this paper will summarize the three previous versions chips. The advantages and the drawbacks will be enlightened. Low noise Charge Sensitive Amplifier (CSA) is essential to measure the amount of electron generated into a Neutrino detector. The main constraint of this detector for the front end electronic is the capacitance of the wires that brings the signal. The CSA has to integrate 500ns signal of 18000 electrons, considering an input capacitance of 250pF. The input referred noise has to be as low as 1500 electrons in order to satisfy a signal to noise ratio higher than 10. In order to minimize the capture of electrons by the input capacitance, the DC gain of the amplifier (A0) needs to verify the equation Cdet « A0.Cpa, which means A0 » 250pF/250fF. Since the CSA architecture that will be detailed in this paper is very sensitive also to the power supply noise, the conversion gain has to be as high as possible. We set a conversion gain of 15mV/fC. Obviously, increasing too much the conversion gain will minimize the dynamic range by limiting the output to the power supply bounds. However in our case the first limitation encountered was due to the parasitic capacitance of the integrated huge feedback resistance Rpa=4MΩ that were significant comparing to the feedback capacitance Cpa=250fF. The actual conversion gain is made in two steps, with the minimum acceptable value for Cpa, and a gain of 4 in the CR-RC shaper.

It is very cumbersome to debug a solid state ASIC, when the expected behaviour is not meet, since modifications are not possible anymore. To prevent such uncomfortable situation, we added additional configuration signals. Since the number of pins is limited, we chose to hard wire those signals to registers. The configurations registers are adjustable thanks to the digital 'i2c-like'block that requires an area of 100µ x 550µ and only 3 pins: a clock, a data and a reset. This slow control bloc was successfully tested in liquid nitrogen. This 'i2c-like'block could operate up to 40MHz, despite in our case, there is no speed requirement.

Experimental results in terms of cross-talk, noise as a function of Cdet and stability will be detailed and explained in this paper. Further designs are carried out to reduce the consumption but in the overall, our goals had been fulfilled.

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