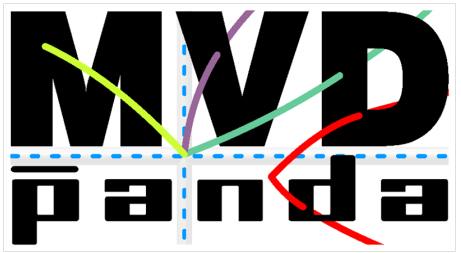
The silicon pixel readout architecture for the Micro Vertex Detector of the Panda experiment.

D. Calvo, P. De Remigis, T. Kugathasan,
G. Mazza, M. Mignone, A. Rivetti, R. Wheadon

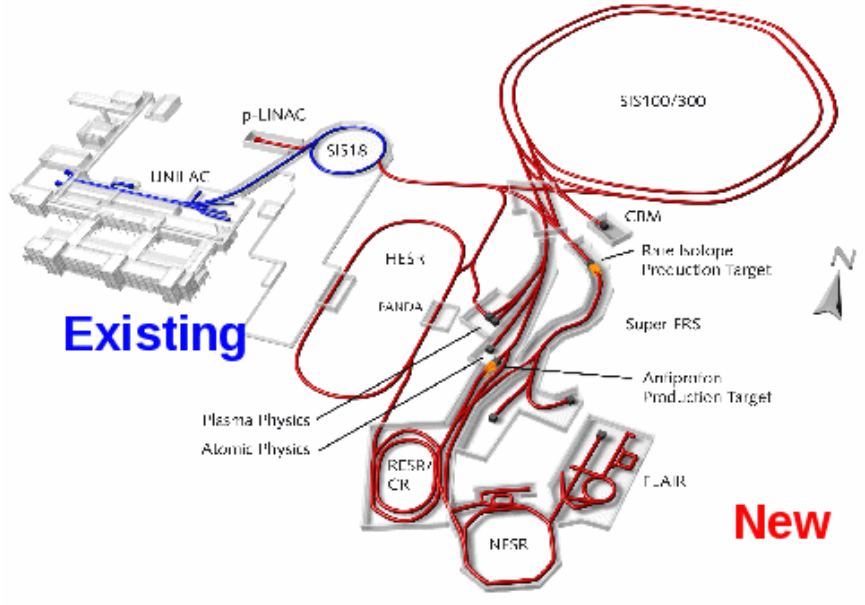
INFN Torino

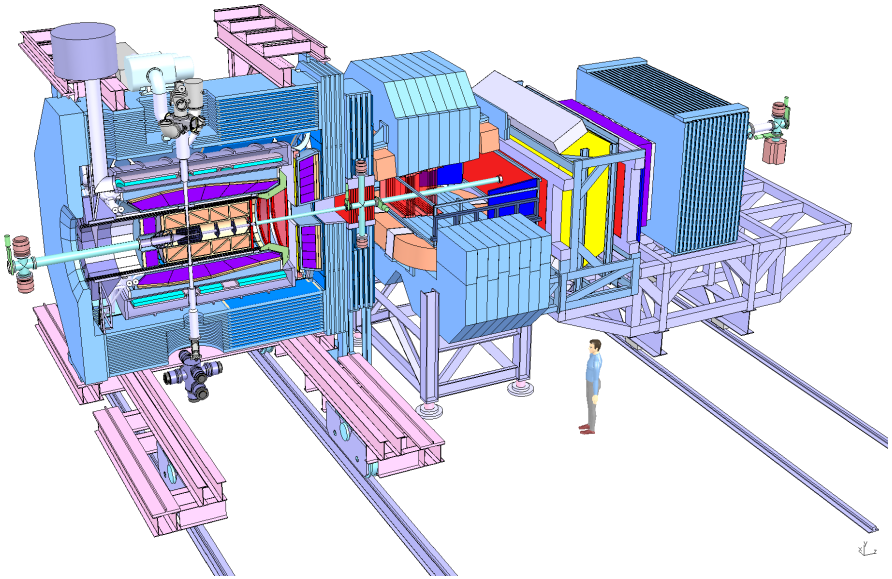


Twepp, Aachen

RWTH, 2010

The Fair laboratory and Panda experiment.

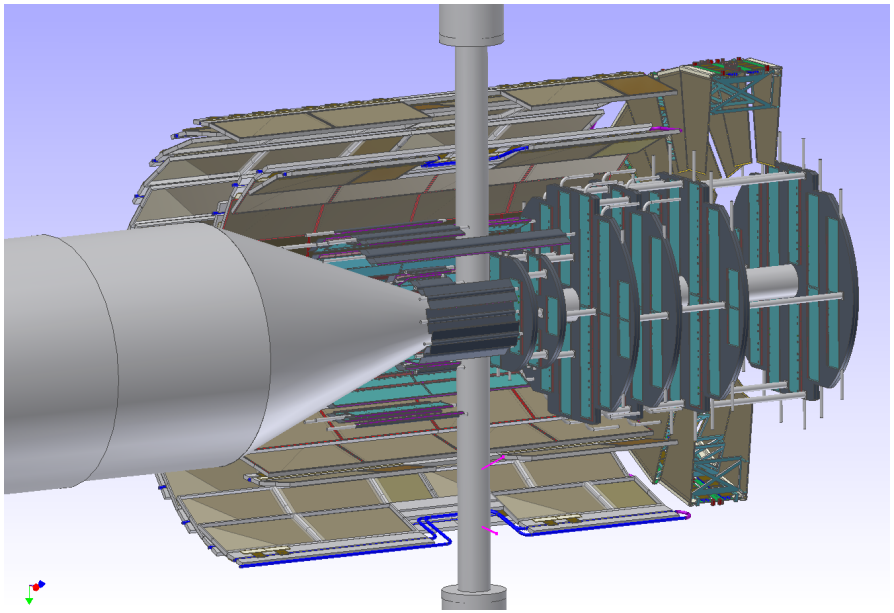




annihilation rate: $2 \cdot 10^{7} s^{-1}$ @ 15GeV/c

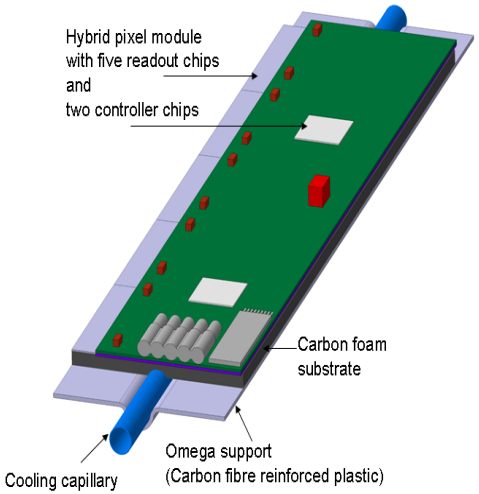
FAIR (Facility for Antiproton and Ion Research) is an international laboratory and it is an extension of the GSI facility. The antiProton ANnihilation at DArmstadt (Panda) is a fixed target experiment and it is composed by two sections: the target and the forward spectrometer.

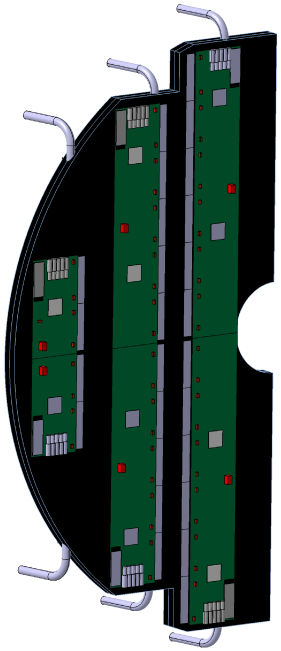
The Micro Vertex Detector (MVD).



The MVD consist of 4 barrels in the central part (two layers of pixels, then two layers of strips) and 6 disks along the forward direction (4 layers of pixels, then two layer mixed). Summarizing there are roughly 11M pixel cells and 200K strip readout channels.

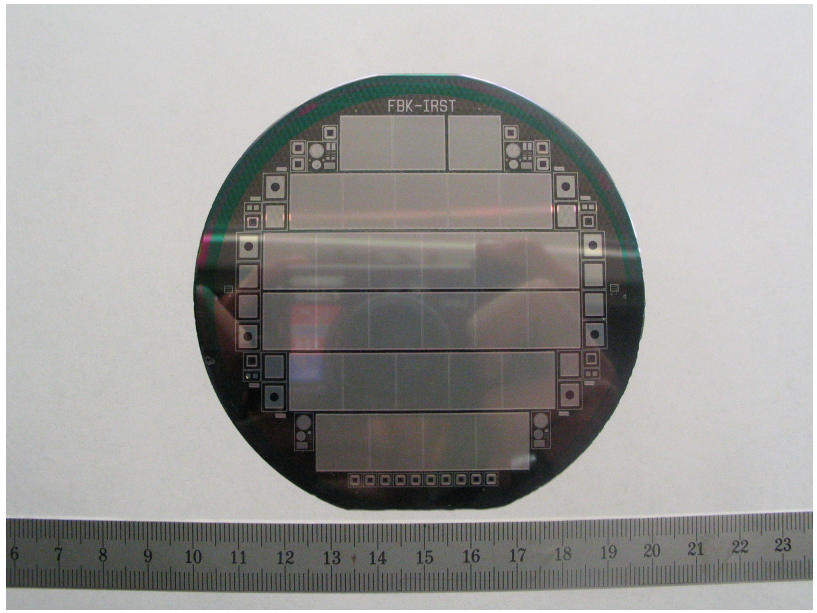
The concept for the hybrid pixel module.

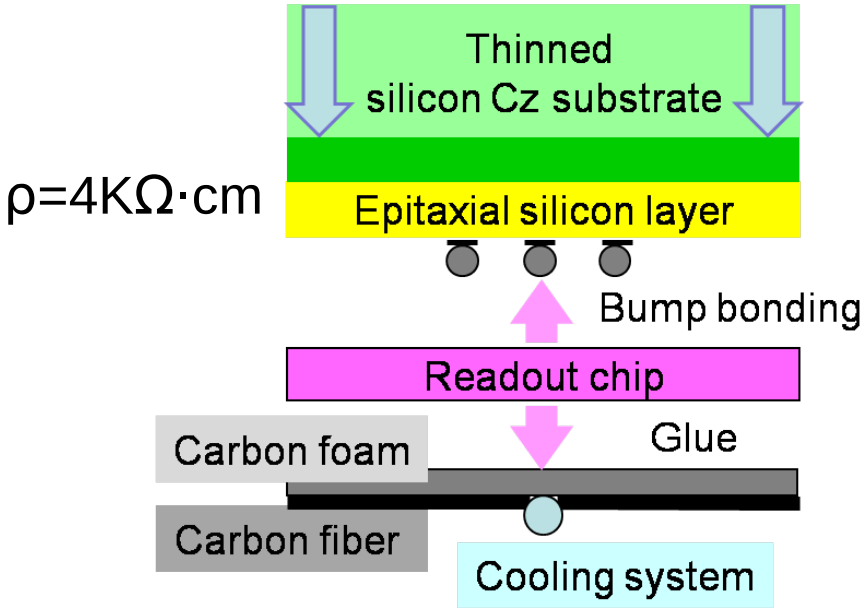




The sensor is bump bonded over the readout chips, and the multilayer bus is added on the top. Then this structure is glued on a carbon foam to improve the thermal conductivity, and on the bottom there is the cooling pipe for the heat extraction.

The hybrid pixel sensor.





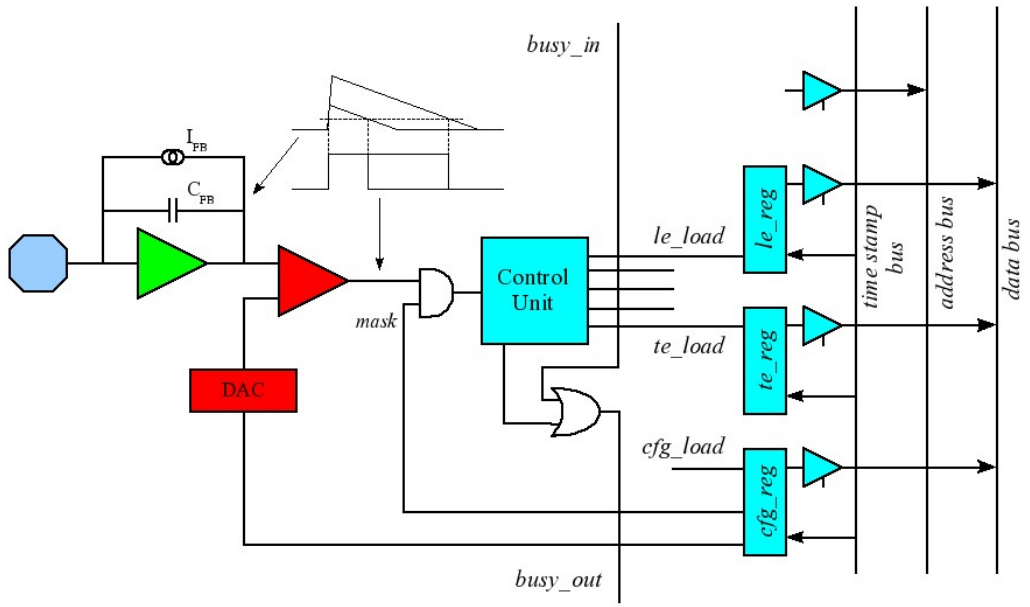
Each pixel is 100·100μm^2 large, and is implemented on an epitaxial layer deposited on a Czochralski substrate; it is connected to the readout chip by a standard bump bonding process. Some tests have been performed, with the overall thickness in the range 150 to 100μm.

Specifications for the Topix readout chip.

pixel size	$100 \cdot 100 \mu m^2$
active area	$11.4 \cdot 11.6 mm^2$ (110·116 cells)
dE/dx measurement	TOT (12b range)
input charge	1÷50fC
noise floor	.032fC ($200e^-$)
system clock	156MHz
time resolution	6.41ns (1.85ns rms)
power consumption	$500 mW/cm^2$
event rate	$6.1 \cdot 10^6 hit/(s \cdot cm^2)$
total dose	100KGy

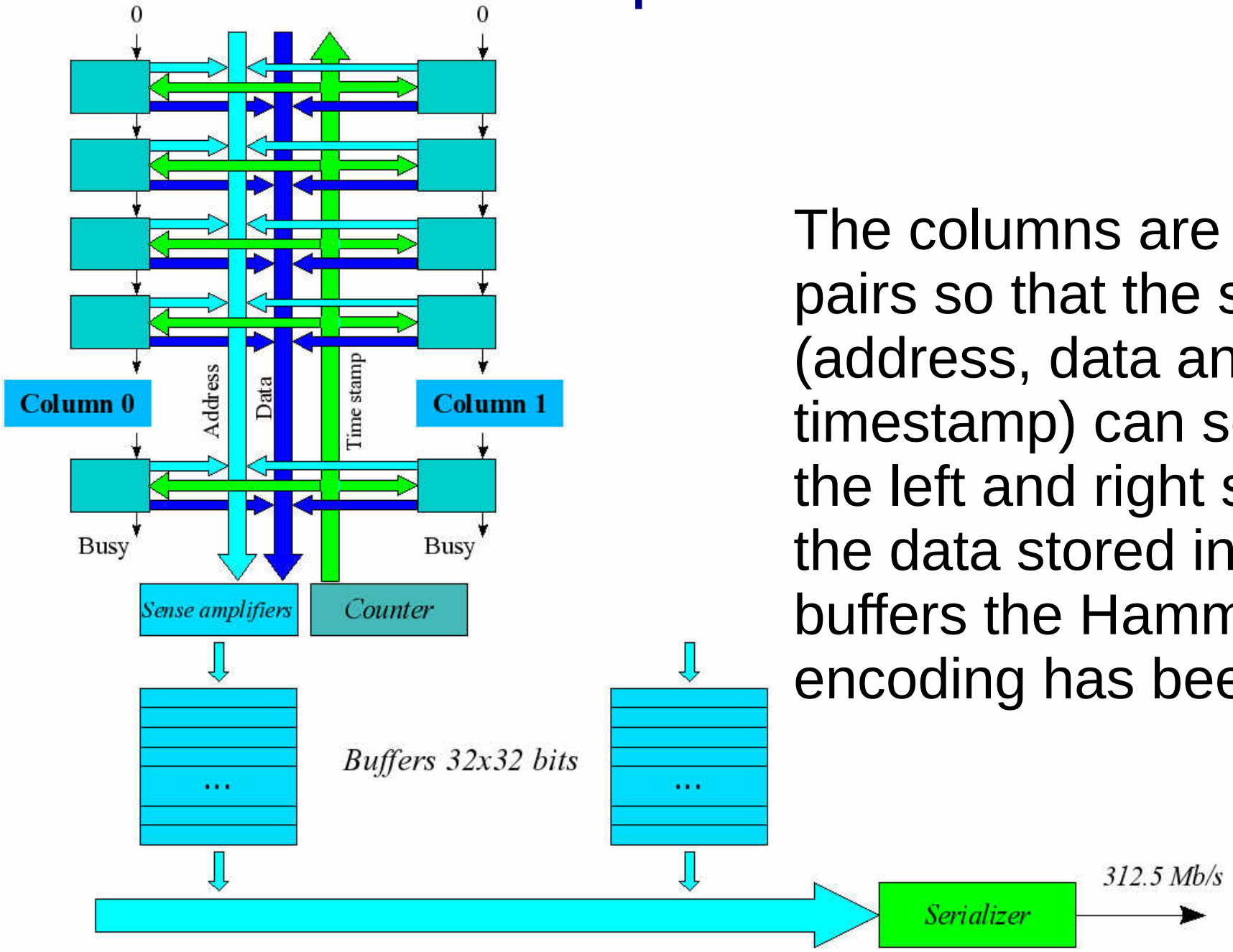
Since the system is triggerless, considering the constraints and a 50b word per event due to the 8b/10b encoding, then a 400Mb/s data rate per chip is expected as peak value.

The Topix cell structure.



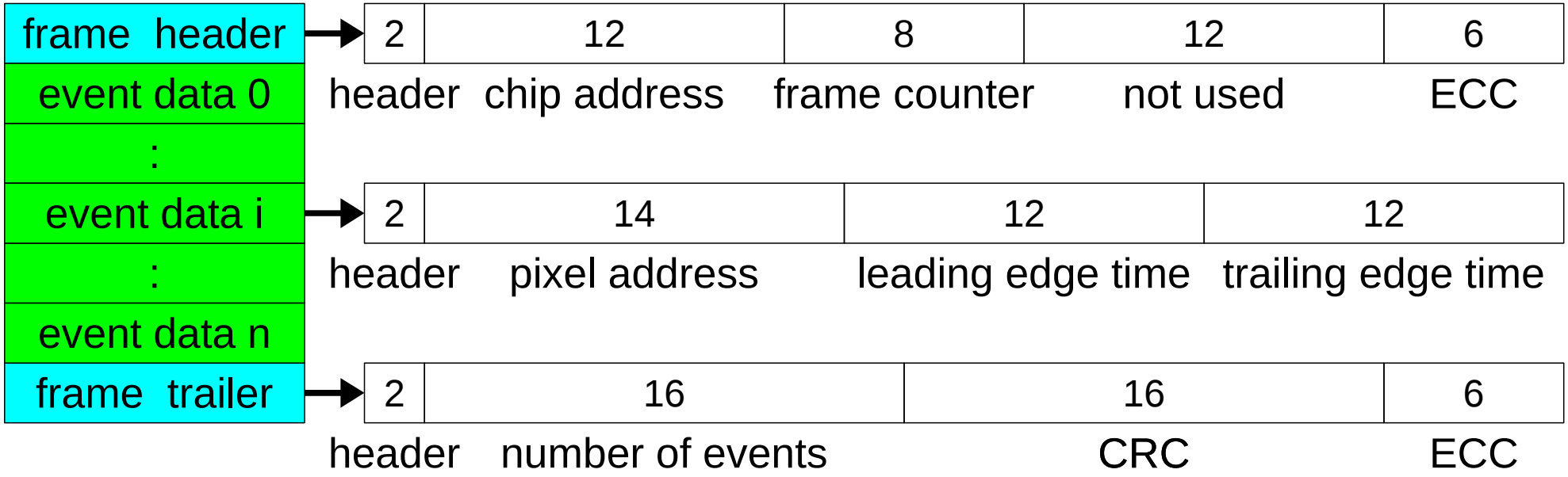
In each pixel cell there is a charge amplifier producing an output with a triangular shape, that is discriminated by a comparator indicating the leading and trailing time. This information is stored in the respective registers, latching the timestamps distributed to the chip.

The Topix architecture.



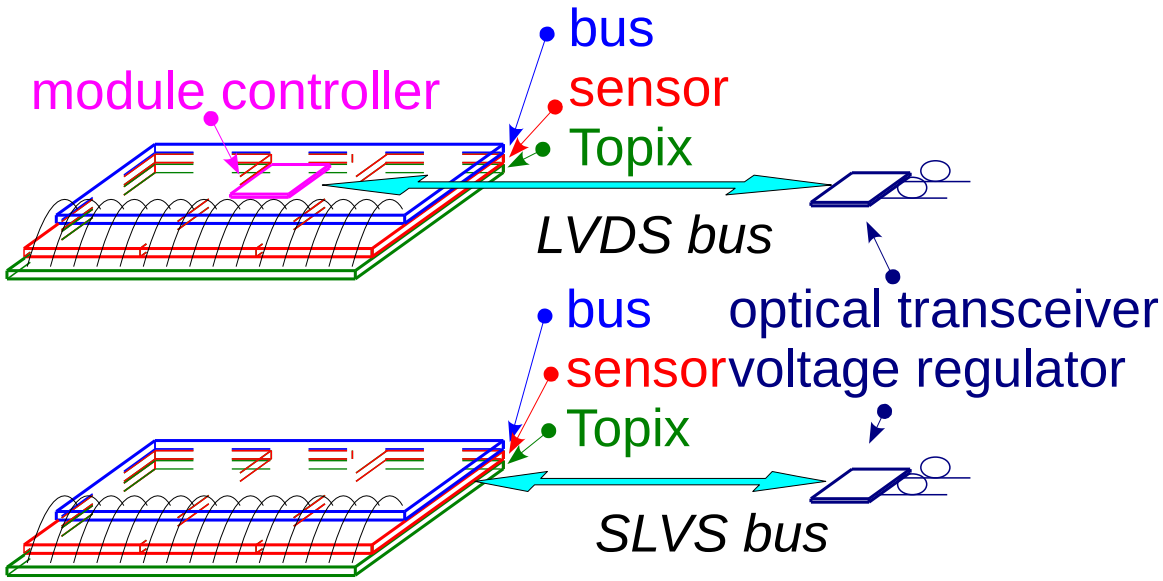
The columns are arranged in pairs so that the same bus (address, data and timestamp) can serve both the left and right sides. For the data stored in the FIFO buffers the Hamming encoding has been used.

Topix data format.



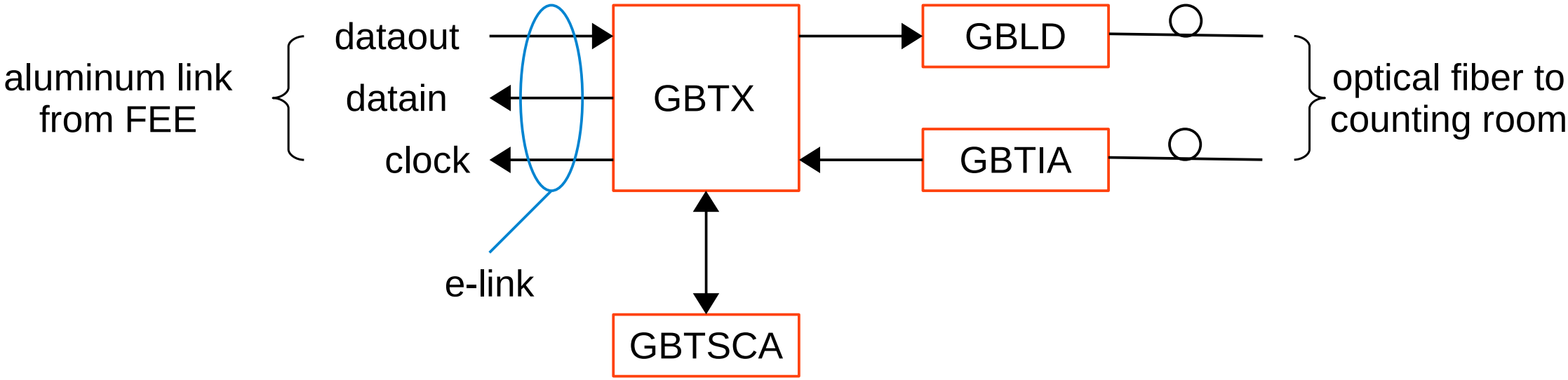
Each event is organized in a frame (with a header and a trailer protected by the ECC) collecting the data coming from every hit pixel (with leading and trailing edge times). A CRC, relative to the whole frame, is available in the trailer word.

Module alternatives.



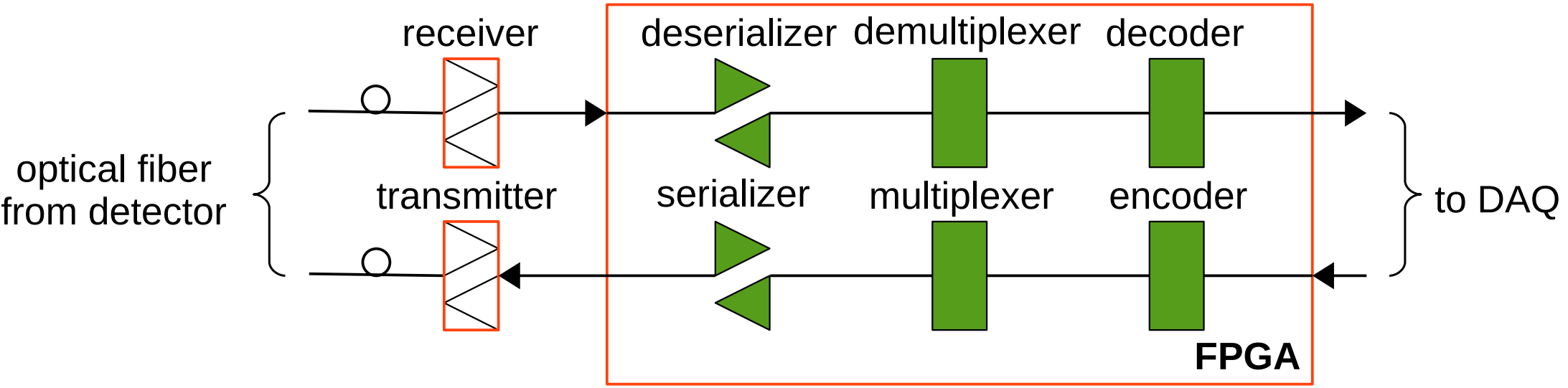
The design is progressing towards the last option because it does not require an extra chip, even though it could ask more electrical links. At present, a solution for the serial port needed for Topix could come from a Cern development.

The GBT interface towards the FEE.



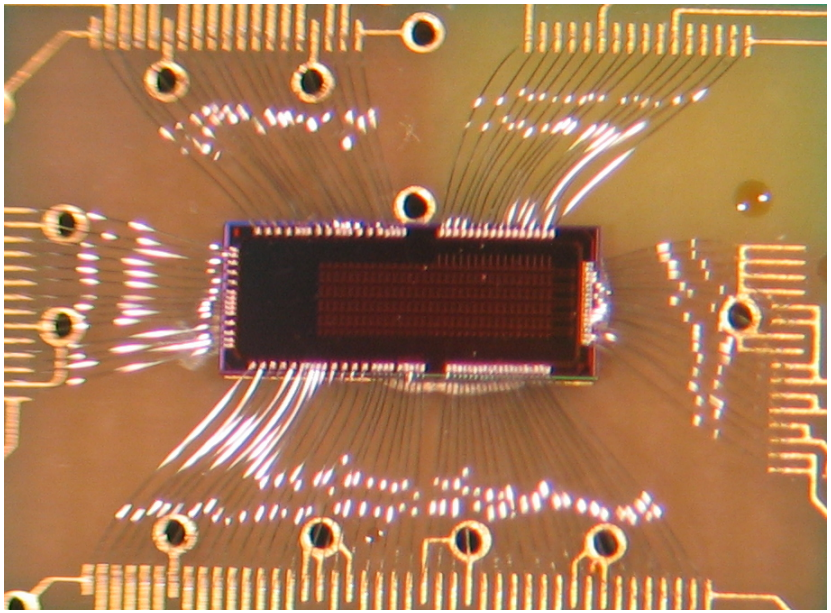
The GBT is the radiation hard chipset designed at Cern to provide an optical link for the next generation experiment and it consists of: a data transceiver (GBTX), a laser driver (GBLD), a transimpedance receiver (GBTIA) and a slow control (GBTSCA).

The GBT interface towards the DAQ.



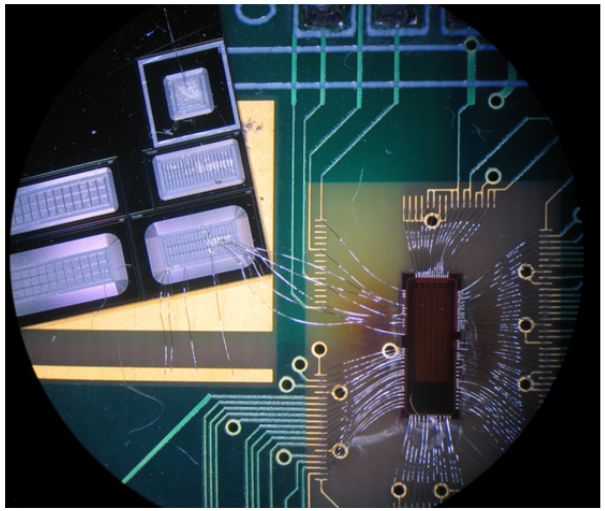
In this case the radiation hardness is not needed and, after the optical transceivers, the logic can be arranged in a FPGA taking advantage of the embedded serial transceivers; this interface is under study by the Jülich group.

Topix prototype in reduced scale.

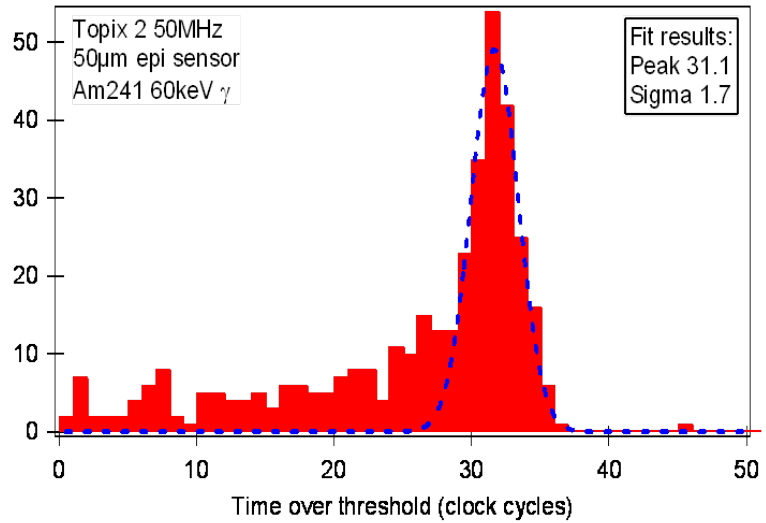


It has been produced in a Cmos 130nm technology, and it features 320 pixels arranged in 4 columns with various lengths. Each cell ($100 \cdot 100 \mu m^2$) presents the full analog and digital functionality, while there is a simplified end of column logic.

Topix test.



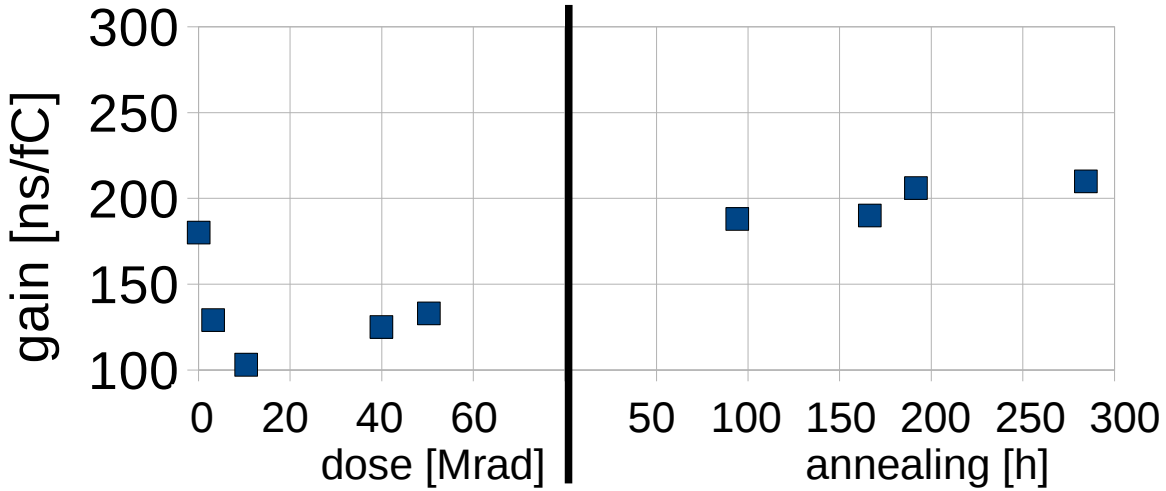
ToPix + epitaxial sensor



TOT calibration

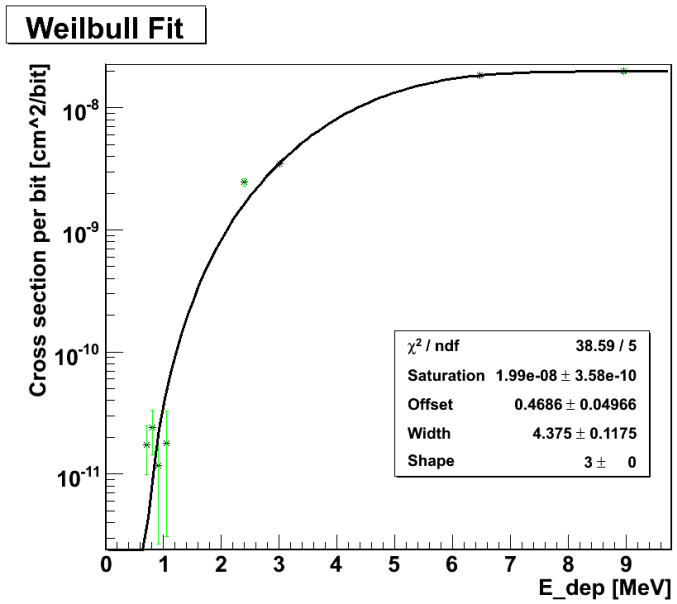
The Topix chip test has been performed with good results: the TOT gain is around 160ns/fC, there is a good linearity over the input range, the threshold dispersion has to improve but it can be compensated by the DAC present in each cell.

Test for Total Ionizing Dose.



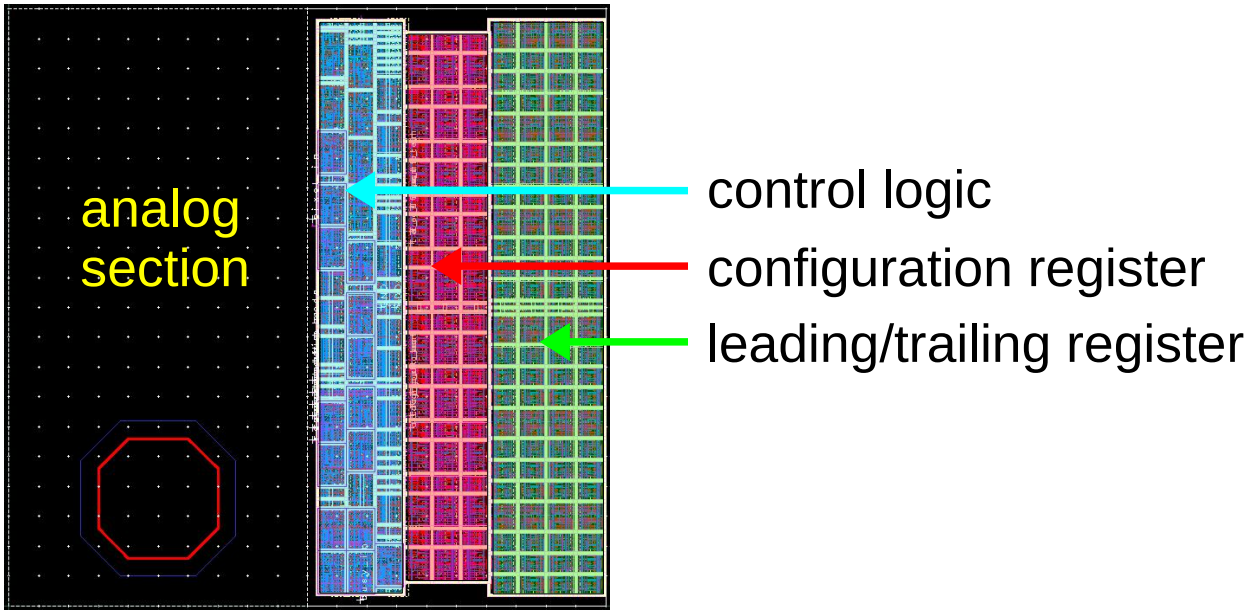
From the test for TID a variation of roughly 40% in TOT gain has been pointed out; for this reason the relevant transistors will be redesigned with an enclosed structure. The changes for the other parameters are below the 10%.

Test for Single Event Upset.



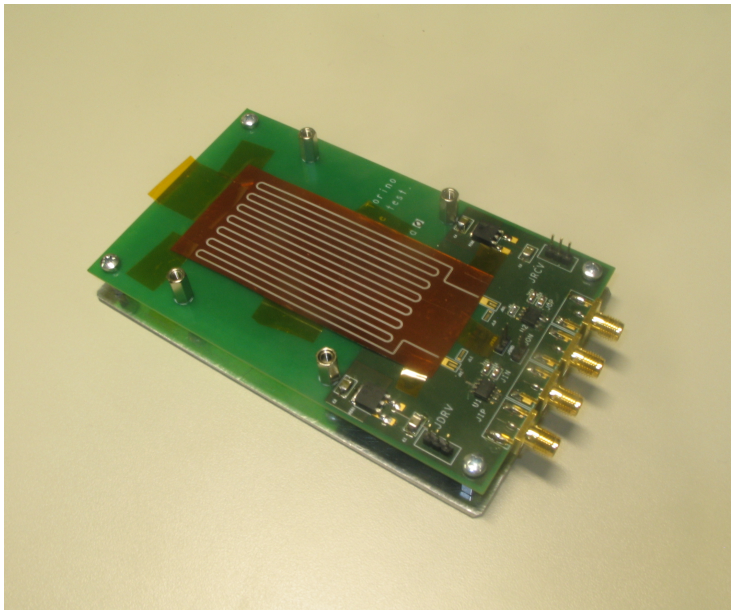
The test has been performed at Laboratori Nazionali Legnaro (INFN) with several heavy ions to evaluate the cross section. Tacking into account the Panda environment this result leads to an expected value of 2.3SEU/(chip·h): that asks for a better radiation hardness.

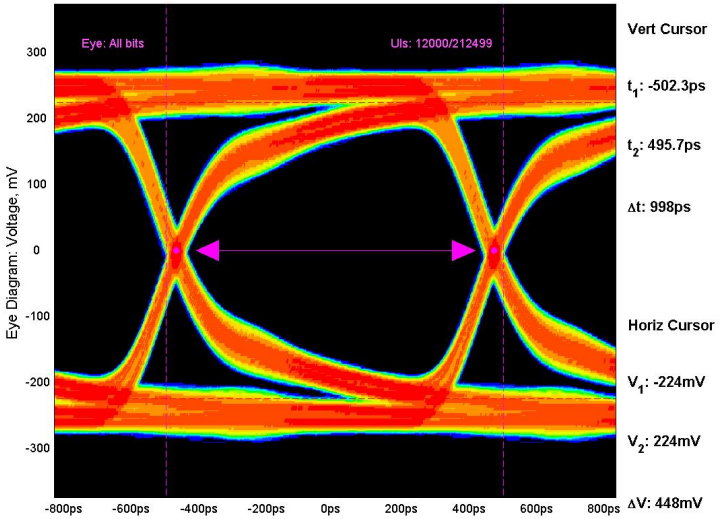
New Topix prototype.



The new prototype takes up an area of $4.5 \cdot 4mm^2$ and it features 640 pixel cell implemented with triple redundancy registers, a serial output and pads for bump bonding to test a complete hybrid.

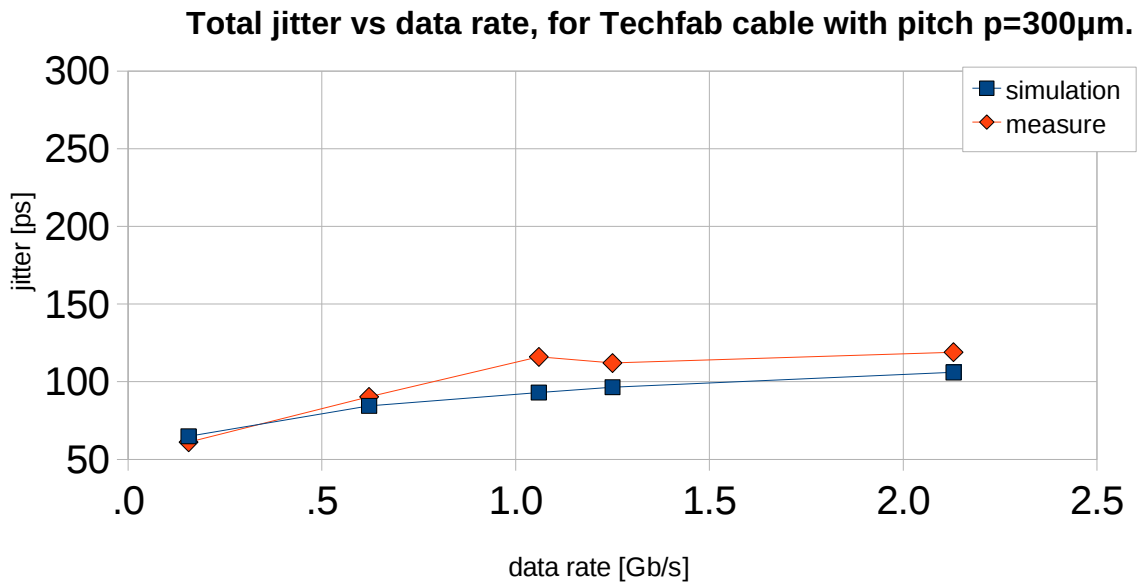
Tests on the aluminum cable.





Some tests are in progress to evaluate the aluminum microstrip cables made by two producers (Cern and Techfab). In the first case a laminated sheet of aluminum over polyimide is etched, while in the second case the metal is deposited on top of the insulator.

Total jitter for aluminum cable.



At present both microstrips work well on a 1m total length for data rate up to 1Gb/s (and beyond for the Techfab cable); the bit error rate test has been performed without any failure. However the Cern cable shows a better bonding capability.

Short summary.

- The prototype test produced satisfying results and suggested some modifications to reduce the threshold dispersion, an enclosed structure for selected transistors and triple redundancy for configuration and data registers.
- A new prototype is under design for the next submission, and it features a serial output to match with the GBT chipset.
- The new prototype features the special pads on each cell, to check the bump bonding process with a thinned pixel sensor.
- The tests regarding the aluminum microstrip cable are ongoing to select the product that matches better with Topix readout and the GBT chipset.