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The Silicon Pixel Readout Architecture for the Micro Vertex Detector of the PANDA Experiment

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The electronic readout architecture for the silicon pixel sensors of the PANDA Micro Vertex Detector is presented. The pixels will provide timing, position and energy information; moreover, no trigger signal is foreseen, thus leading to a huge amount of data to be transmitted.
The foreseen readout system is based on a custom ASIC development, named ToPiX, which provides time information via a time stamp synchronous with the 155 MHz global clock signal and energy information via the Time-over-Threshold technique. High speed serial links and early electrical to optical conversion are adopted to reduce the amount of cables and material.

Summary

The PANDA (antiProton ANnihilations at DArmstadt) experiment at the future FAIR facility currently under construction at Darmstadt, Germany, aims to the study of the antiproton-proton and antiproton-nucleus annihilation reactions. The detector layout is divided into a target section, positioned around the interaction point, and a forward section, positioned downstream. The interaction point is defined by the intersection of the beam pipe, where the antiproton beam is circulated, and the target pipe, where the target (protons or ions) is injected.
The Micro Vertex Detector (MVD) is the innermost part of the detector and will consist of silicon pixel and strip sensors. The sensors are organized in a barrel section, with two pixel and two strip layers, and a forward section, with 6 disks with mixed pixel and strip sensors. A hybrid pixel solution was chosen as a baseline concept to accommodate the high radiation dose (up to 100 kGy) and the required time resolution. Prototypes of the pixel sensors, based on epitaxial silicon, have been produced and tested after irradiation.
The main requirements for the pixel detectors include a pixel size of 100 um x 100 um, an amplitude resolution limited by the Landau fluctuation and a time resolution of 6.4 ns. Moreover, no hardware trigger signal will be available and therefore all the data has to be sent to the data acquisition system. Owing to these peculiar requirements, an ASIC based custom solution for the electronic readout of the pixel detector is under development.
The ASIC, named ToPiX, will provide the time position of each hit with a resolution of 6.4 ns and a measure of the charge released with a Time over Threshold (ToT) technique. ToPiX will consist
of a matrix of 116x110 cells with a pixel size of 100x100 um^2, a column readout logic and 320 Mb/s serializers for data transmission. A CMOS 130 nm technology has been used to reduce the size of the circuitry and to provide tolerance to radiation effects related to the total ionizing dose. Various single event upset protection techniques are under evaluation in order to provide the best size versus protection efficiency trade-off. A prototype of the ToPiX ASIC, with the full pixel cell and column and a simplified end of column logic has been designed and tested before and after irradiation. A new version of the chip is currently under design.
The stringent requirements in terms of space, material and routing directions for the cabling of
the MVD lead to an architecture based on high speed optical links. The GBT chipset under development at CERN has been chosen as baseline solution for the interface to the data acquisition, clock distribution and detector control systems.
Low mass cables based on aluminum on kapton technique are under development for the high speed interconnections between ToPiX and the optical transceiver. Prototypes from two different producers have been tested.

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