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Radiation-hard ASICS for optical data transmission in the first phase of the LHC upgrade

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The LHC at CERN will be upgraded in two phases to increase the design luminosity by a factor of ten. The ATLAS experiment plans to add a new pixel layer to the current pixel detector during the first phase of the upgrade. The optical data transmission will also be upgraded to handle the high data transmission speed. A new driver and receiver ASIC has been designed for this new generation of optical links to incorporate the experience gained from the current system, including redundancy circuitry to bypass a bad channel in a VCSEL or PIN array.

Summary

The LHC at CERN is currently being commissioned to be the highest energy collider in the world. In addition, planning has already been initiated to increase the design luminosity by a factor of ten in two phases. The ATLAS experiment plans to add a new pixel layer to the current pixel detector during the first phase of the upgrade. The optical data transmission will also be upgraded to handle the high data transmission speed. An ASIC with multiple circuits has been designed for this new generation of optical links to incorporate the experience gained from the current system.

The ASIC has been designed using 130 nm CMOS process. It contains both driver and receiver chips to couple to a 12-channel VCSEL or PIN array where one channel of each array is designated as a spare. This allows redundancy in both directions to bypass a bad VCSEL or PIN channel. The ASIC contains four VCSEL driver chips, four PIN receiver chips, and the associated circuitry to control the re-routing of the signals to the spare channels.

Each of the receiver contain a pre-amplification, a bi-phase mark (BPM) clock/data recovery circuit, and has low voltage differential signal (LVDS) outputs for both the clock and data. All receivers are designed to operate with BPM input of 40 Mb/s. One receiver includes circuitry to extend its speed to 80, 160, or 320 Mb/s. Two-channel multiplexers have been inserted in the post amplification paths of the non-spare receiver channels to allow the signal from the spare amplifier channel to be routed. In order to allow remote control of the chip, a command decoder has been included in three of the receivers. The command decoder has been designed to be single event upset (SEU) tolerance. The command word for configuring the chip is formed by a majority vote of the three command decoders. To further improve the SEU tolerance, all latches are based on a dual interlocked storage cell (DICE) latch.

The four driver channels are designed to operate up to 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a VCSEL driver. Two channels have the capability to add a pre-emphasis to the VCSEL modulation current. One channel is designated as the spare channel and contains a 16:1 multiplexer. The multiplexer allows routing of the received signal from any of the three channels to the spare channel output. The 8-bit DAC is used to set the VCSEL modulation current. To enable operation in case of a failure in the communication link to the command decoder, we have included a power on reset circuit that will set the VCSEL modulation current to 10 mA upon power up.

The ASIC will be irradiated with 24 GeV/c protons at CERN this summer. We will present the performance of the ASIC before and after the irradiation.

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