Digital Trigger System
for
the COMPASS Experiment

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Outline

1. COMPASS experiment
2. Triggering in COMPASS or event selection
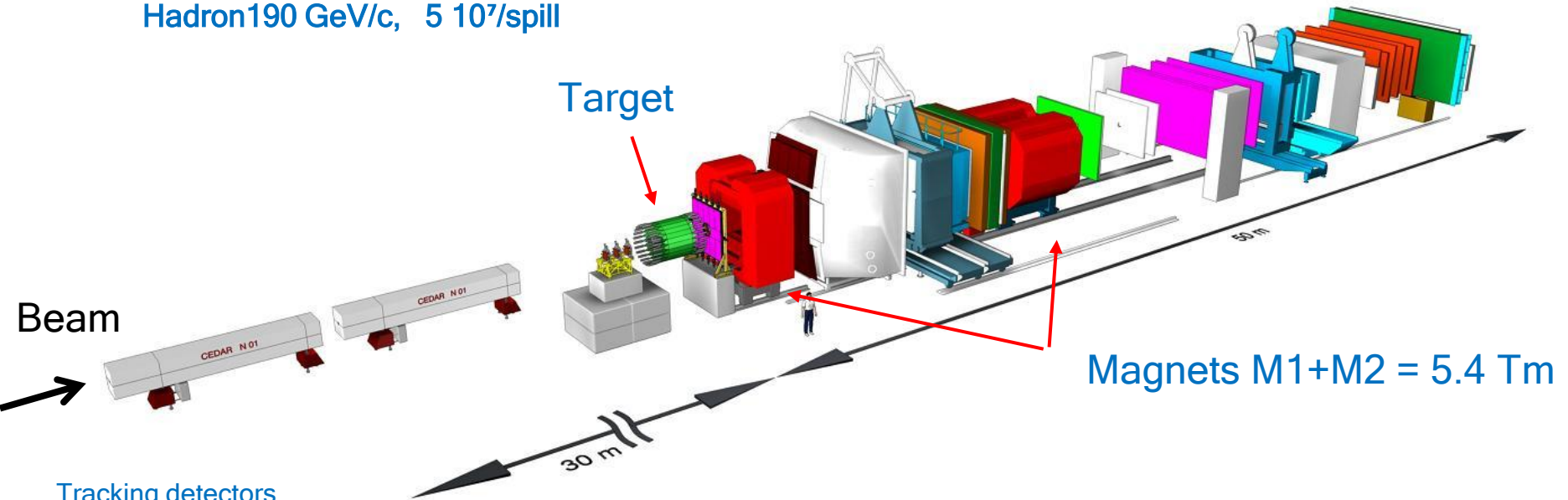3. Digital ECAL2 trigger
4. TDC based trigger
5. Summary and Outlook

COMPASS spectrometer @SPS CERN

Fixed target experiment , first run 2002
Beam:
  Muon 160 GeV/c, $2 \cdot 10^8$/spill
  Hadron190 GeV/c, $5 \cdot 10^7$/spill

Target

Beam

Magnets M1+M2 = 5.4 Tm

50 m

30 m

Tracking detectors
  • silicon
  • MicroMega & GEM
  • Drift Chambers, Straws
Calorimetry
  •ECAL1,2; HCAL1,2
PID
  • CEDAR
  • RICH
  • Muon Wall(filter)
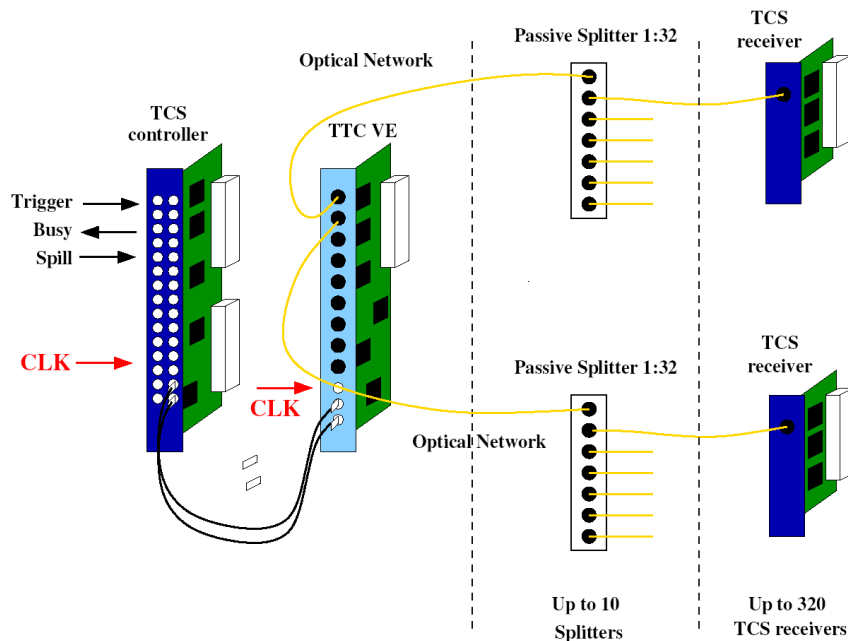
Physics objections:
  Nucleon spin structure
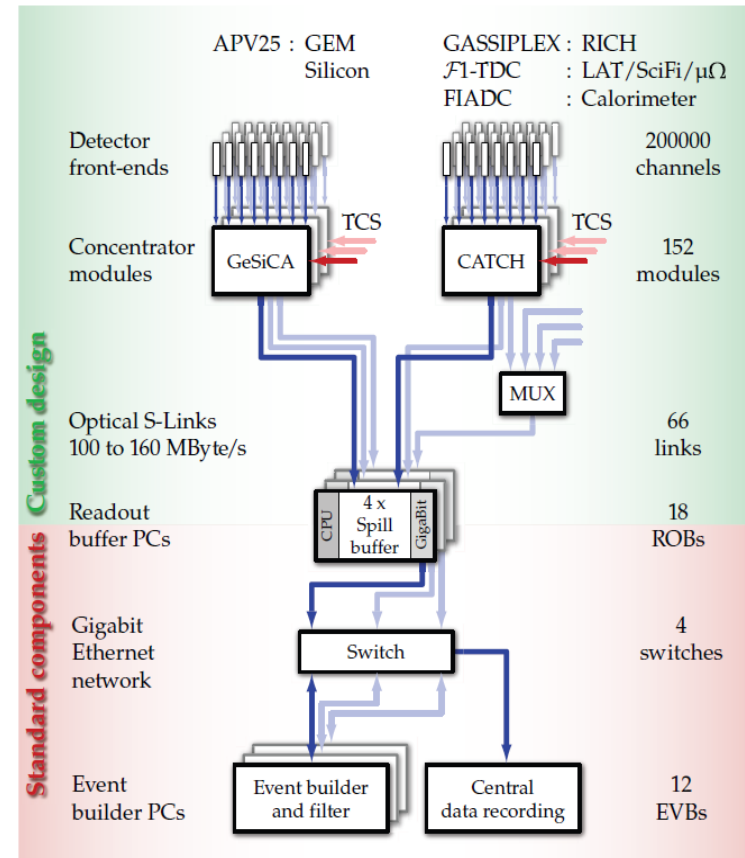 Spectroscopy of hadrons

DAQ and Trigger Distribution System

Trigger Control System

DAQ architecture
DATE(ALICE) DAQ software

- TCS architecture derived from TTC (LHC)
- Built using commercial components
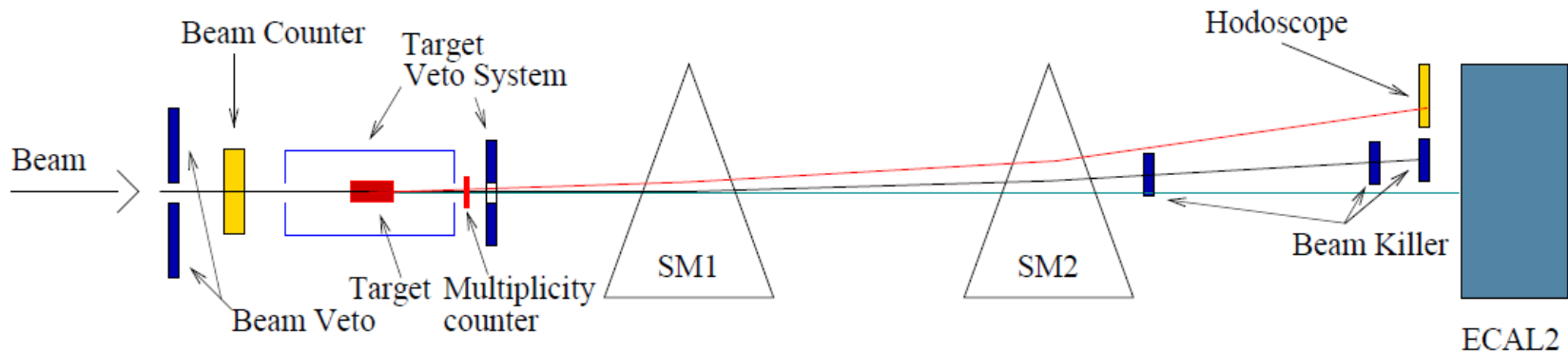- Trigger distributed synchronously with 38.88 MHz clock

Maximum trigger rate: 30kHz

Triggering or event selection

Example of Simplified Hadron program triggers:

Diffractive trigger : Beam * Recoil Proton * $\overline{VETO}$ * $\overline{\text{Beam Killer}}$

Primakoff trigger : Beam * $\overline{\text{Beam Killer}}$ * (ECAL2 Energy > Threshold)

Total number of trigger channels ~140

Two complementary developments for Digital Trigger System :
1. Electromagnetic Calorimeter Trigger – total energy
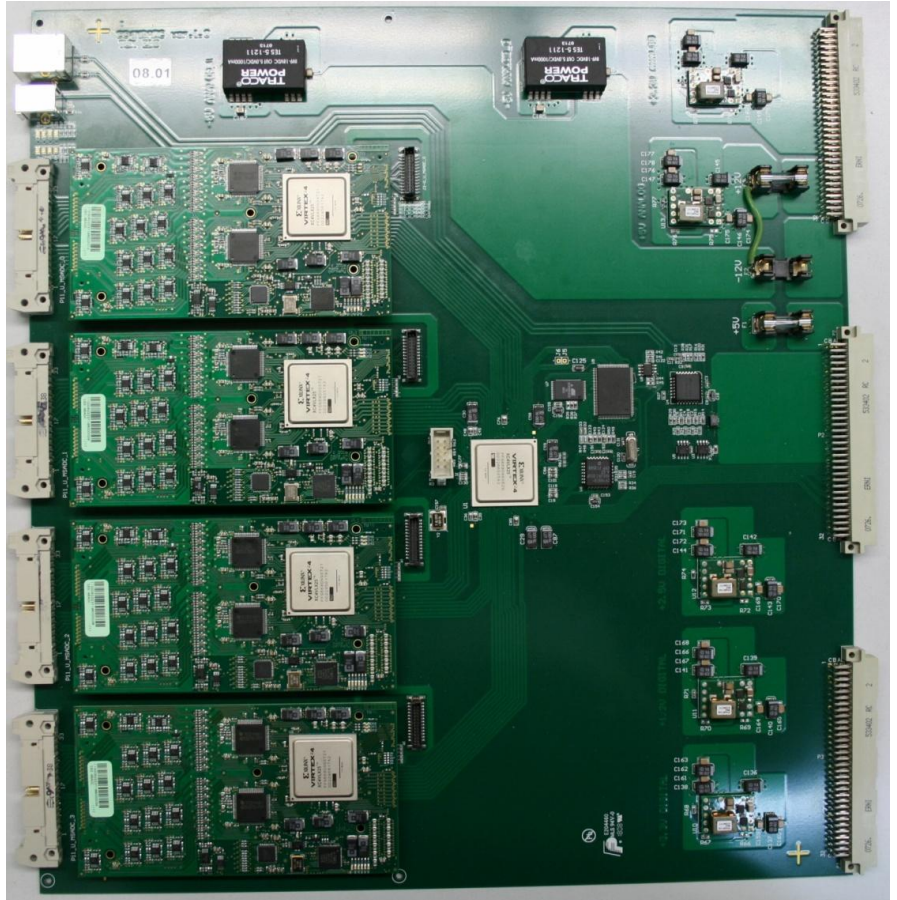2. TDC based trigger logic

ECAL2 readout electronics

MSADC 9U VME card:

- 12 bit ADC
- 77.76 MS/s
- 4+1 FPGA: XC4LX25
- 4x16 = 64 channels
- Debug FPGA interface at P2

Two data streams in FPGAs

- DAQ data stream
- Trigger data stream

Trigger data processor

1. **Signal detection:**
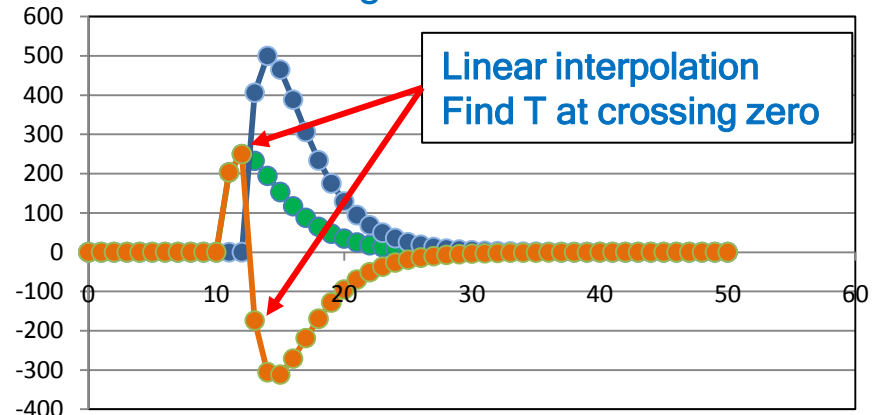   - Threshold 600MeV

   ~0.5% of dynamic range

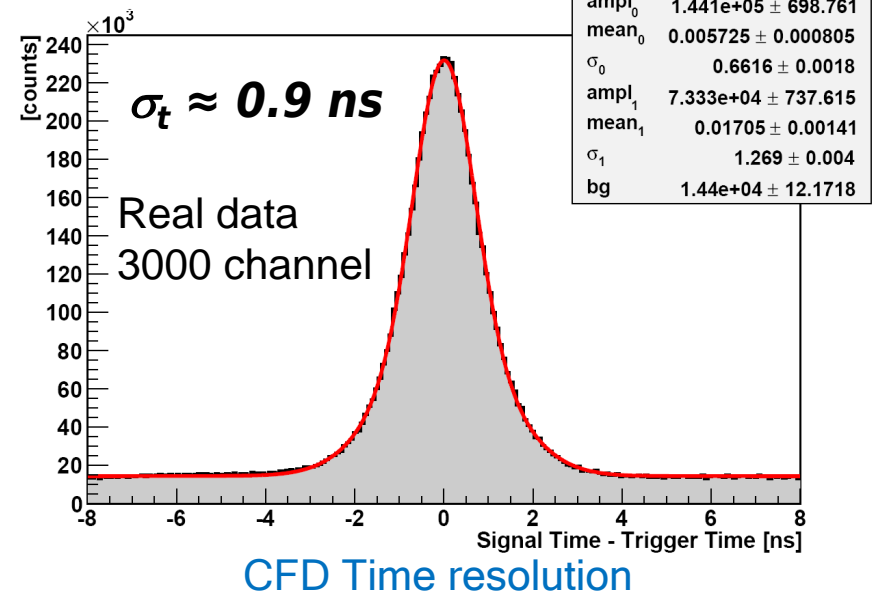2. **Signal Time**
   - digital CFD
   - TIME IN all channels

3. **Amplitude :**
   - maximum value
   - Channel wise normalization i.e. conversion ADC values to Energy

Digital CFD

Linear interpolation
Find T at crossing zero

Temporal Residual

$\sigma_t \approx 0.9\ ns$

Real data
3000 channel

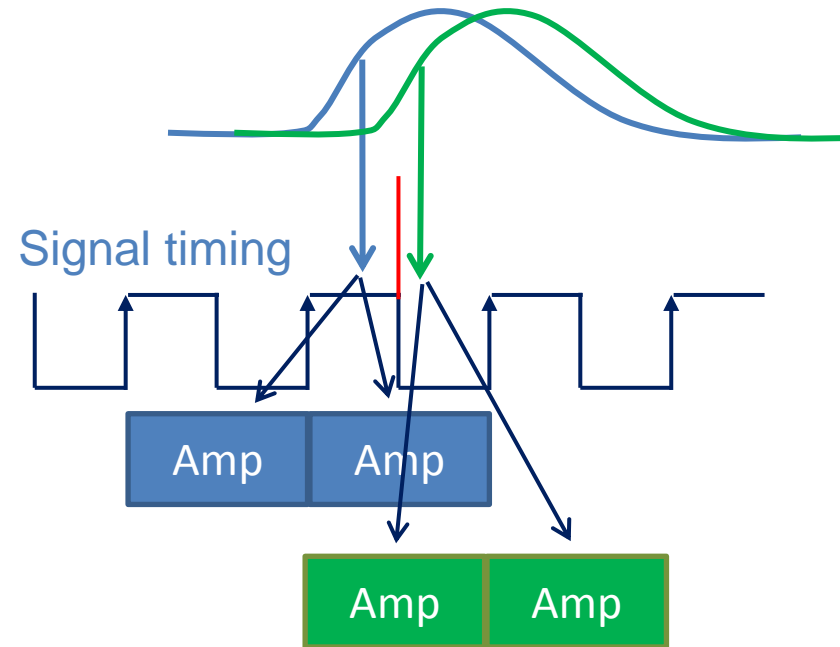| χ^2 / ndf	6262 / 194
$ampl_0$	$1.441e{+}05 \pm 698.761$
$mean_0$	0.005725 ± 0.000805
σ_0	0.6616 ± 0.0018
$ampl_1$	$7.333e{+}04 \pm 737.615$
$mean_1$	0.01705 ± 0.00141
σ_1	1.269 ± 0.004
bg	$1.44e{+}04 \pm 12.1718$

[counts]

Signal Time - Trigger Time [ns]
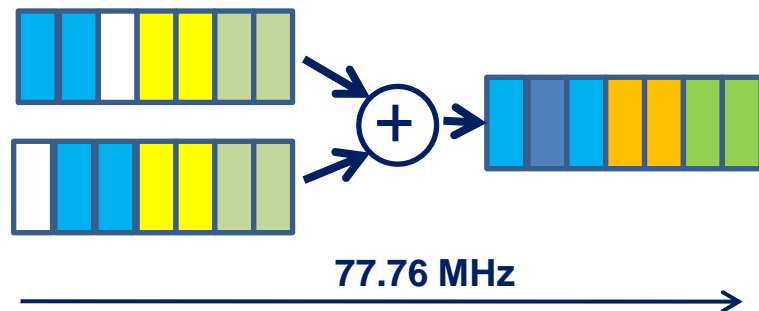
CFD Time resolution

Summation logic

- 77.76 MHz clock – common time reference system
- All pipelines synchronized to absolute time
- To avoid mismatch at clock boundaries

signal amplitude copied to two consecutive pipeline cells
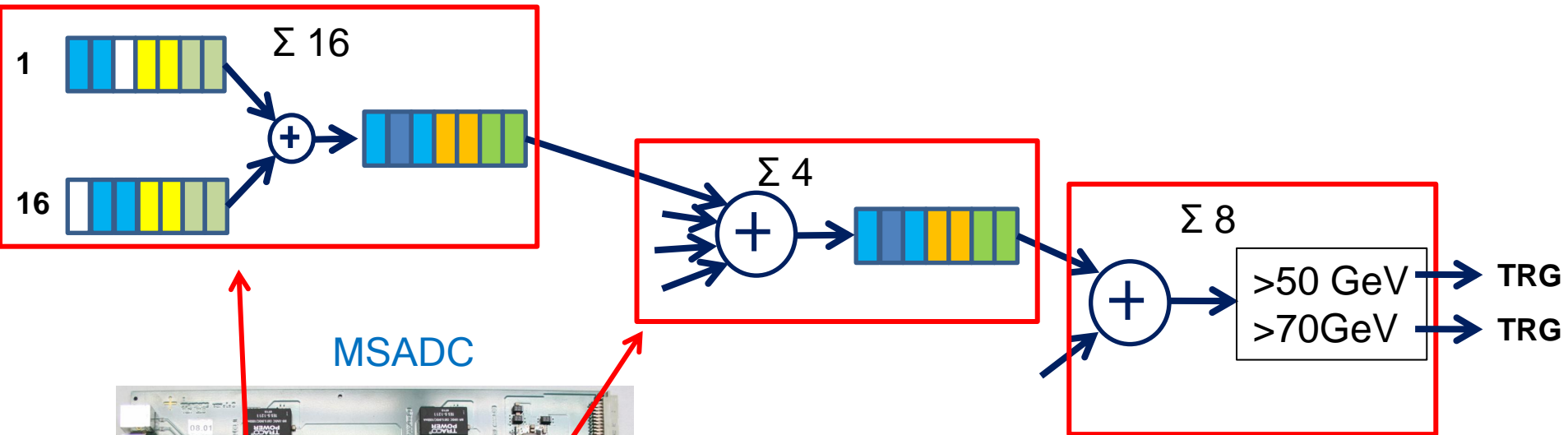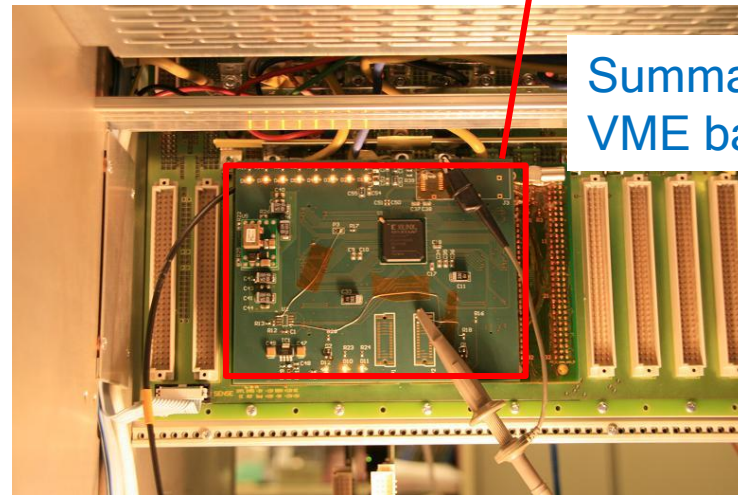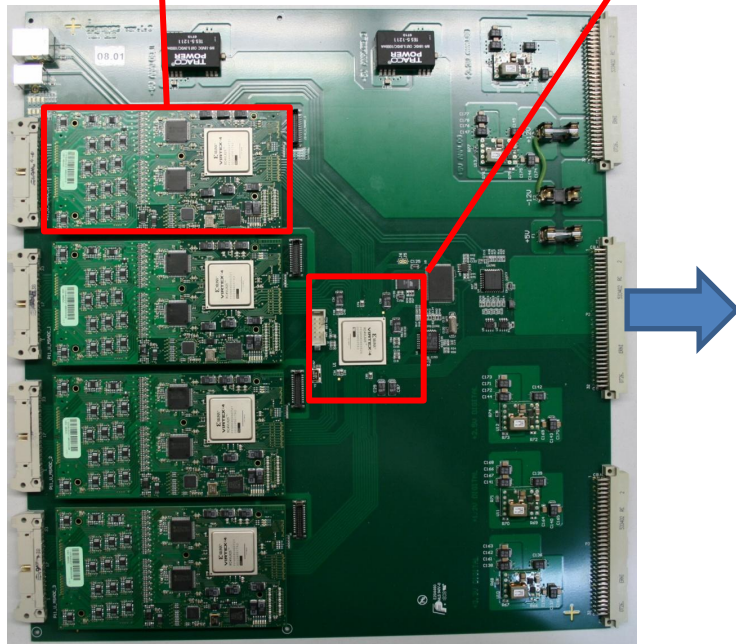
- Pipeline summation

Signal timing

Amp   Amp

Amp   Amp

77.76 MHz

Σ 16

1

16

Σ 4

Σ 8

>50 GeV → **TRG**

>70GeV → **TRG**

MSADC

Summation card on
VME backplane

ECAL2 trigger performance during pilot Primakoff run in 2009

ECAL2 trigger configuration in 2009

- Up to 512(32x16) channels or 8 MSADC modules included in Trigger

- Actually used 12x12 – hole 2x3

- Two triggers
  - >50GeV – prescaled by factor two
  - >70GeV

- ECAL2 trigger latency: about 100 clock cycles

- Trigger latency increased by 720 ns

EC02P1__ Number of hits vs XY, amp> 20
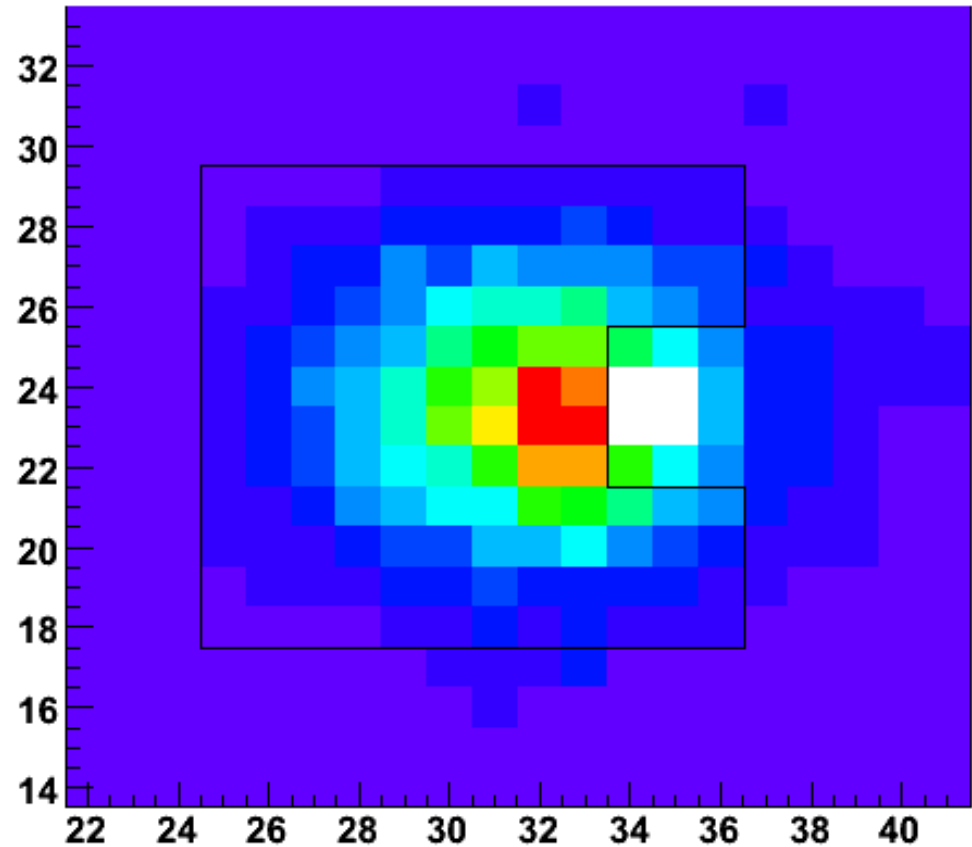
Trigger rate vs threshold for 12x12
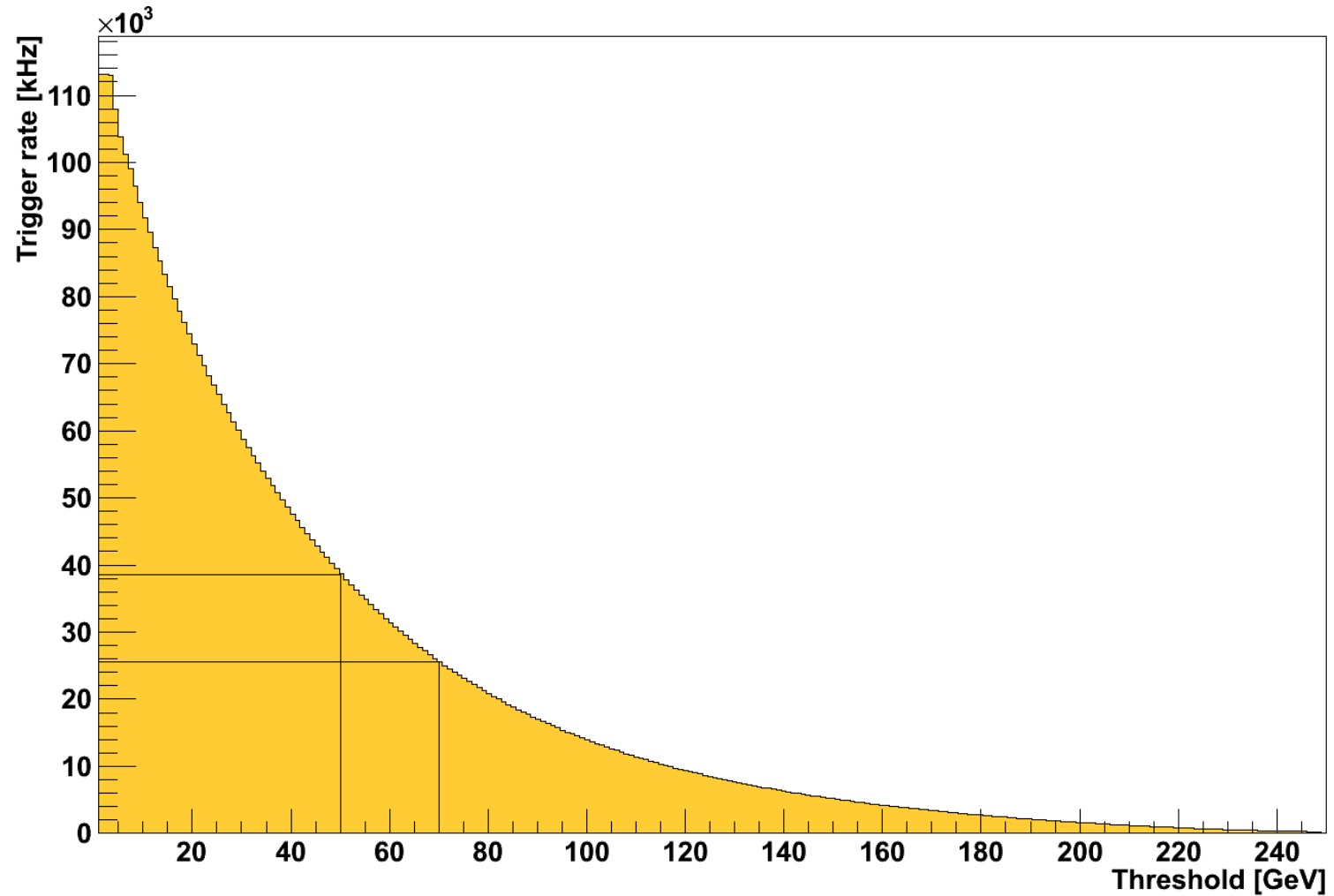
ECAL2 trigger rate vs area
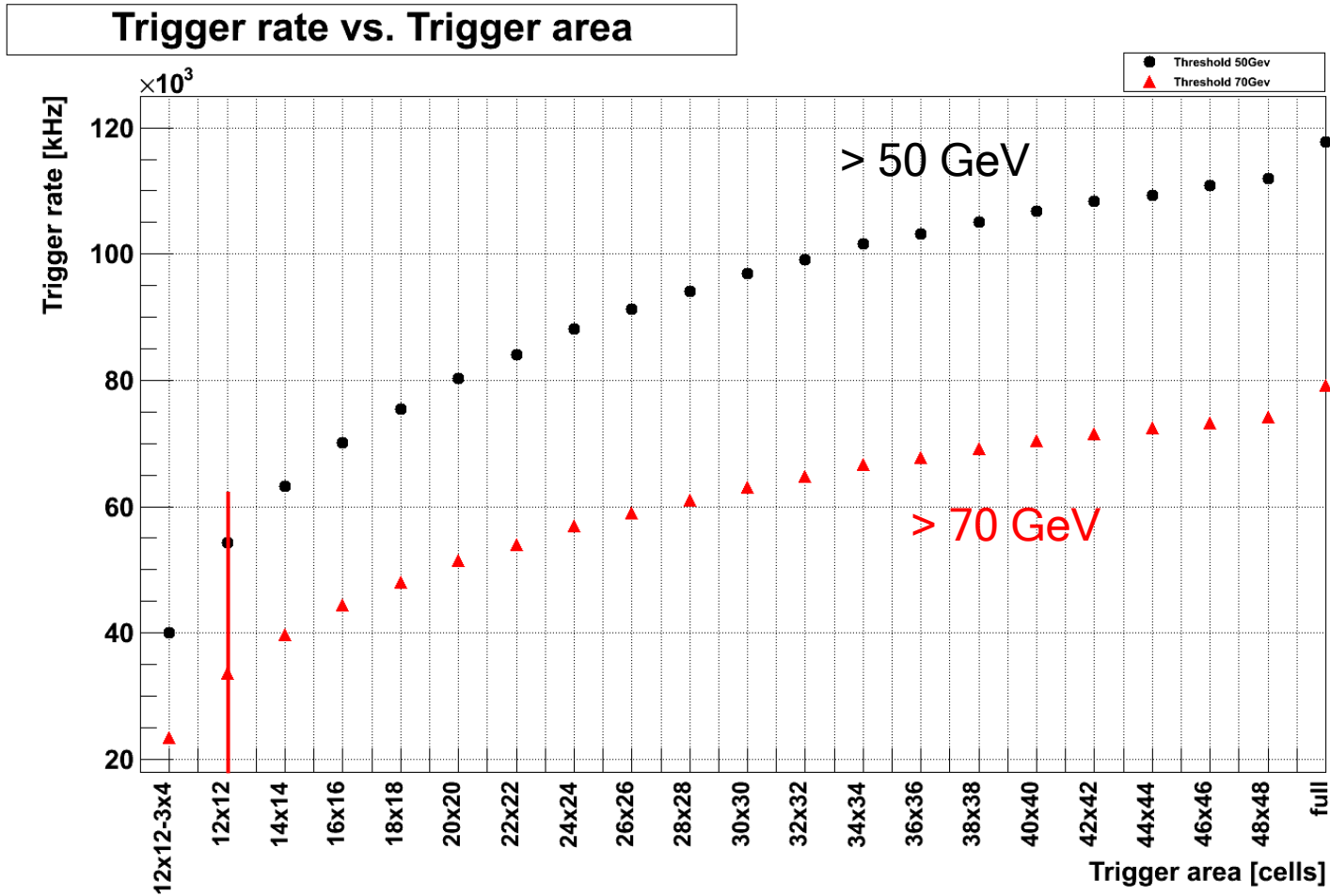
Trigger efficiency

effi70

effi70	
Entries	336
Mean	138.3
RMS	35.81
p0	0.9903
p1	76.09
p2	3.336

$\sigma = 3.3$ GeV
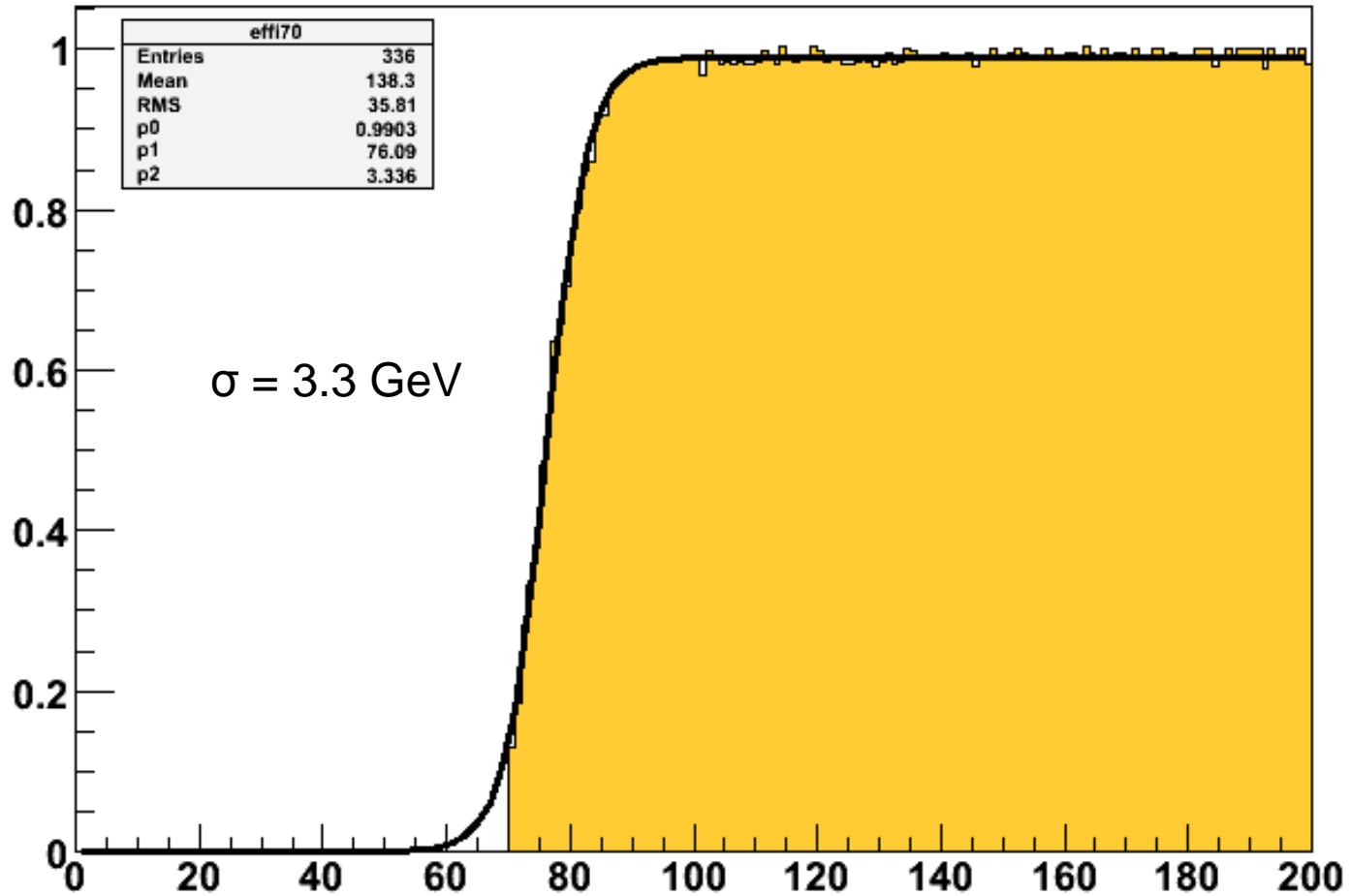
ECAL2 trigger outcome

- Trigger architecture fulfill requirements for Primakoff measurements
- Trigger rate would be too high to include all 3000 channels and to lower threshold
- Pipeline data processing takes more clock cycles than anticipated and cause long latency – ~90 clock cycle

Solutions and further improvements

- Improve trigger selectivity by providing cluster information instead of total sum
- Increase processing speed to 200-300 MHz

TDC based Trigger Logic in FPGA

Motivation

Currently COMPASS trigger electronics based mostly on NIM modules.

Substitute NIM logic by flexible FPGA based electronics

What is Trigger logic

Interconnection of si

How Digital Trigger Log

– Synchronous pipe

– Convert analog Ti   FPGA)

– Unified interface   erface with TDC
  information

– Library componer

How to create FPGA

– Interconnection   ile

– User creates sc

– Software tools

Goal: provide a possibility to create Complex Trigger Logic wo
FPGA/VHDL knowledge

Trigger logic components

- TDC
- Programmable delays
- AND, OR, NAND with programmable coincidence window(GATE) and master signal
- Time calibration – automatic scanning signal timing
- Monitoring
- DAQ interface – no need for splitting signals to TDCs
- Inter module interface for scaling up the system

Software

- GUI for creating trigger logic schematic
- Software for generation VHDL code and project files
- Standard Xilinx tools to be used for implementation
- No special knowledge required for using the system

TDC design in Virtex5 FPGA

- Conservative TDC design using built-in SERDES hard cores

LVDS

0 ps
IDELAY → SERDES

312 ps
IDELAY → SERDES

624 ps
IDELAY → SERDES

936 ps
IDELAY → SERDES

400MHz DDR

DECODER
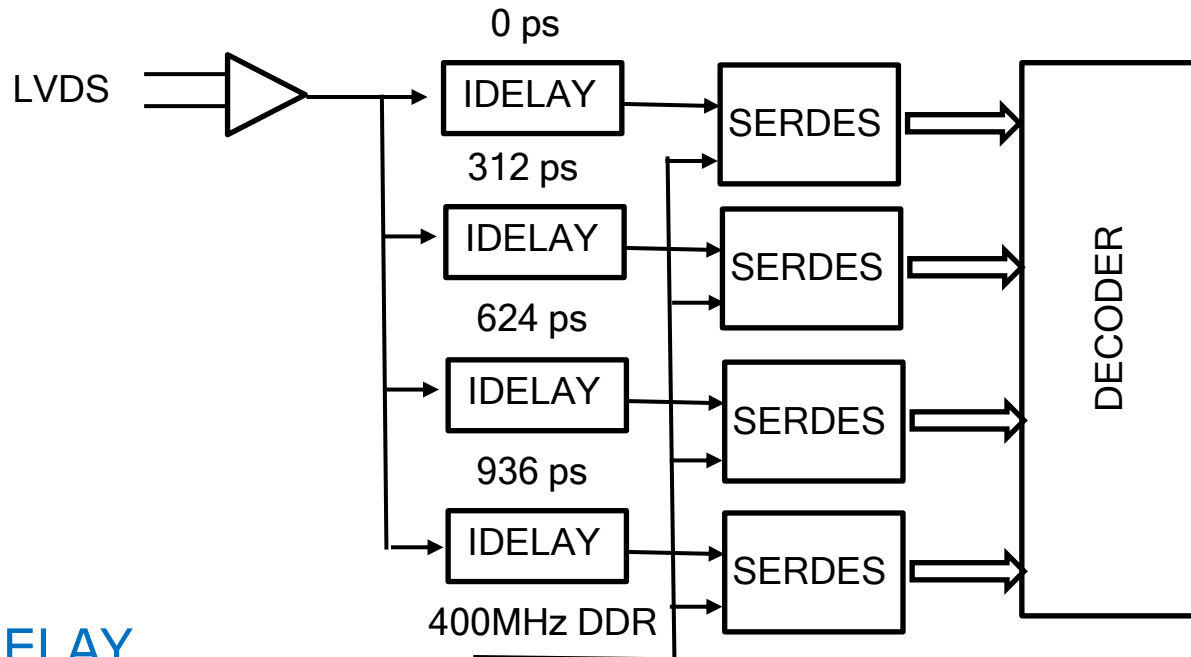
- IDELAY
  - 64 taps, 78 ps/tap
  - Calibrated and independent from process, temperature and voltages
- Bin size 312 ps
- Auto calibration at power up – tuning IDELAY
- About 50 TDCs with XC5VLX50

TDC resolution

Time difference between two signals

Time resolution	
Entries	4
Mean	13.83
RMS	0.4662
χ^2 / ndf	718.4 / 1
Constant	$7.107e+04 \pm 298$
Mean	14.31 ± 0.00
Sigma	0.4593 ± 0.0011
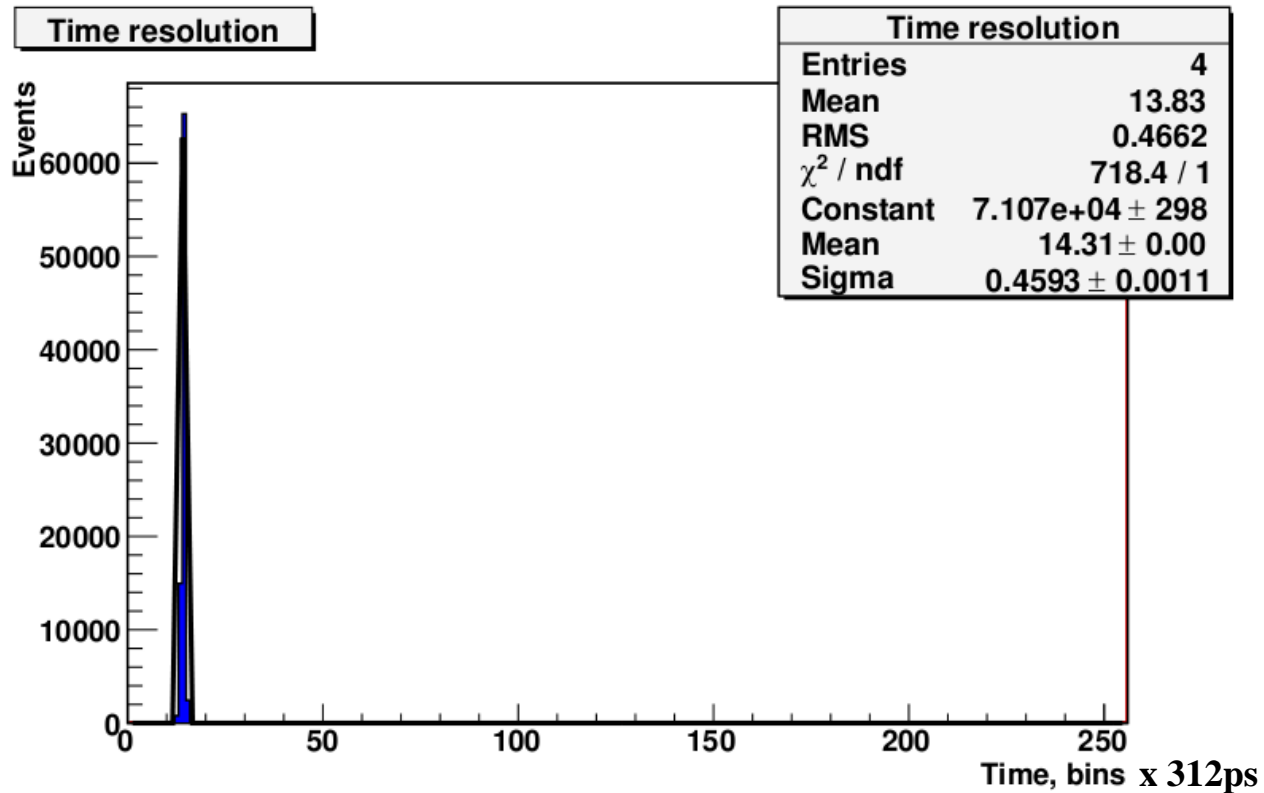
σ = 0.46 * 312/SQRT(2) = 101 ps

TDC performance

Differential nonlinearity

Bin plot

21 % or better

Temperature Stability, TDC Bins
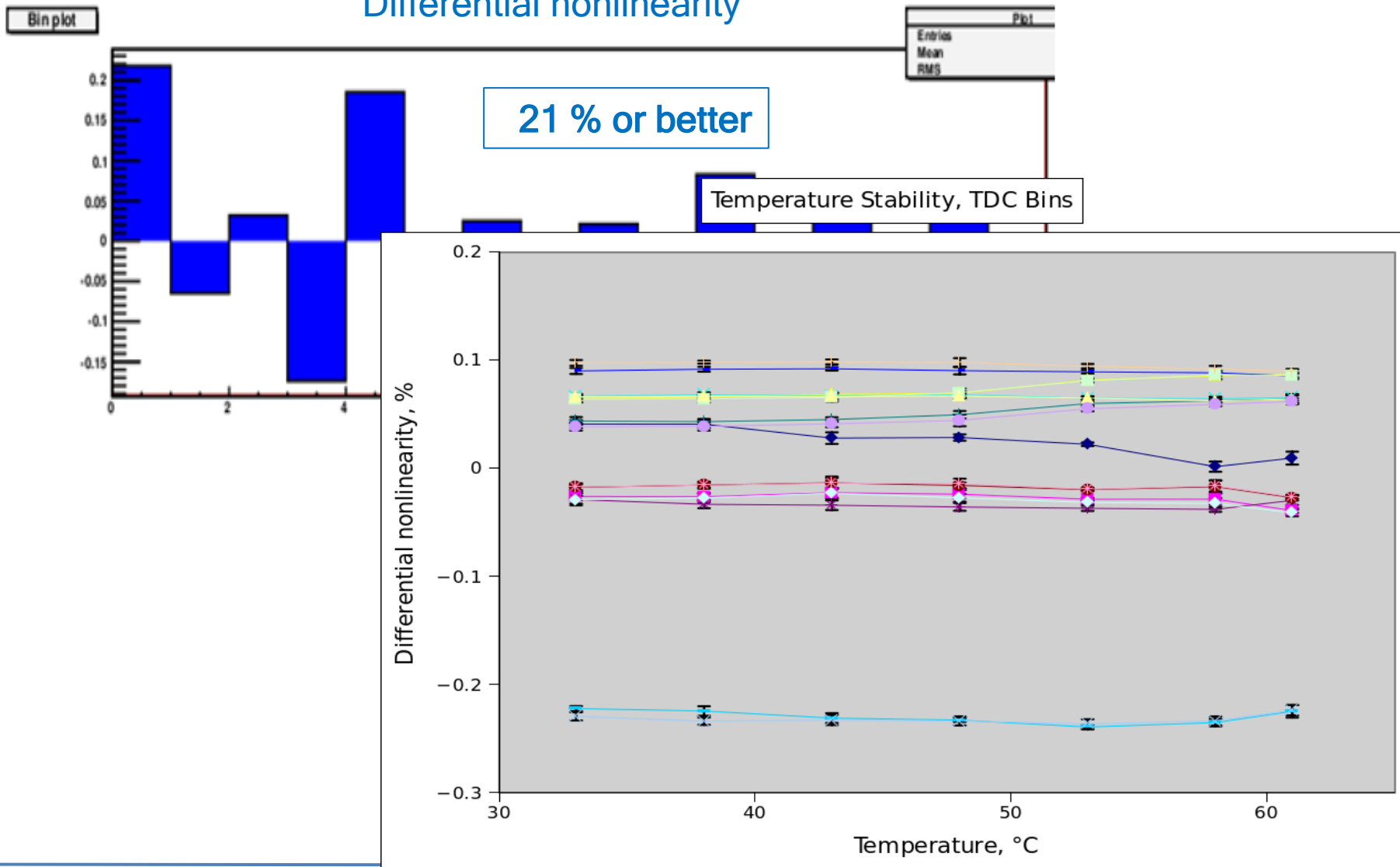
AND/NAND/OR component

Component parameterization

- Function: AND, NAND, OR
- Number of inputs
- Component Gate
- Offset

Ts(): | S Time 16 bits |

Example: (S1 and S2)
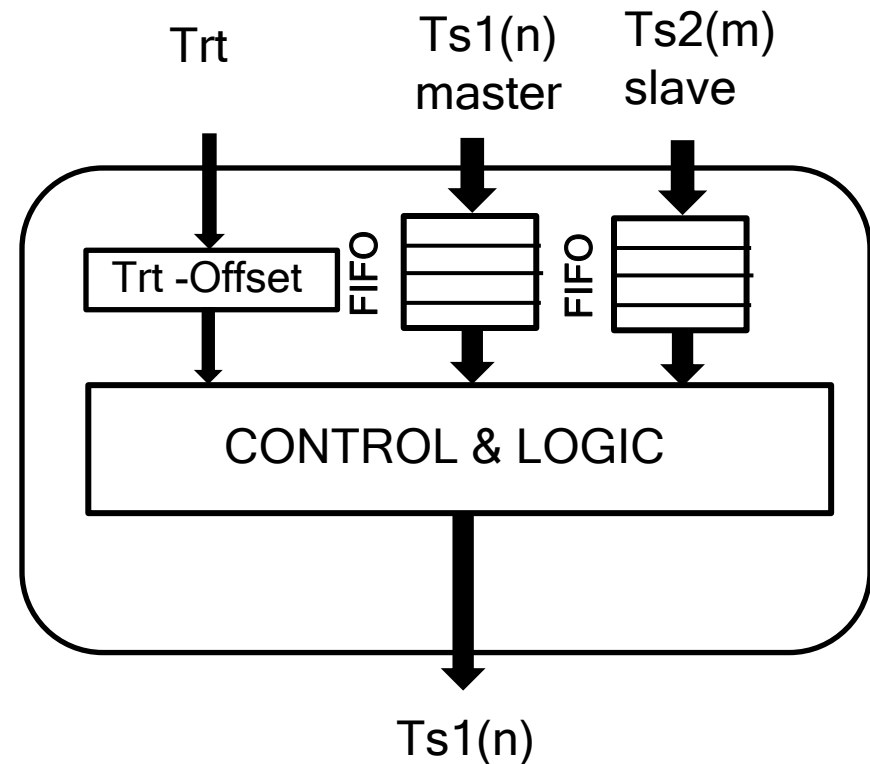
Trt - real time

Time to processed:

$Ts1(n) < Trt - OFFSET$

$Ts2(m) < Trt - OFFSET$

Coincidence conditions:

$(Ts2(m) - GATE) < Ts1(n) < Ts2(m)$

Trt   Ts1(n) master   Ts2(m) slave

Trt -Offset   FIFO   FIFO

CONTROL & LOGIC

Ts1(n)

Generation top level VHDL file

```xml
- <trigger>
    <name>tttt</name>
    <type>AND</type>
    - <signal>
        <name>ts1</name>
        <source>TDC</source>
        <gate>10</gate>
        <notFlag>0</notFlag>
        <master>0</master>
    </signal>
    - <signal>
        <name>ts2</name>
        <source>test</source>
        <gate>10</gate>
        <notFlag>0</notFlag>
    </signal>
    - <signal>
        <name>ts3</name>
        <source>TDC</source>
        <gate>10</gate>
        <notFlag>1</notFlag>
        <master>1</master>
    </signal>
</trigger>
```

```vhdl
tttt : trigger_logic
    generic map (
        LEVEL => 2,
        SLAVE_NUMBER => 2,
        DELAY_PRO_LEVEL => 10,
        TRIGGER_TYPE => 0
    )
    port map (
        control => control,
        t => t,
        channels_in => channels_in_tttt,
        result => result_tttt
    );
```

Digital trigger hardware

Digital trigger module is in development stage
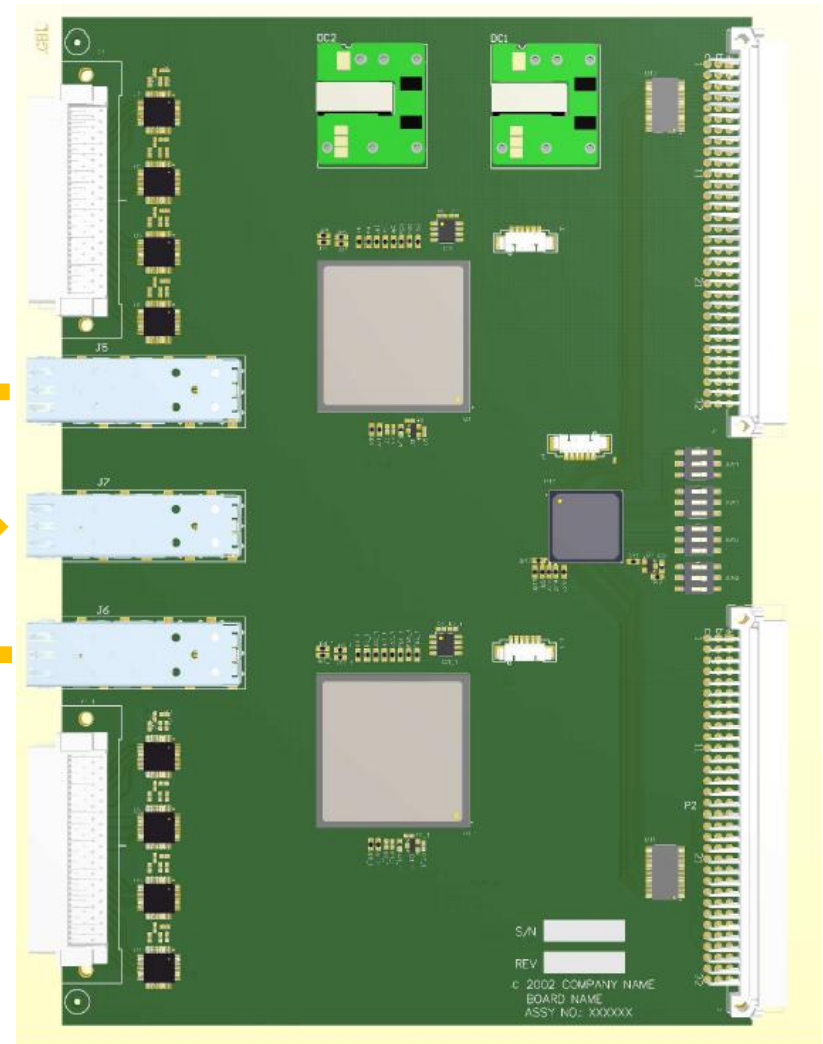Further optimization of architecture going on

32 LVDS inputs

From/To
Previous/Next Trigger logic level

From TCS Trigger Distribution System

From/To
Previous/Next Trigger logic level

32 LVDS inputs

Status of development

- FPGA TDC implementation
  - completed and tested
- Logic components AND, NAND, OR
  - implemented in VHDL code and simulated
  - To be tested in hardware
- Time calibration
  - Implemented in VHDL
- Software to generate VHDL code
  - ready for XML input
  - GUI in the list to be developed

Summary and outlook

ECAL digital trigger

- Successful integration ECAL2 digital trigger logic into existing readout electronics – 512 channels
- Problems to extend to 3000 channels due to too high trigger rate
- Studying implementation of more advanced logic to reconstruct clusters, cluster Time and Amplitude

TDC Digital Trigger Logic

- TDC with 110ps resolution and 312 ps/bin
- Concept of programmable TDC based trigger logic
- Basic tools to generate VHDL project

Goal: to complete project by summer 2011