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Digital Trigger for the COMPASS experiment

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The COMPASS digital trigger system is an FPGA based real time trigger logic which detects event signature by analyzing already digitized detector information. The trigger system has distributed multi stage architecture. The first stage is implemented in front-end electronics and it runs in parallel to data acquisition. The COMPASS event selection criteria are based on event geometry, extracted from hits in scintillating counter detectors, and a calorimetric trigger. A signal time of scintillating counters is measured with a specially developed for this project FPGA TDC. The calorimeter trigger logic evaluates a total energy detected in a calorimeter by extracting signal time and signal amplitude from digital waveform of detector signal. The architecture and performance of the digital trigger system are discussed.

Summary

COMPASS (Common Muon and Proton Apparatus for Structure and Spectroscopy) is a two stage magnetic spectrometer, built for the study of the gluon and quark structure and the spectrometry of hadrons using high intensity muon and hadron beams of (100-300 GeV/c) from CERN's Super Proton Synchrotron.

A development of the digital trigger logic started in 2008 when it was decided to include information about a total energy released in the second electromagnetic calorimeter (ECAL2) into the trigger in order to enrich the statistic for the Primakoff reaction measurement. An existent read out module of the ECAL2, built using pipeline sampling ADC, and a read out logic implemented in a Xilinx Virtex 4 FPGA, allowed relatively easy to integrate additional logic into the FPGA. A trigger logic code which extracts online the signal amplitude and time was added to the FPGA firmware. In addition, the ECAL2 readout electronics was extended by a specially developed interface card (BP card), mounted on the back side of the VME backplane. The BP card receives energy information from 8 attached front-end modules, calculates the total energy as a sum of coincided in time signals from 512(3000) crystals. The BP card has additional interfaces to communicate to 5 other BP cards of the calorimeter. At the last stage of the logic, a value corresponding to the total energy is compared to a programmable threshold and a pulse synchronous to 77.76 MHz is generated. This frequency is synthesized from the common experimental clock of 38.88 MHz. The calorimeter trigger pulse shall coincide with analogue trigger signals of other detectors in order to be accepted by the DAQ.

The calorimetric digital trigger was commissioned and successfully operated for 512 channels, although, the electronics design allows to scale up the system to all 3000 channels. The system demonstrated a very good time and energy resolution, flexibility to adjust timing and energy response values. The only problem which caused some extra work in integration the calorimetric trigger was a longer processing time by 500 ns respectively to an analogue implementation of the summation logic. This problem would not cause any problems if the rest of the trigger logic was implemented in the digital way as well.

In parallel to the development of the calorimetric trigger, a development of a TDC trigger module was launched. It is a 6U VME module which houses 2 Virtex5 FPGAs. It features 64 TDC channels, implemented within the FPGAs and 80% free resources for trigger and readout logic. The module has three external interfaces: one is to hook the module to the DAQ for data taking, and two others for interconnection. The TDC circuit is implemented using four IO SERDES cores in parallel. Such solution gives fixed bin size of 312 ps and an independence of TDC performance parameters from temperature. The time resolution of the TDC is 100 ps and the differential nonlinearity was measured to be in the worst case scenario of 15%. An important feature of this development is a provision of parameterized IP cores such as coincidence, anticoincidence, multiplexer, mean timer, delay and so on. Any complex trigger logic shall then be built by using this set of IP cores. It is foreseen to describe the trigger logic schematic in an ASCII format which is later used to generate a complete VHDL project including constrain file for the ISE Xilinx development tool. The procedure requires a minimum experience in usage of the Xilinx tools.

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