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CMS Pixel Detector with new Digital Readout Architecture

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The CMS pixel detector is planned to be upgraded in 2015 to a new one with a significantly reduced material budget. The new pixel system with more layers has to operate through the existing services at double the luminosity. Therefore a new readout scheme is implemented in the new pixel read out chip (ROC).
A detailed description of the ASIC modifications of the digital readout interface of the ROC is presented as well as the results and the performance of the physics based electronic simulations of a complete pixel module consisting of 16 pixel ROCs and a token bit manager chip.

Summary

The CMS pixel detector is planned to be upgraded in 2015 from currently three to four tracking points. For the barrel part (BPIX) this means a new four layer design, whereas for the forward part (FPIX) this implies going from currently 2 disks to 3 disks on each side. The new upgraded pixel detector will significantly reduce the material budget in the sensitive tracking region.
Since the new pixel system will have to be operated through the existing services a number of changes need to be done to the current CMS pixel readout chip (ROC). This should allow the readout of the four layer pixel system with considerable more pixel modules through the existing optical fibres for LHC luminosities up to 2x10^34 cm^-2 sec^-1 with minimal data loss. On one hand this implies the change from the present 40 MHz analog coded multilevel readout to a pure binary 320 MHz readout scheme, still providing an 8-bit digitized pixel pulse height. In addition, the internal ROC data buffering and readout scheme is changed in order to reduce the data losses associated with the readout token passage in the current pixel system. The changes to the digital readout architecture do not imply any changes to the well tested double column architecture and therefore present only a minimal risk of new rare error conditions of the readout chip under maximal data rates.
In order to test the new digital readout interface under realistic data flow conditions the electronic of a complete module has been tested with realistic input data from physics simulations based on PYTHIA and GEANT.
A detailed description of the ASIC modifications of the digital readout interface of the new CMS pixel ROC is presented as well as the results and the performance of the physics based electronic CAD simulations of complete pixel modules with 16 pixel ROCs and the token bit manager TBM.

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