Switched capacitor DC-DC converter ASICs for the upgraded LHC trackers

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This project has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under project SLHC-PP, Grant Agreement no 212114.

ACEOLE

Outline

1. **Powering schemes considered for upgraded ATLAS Inner Tracker**

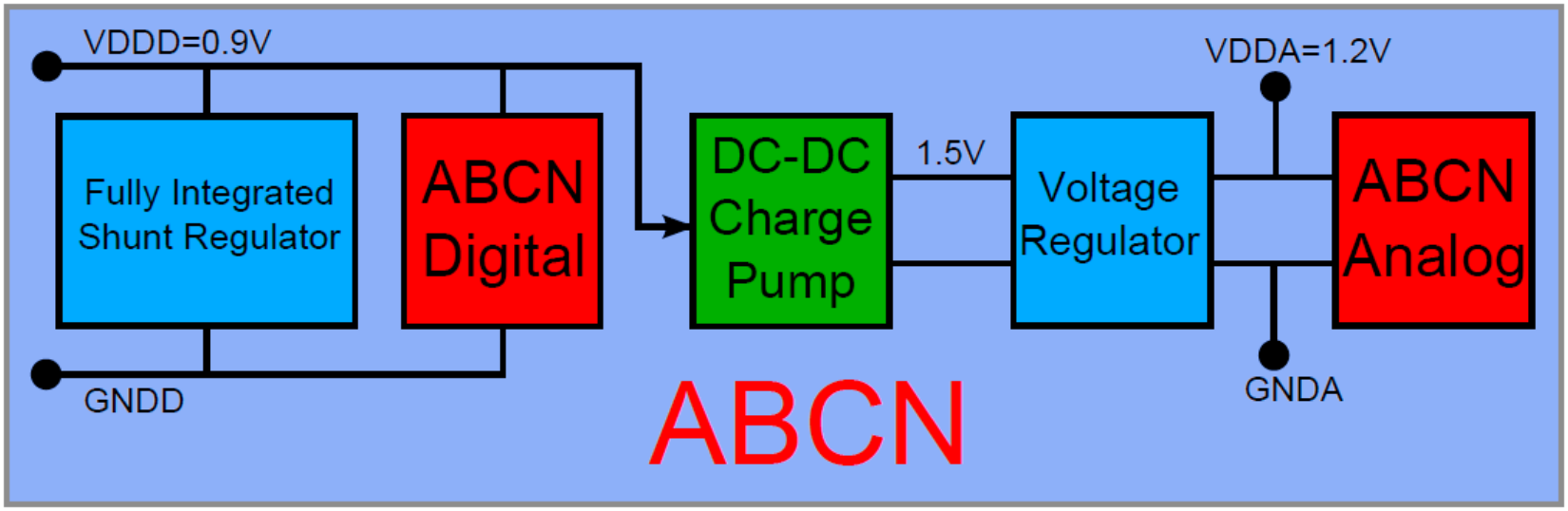
2. **Switched capacitor step-down converter proposed for the DC-DC powering scheme**
   - A model of a simple step-down (2:1) converter and its practical implementation,
   - Designs of the non-overlapping clock generator and buffers.

3. **Switched capacitor voltage doubler proposed for the serial powering scheme**
   - A model of a simple voltage doubler and its practical implementation,
   - Designs of the non-overlapping clock generator, level shifters and buffers.

Due to the fact that the IBM 0.13 µm submission was delayed, we have to wait for the results from the chips.

1. Overview of the powering schemes considered for the upgraded ATLAS Inner Tracker

Serial powering scheme

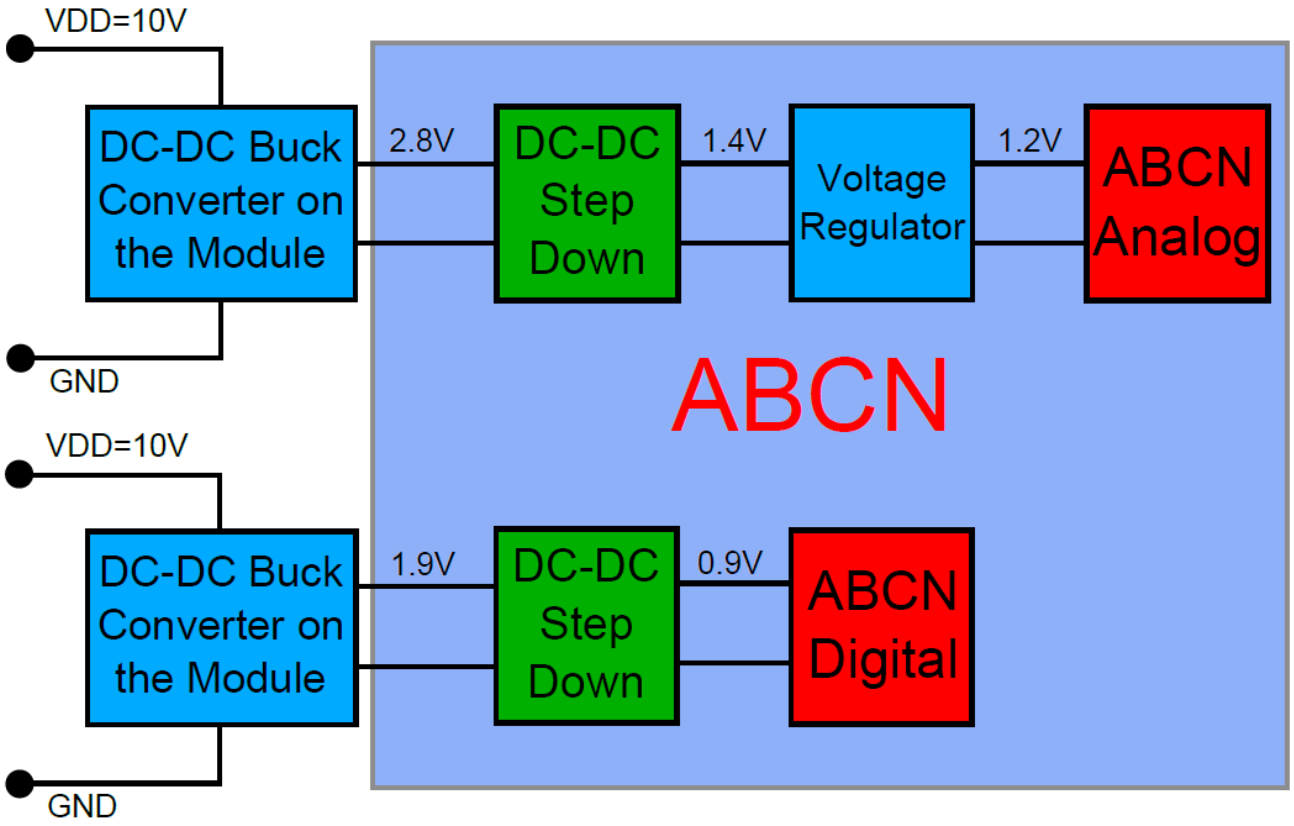


Good quality of analog and digital voltage:

- low output impedance of shunt regulator,
- possibility to use classical linear regulator → good filtering efficiency.

No regulation on DC-DC, but the power consumption in the analog part is constant.

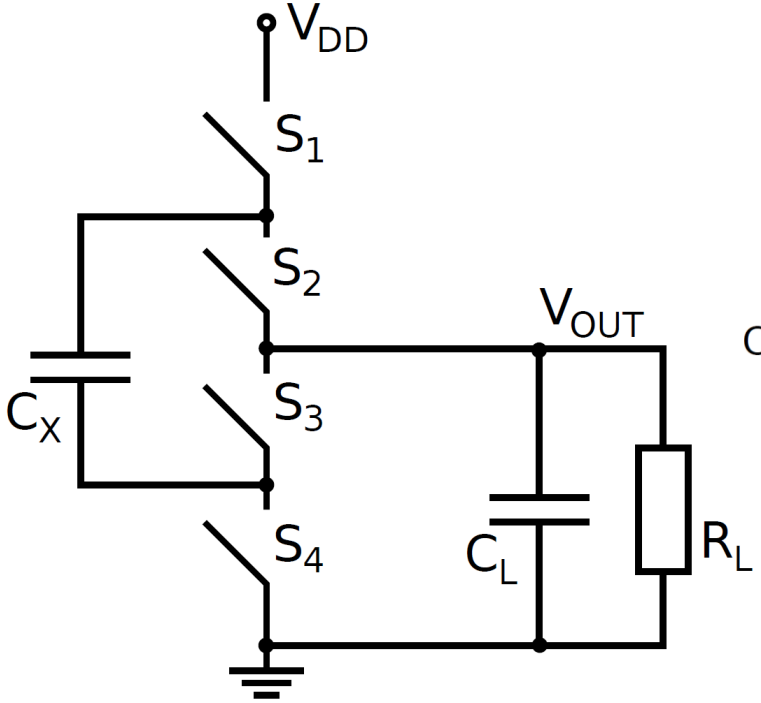
DC-DC conversion technique



- A low-dropout voltage regulator in the "analog bus" is required.
- No regulation on the digital power line
  (required low impedance of DC-DC since the current consumption varies significantly in the digital part).

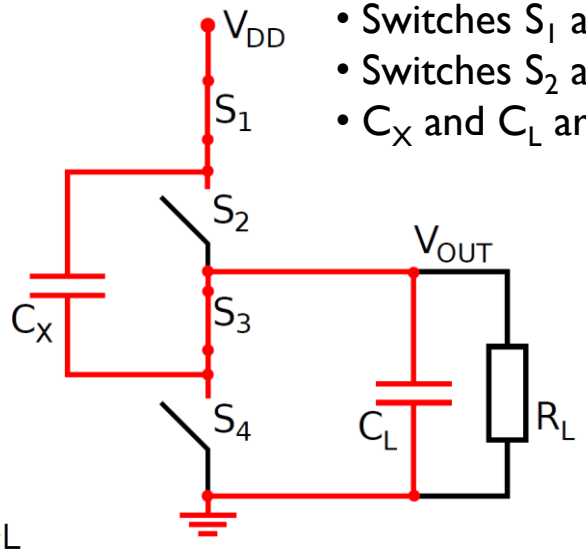
2. Switched capacitor step-down converter

A simple model of the step-down switched capacitor converter



Phase 1:

- Switches S_1 and S_3 are closed,
- Switches S_2 and S_4 are opened,
- C_X and C_L are connected in series.

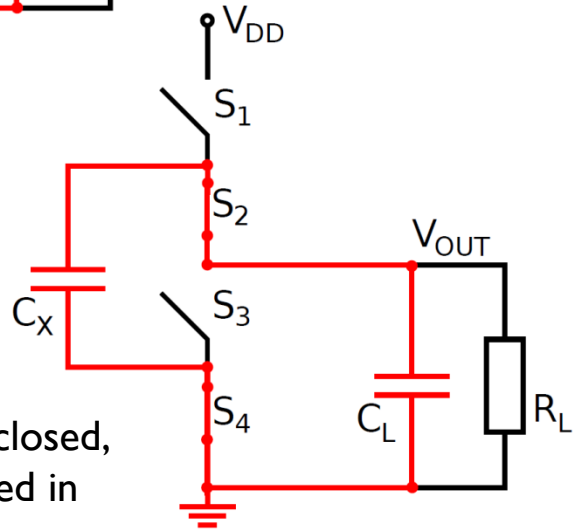


The simplest model for the 2:1 converter contains:

- **Four switches**
- **Two capacitors**

Phase 2:

- Switches S_1 and S_3 are opened,
- Switches S_2 and S_4 are closed,
- C_X and C_L are connected in parallel.



Types of losses in switching MOSFETs

The optimization process is based on minimizing the contradictory types of losses in the switching MOSFETs

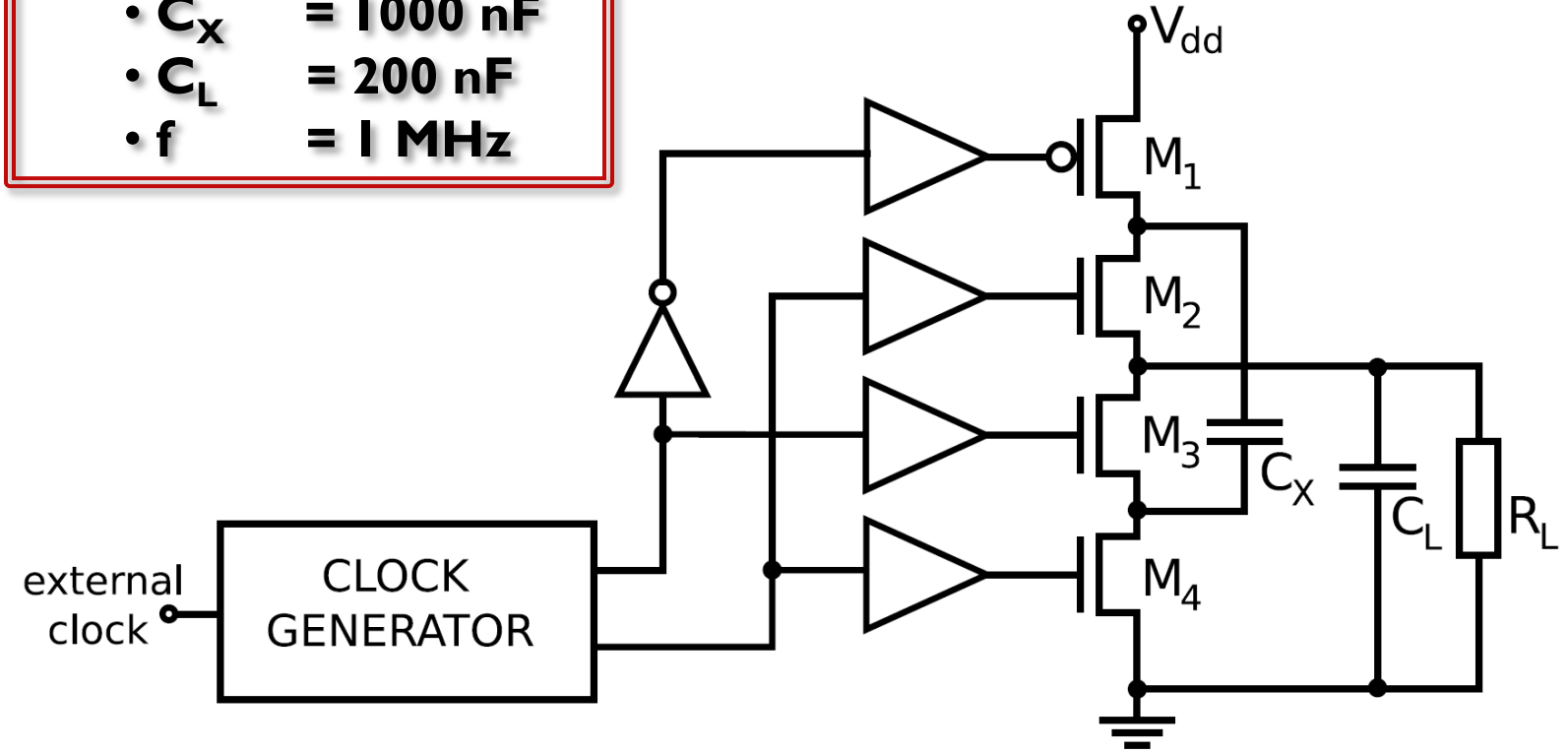
- **Conduction losses** (equal to: $\mathbf{I^2 \cdot R}$) – therefore the total resistance between the source and drain during the "ON" state, $R_{DS(on)}$ has to be as low as possible,
- **Switching losses** (equal to: $\mathbf{t_s \cdot V_{DS} \cdot I \cdot f}$) – switching time, rise and fall time depend on the gate to drain capacitance C_{GD}, internal resistance of the driver and the V_{TH},
- **Gate charge losses** (equal to: $\mathbf{f \cdot Q_{G(TOT)} \cdot V_{DRIVE}}$) – are caused by charging up the gate capacitance and then dumping the charge to ground every cycle.

Practical solution for the DC-DC step-down converter

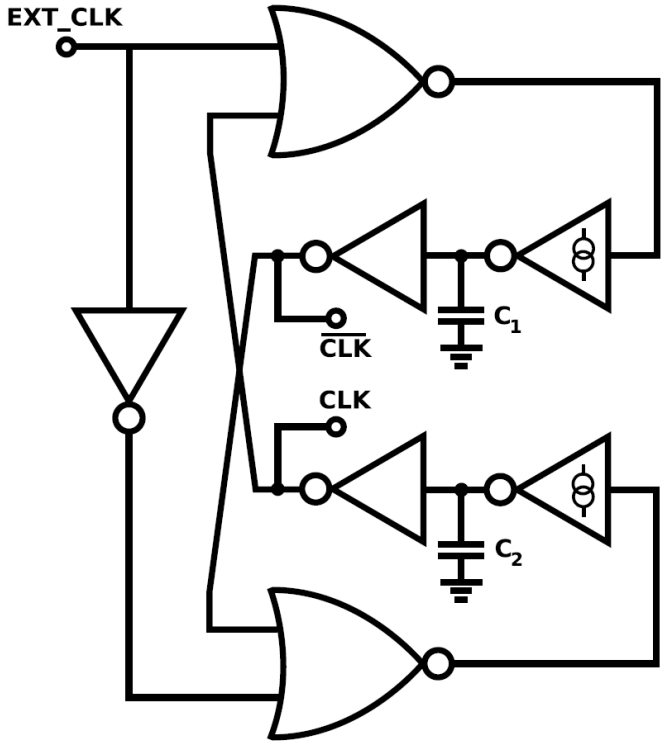
- V_{DD} = 1.9 V
- V_{OUT} = 926 mV
- I_{OUT} = 60 mA
- C_X = 1000 nF
- C_L = 200 nF
- f = 1 MHz

Power Efficiency = 97%

(including all circuitry)

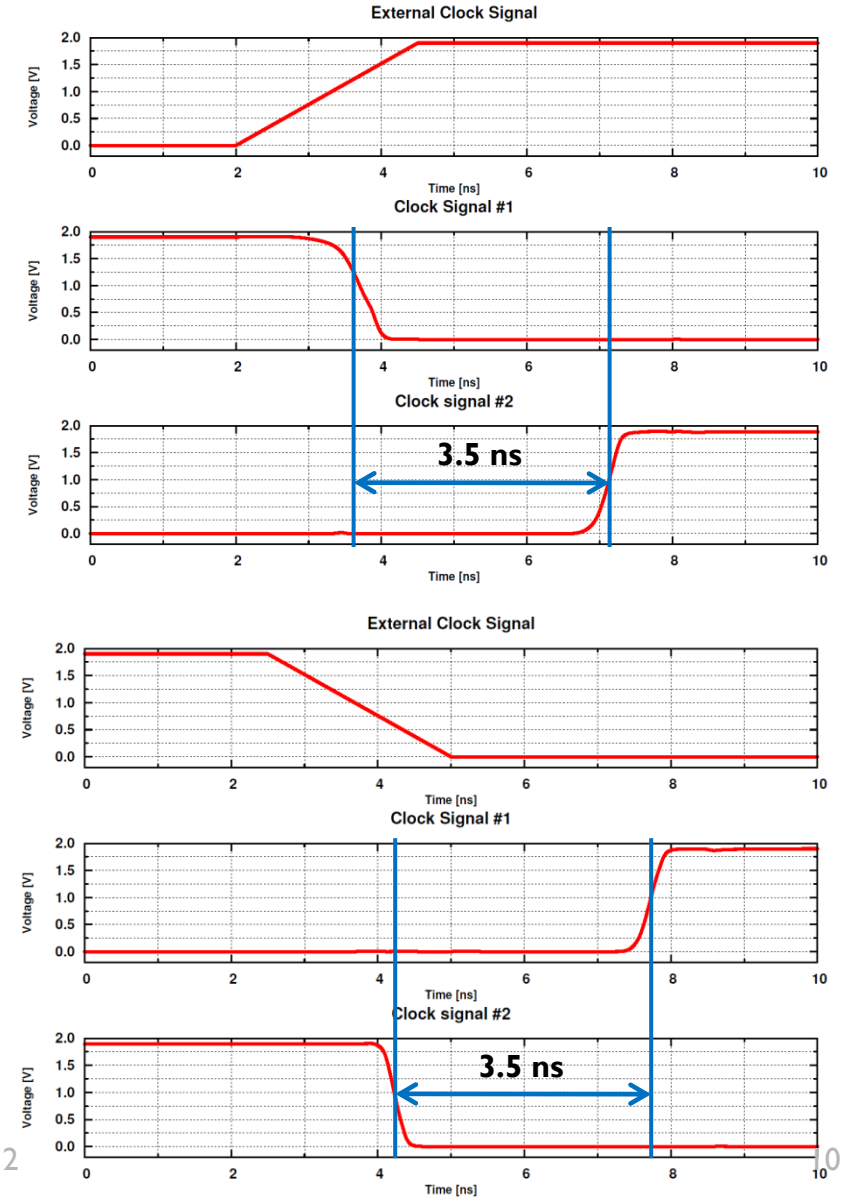


Schematic diagram of the non-overlapping clock generator used in the step-down converter

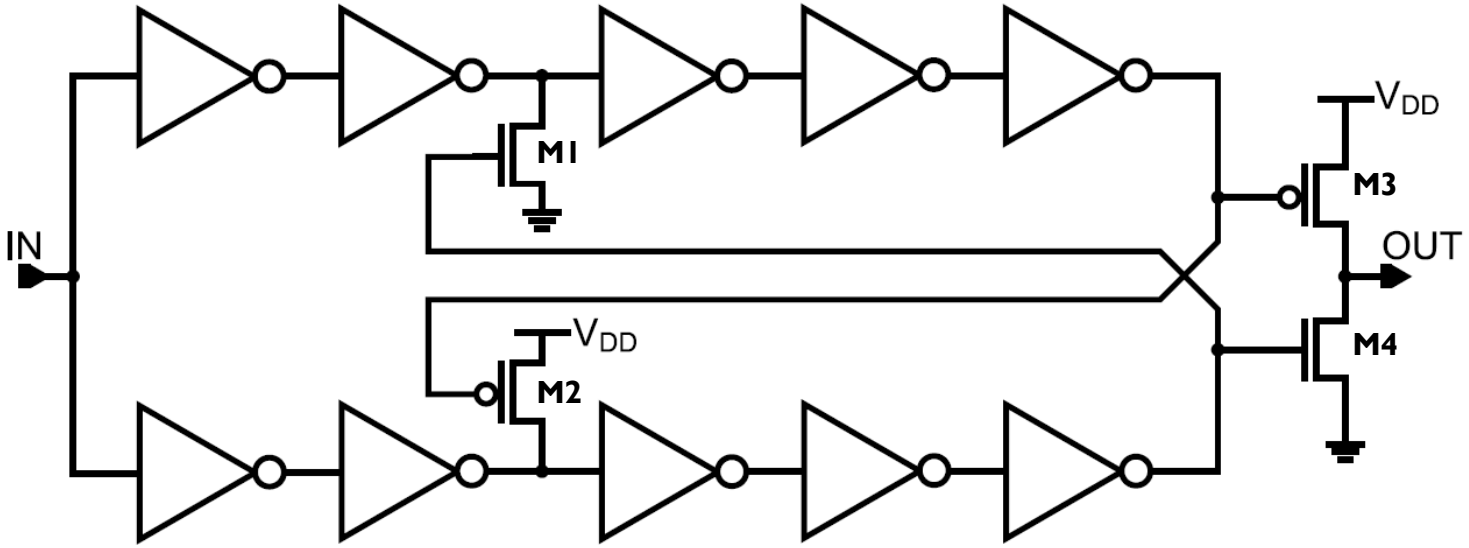


2 x NOR gate
3 x inverter
2 x current starved inverter
$C_1 = C_2 = 20$ fF

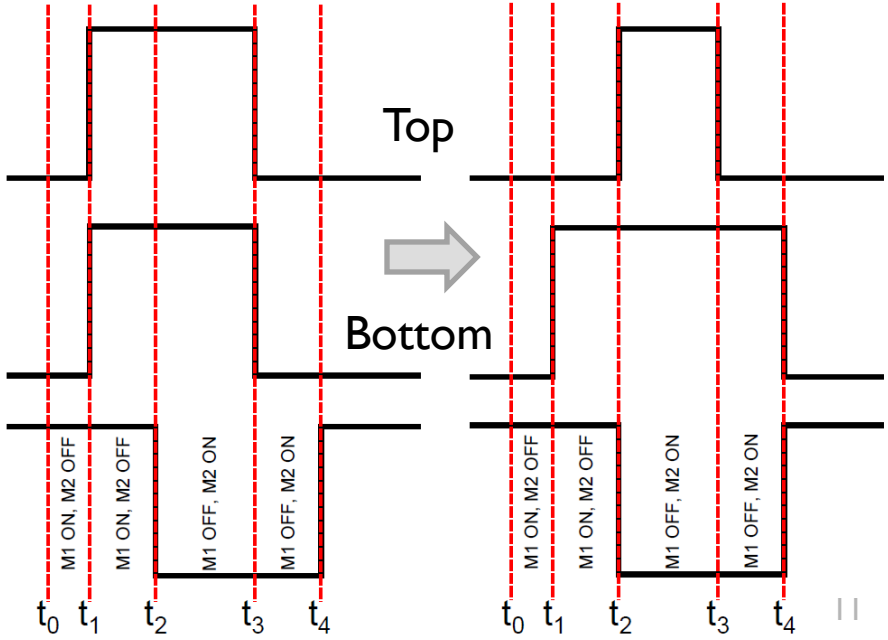
allows for a clock signal separation of 3.5ns



Buffer used in the step-down converter



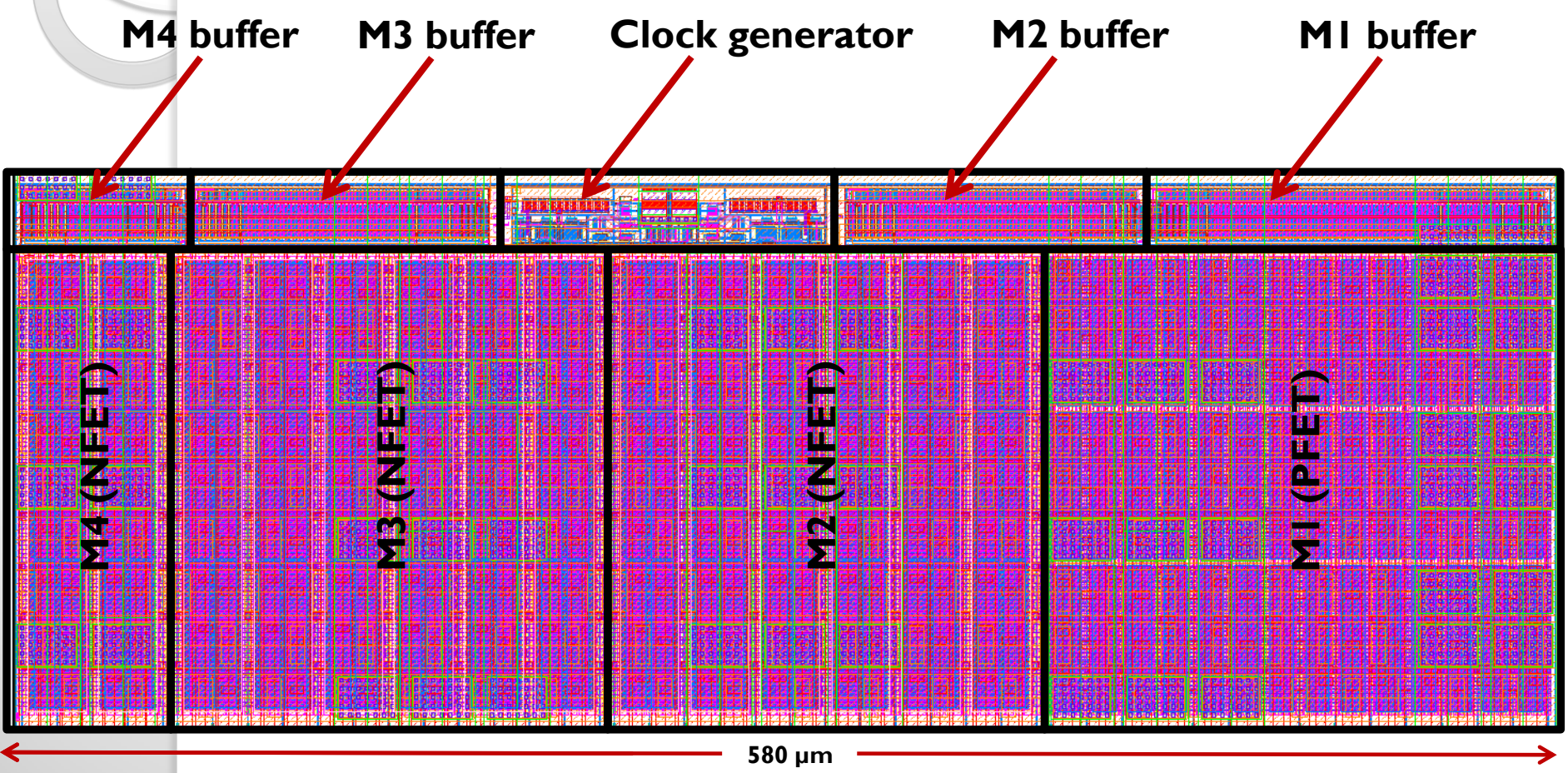
Two chains of scaled inverters with cross-coupled transistors M1 and M2 allow to avoid the conduction current in the last inverter M3 / M4



This architecture of the buffer was used by S. Michelis in AMIS2

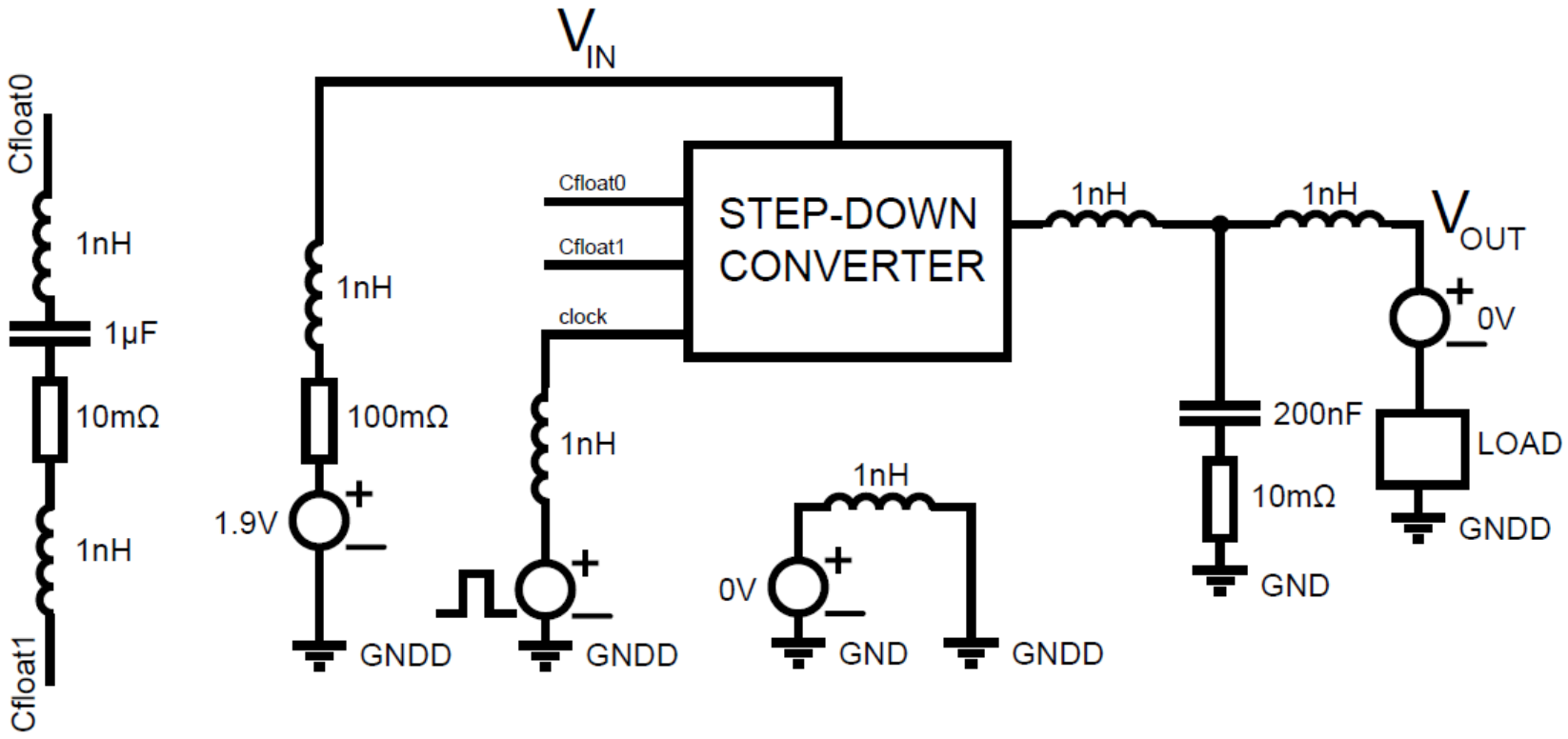
Layout of the step-down converter

M1 = 28.2 mm / 0.24 µm, M2 = M3 = 18.0 mm / 0.30 µm, M4 = 6.0 mm / 0.30 µm

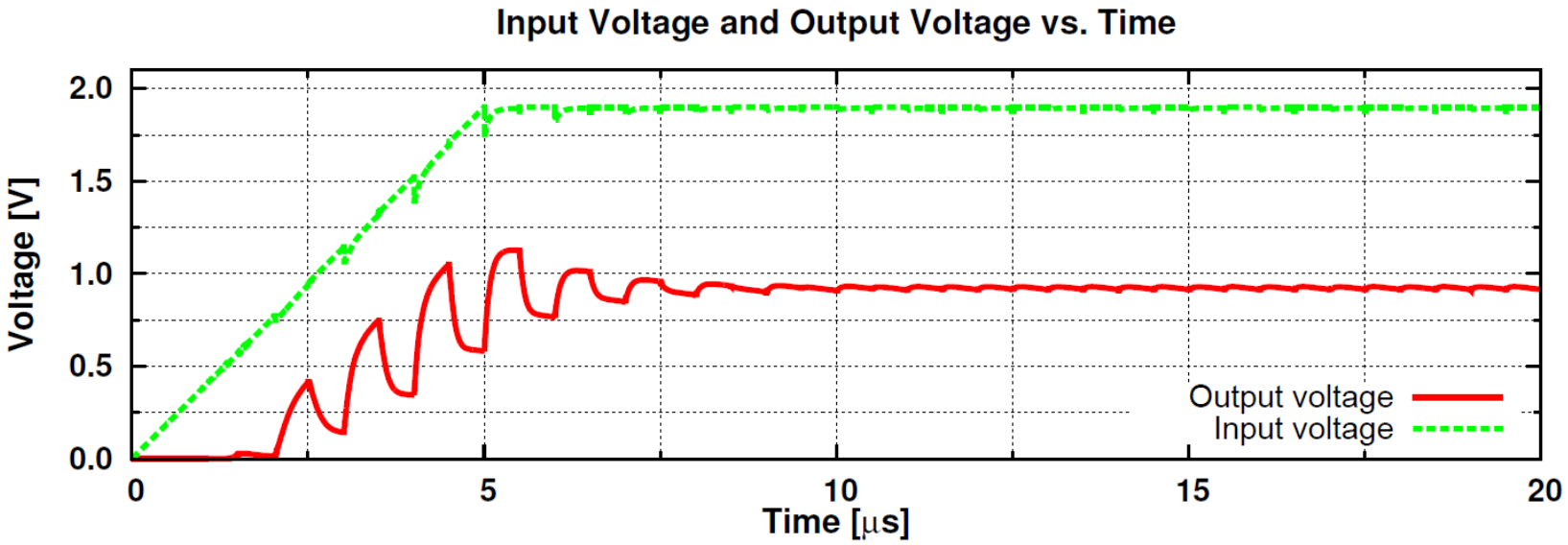


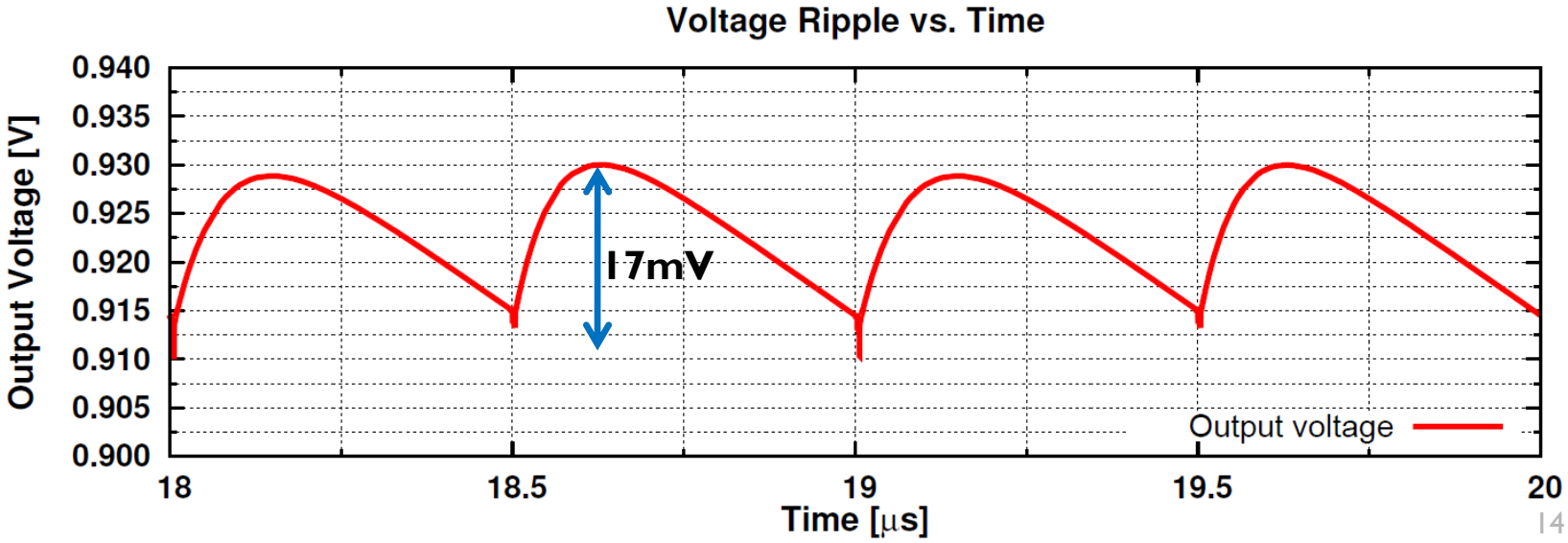
Total area = 0.12 mm^2

Simulation cell for the transient analysis (including package components)

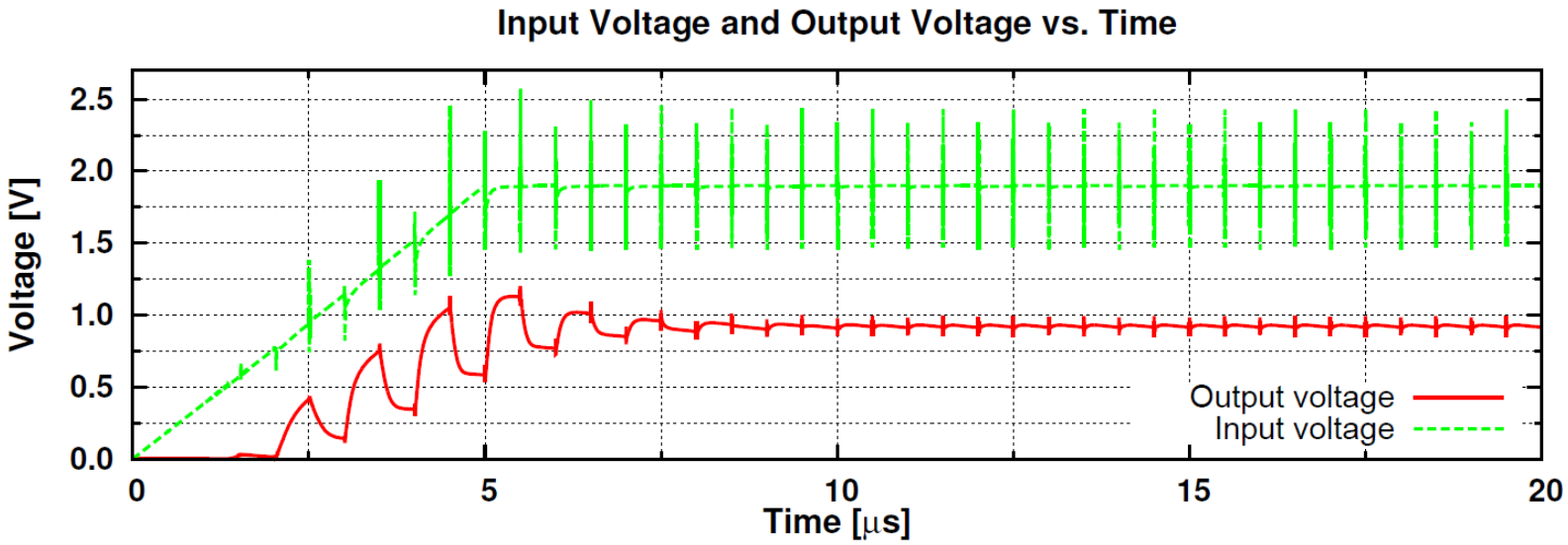


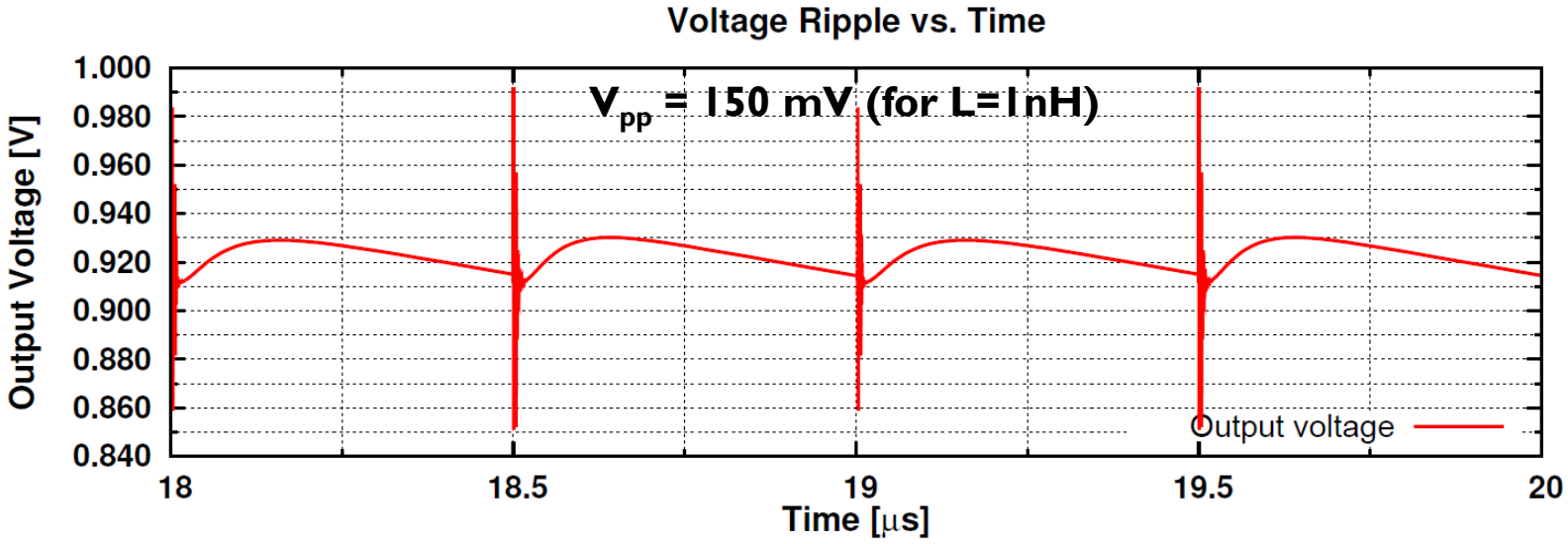
Time response of the step-down converter (no wire bonds)



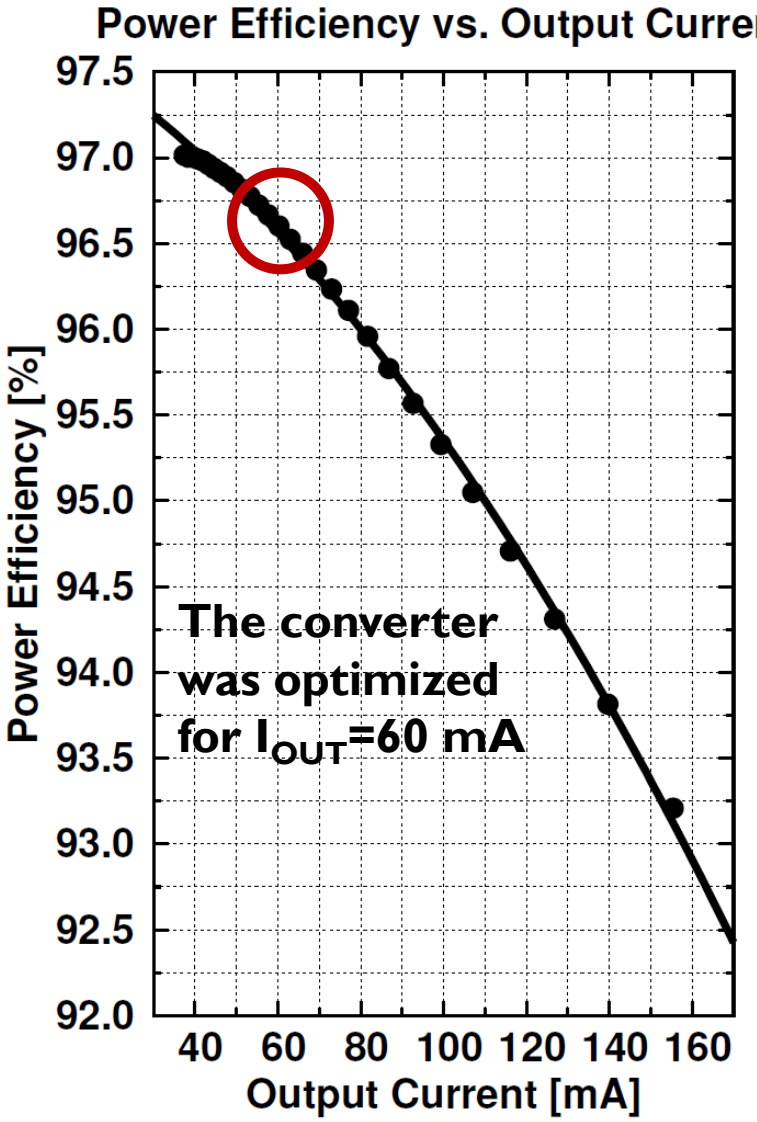


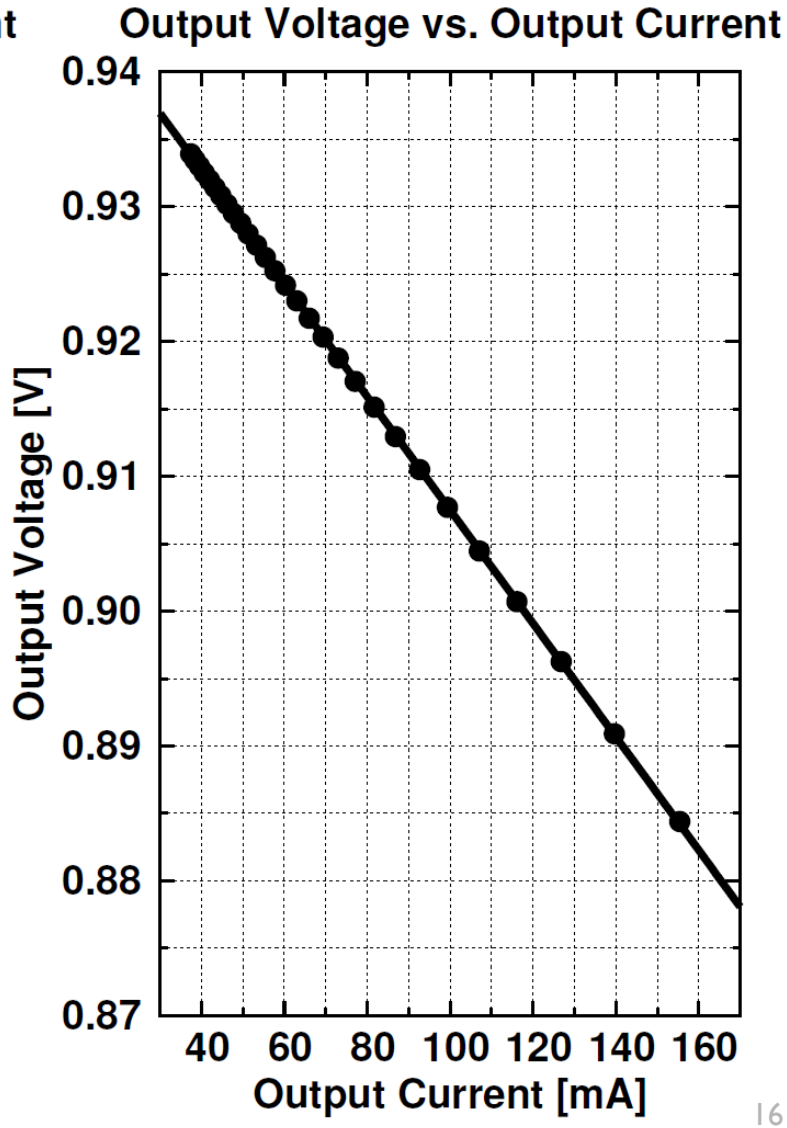
Time response of the step-down (wire bond inductance included)



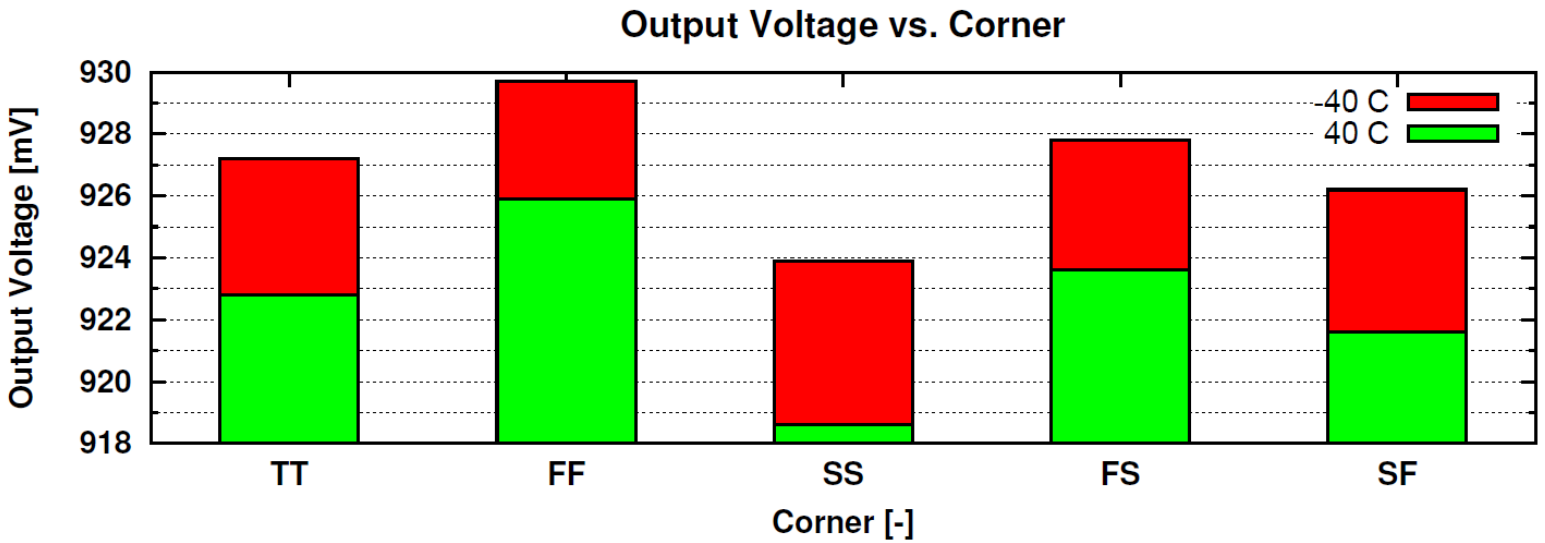


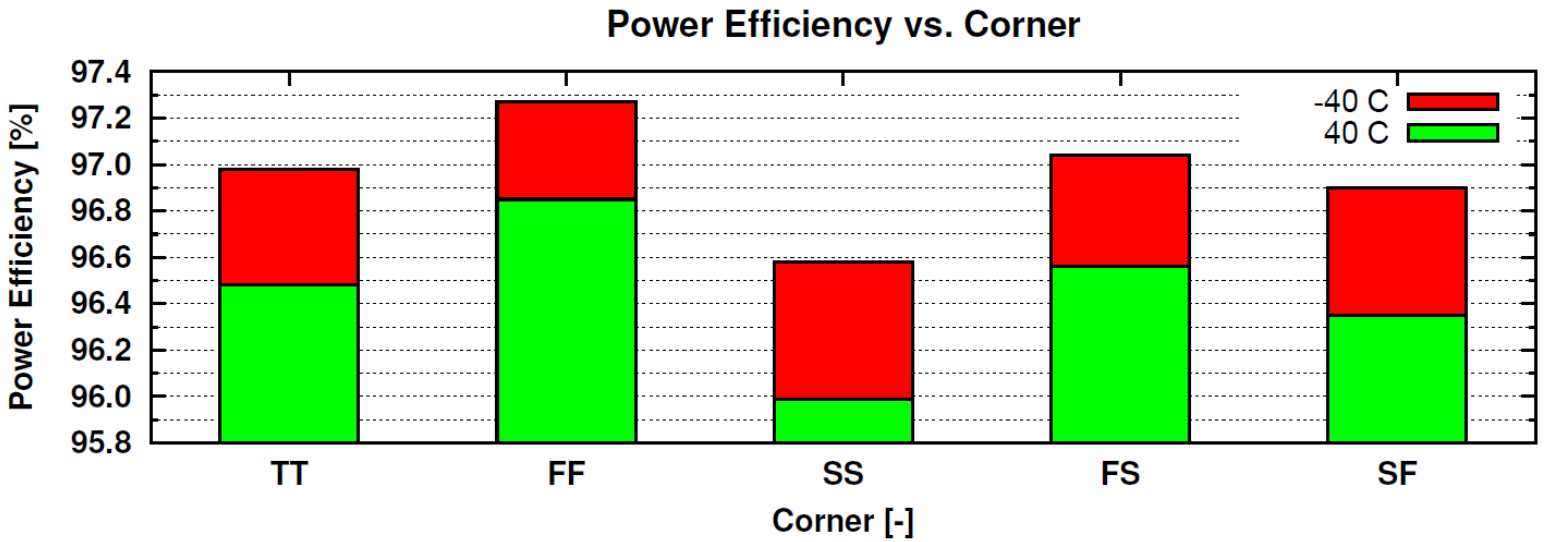
Power efficiency and output voltage vs. output current





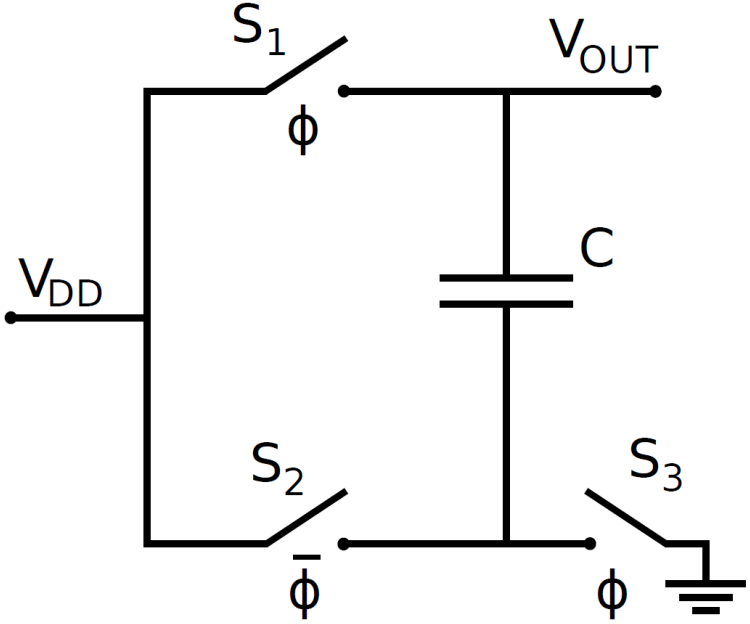
Results from the corner analysis





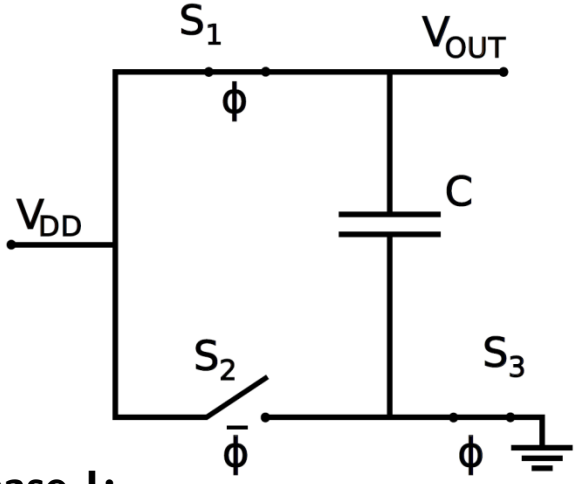
2. Switched capacitor step-up converter

A simple model of the step-up switched capacitor converter



A simple model contains:

- **Three switches**
- **One capacitor**

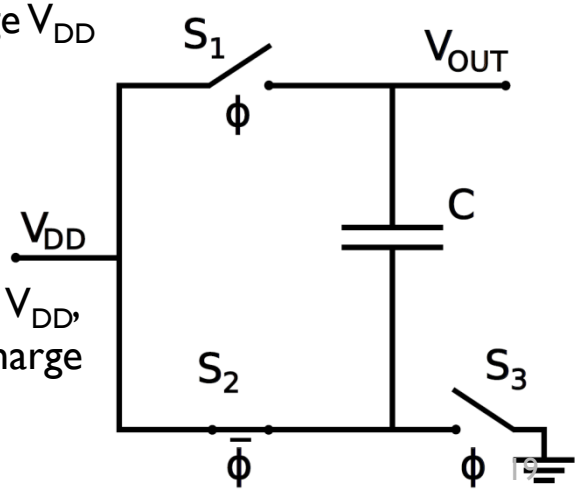


Phase 1:

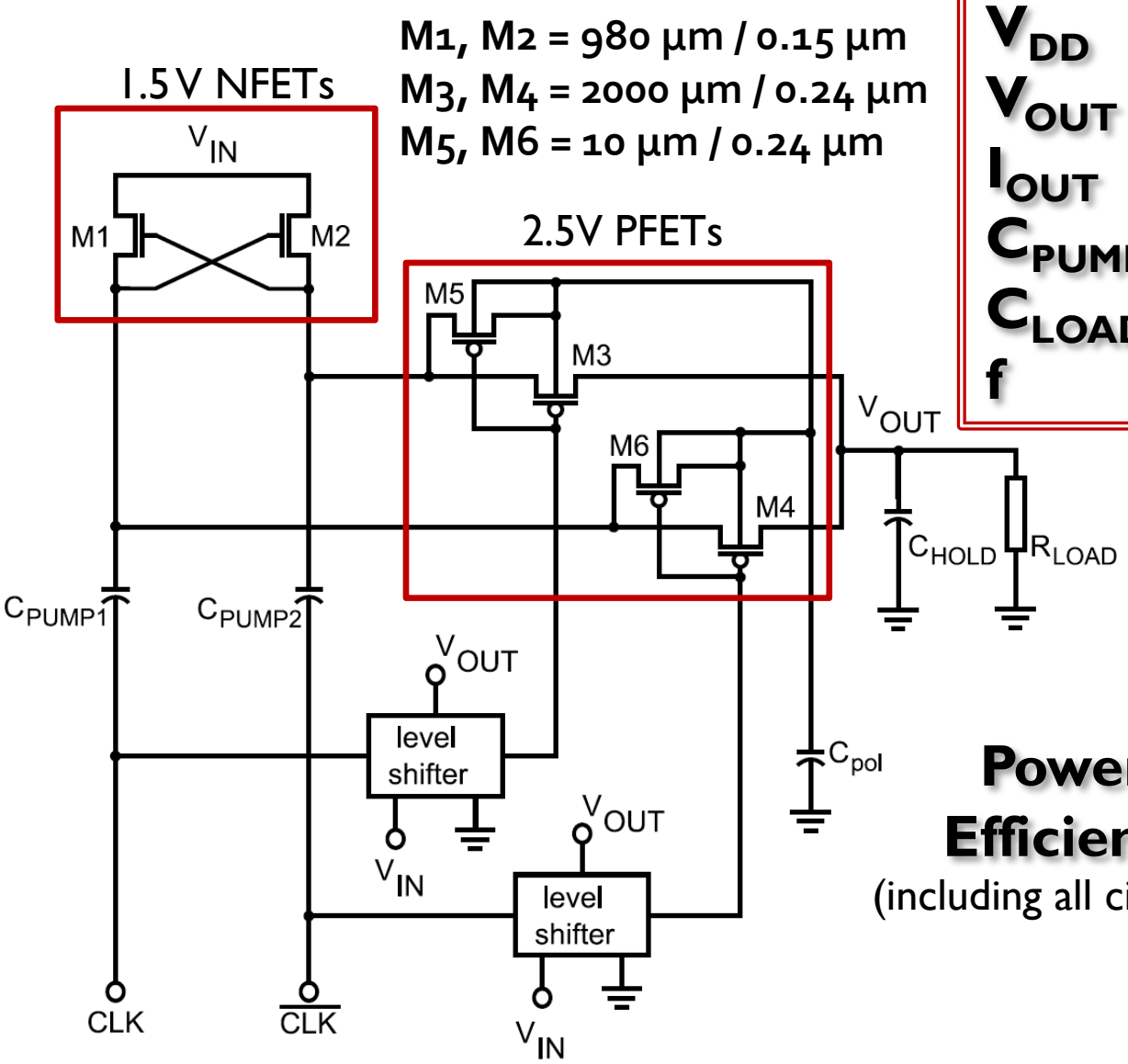
- Switches S_1 and S_3 are closed,
- Switch S_2 is opened,
- Capacitor is charged to the supply voltage V_{DD}

Phase 2:

- Switches S_1 and S_3 are opened,
- Switch S_2 is closed,
- Bottom plate of the capacitor on V_{DD}, while the capacitor maintains its charge $V_{DD}C$ (from the previous phase).



Practical solution for the voltage doubler

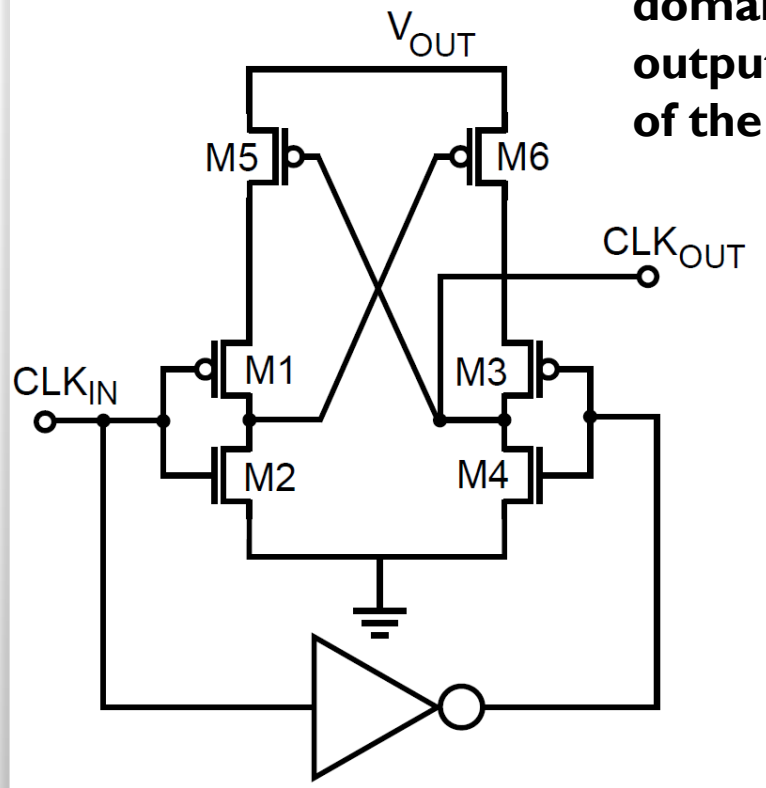


V_{DD}	= 0.9 V
V_{OUT}	= 1.55 V
I_{OUT}	= 32 mA
C_{PUMP}	= 470 nF
C_{LOAD}	= 470 nF
f	= 500 kHz

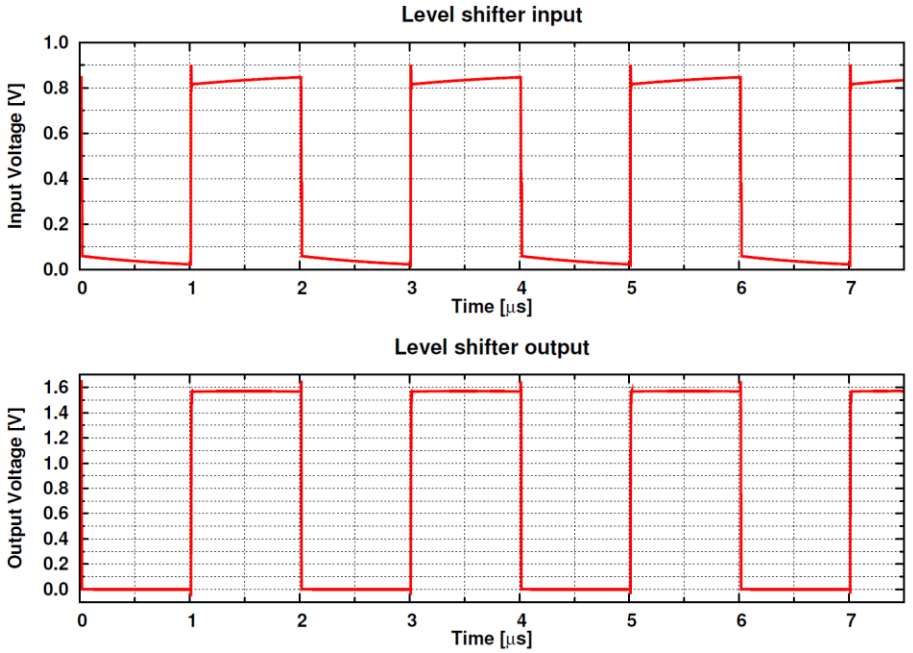
Power Efficiency = 85%
(including all circuitry)

Level shifter

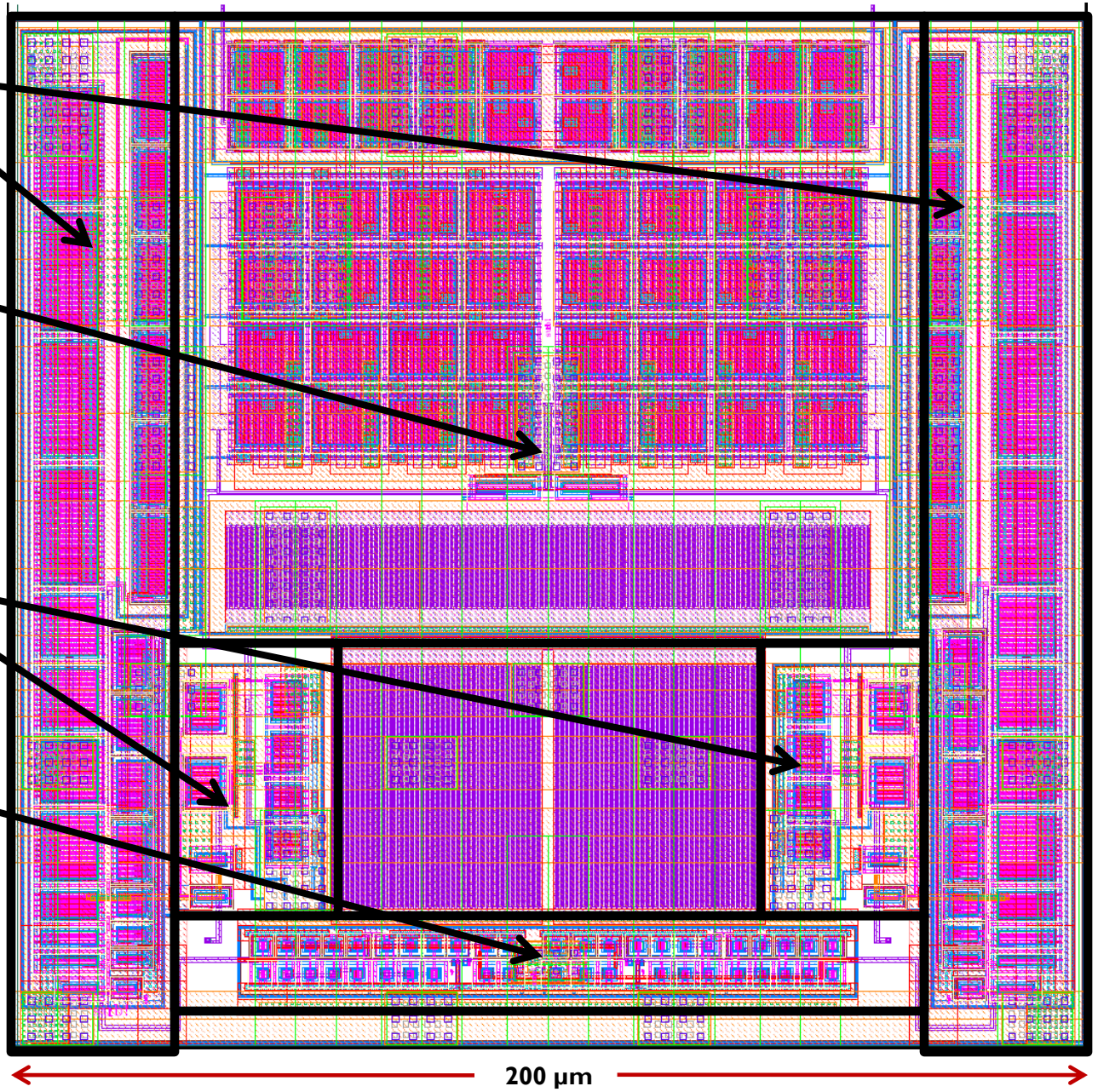
Because of poor driving capability of used big PMOS serial switches two level shifters are needed



The level shifter requires two voltage supply domains: input voltage supply (0.9 V) and output supply (1.6 V) - taken from the output of the charge pump

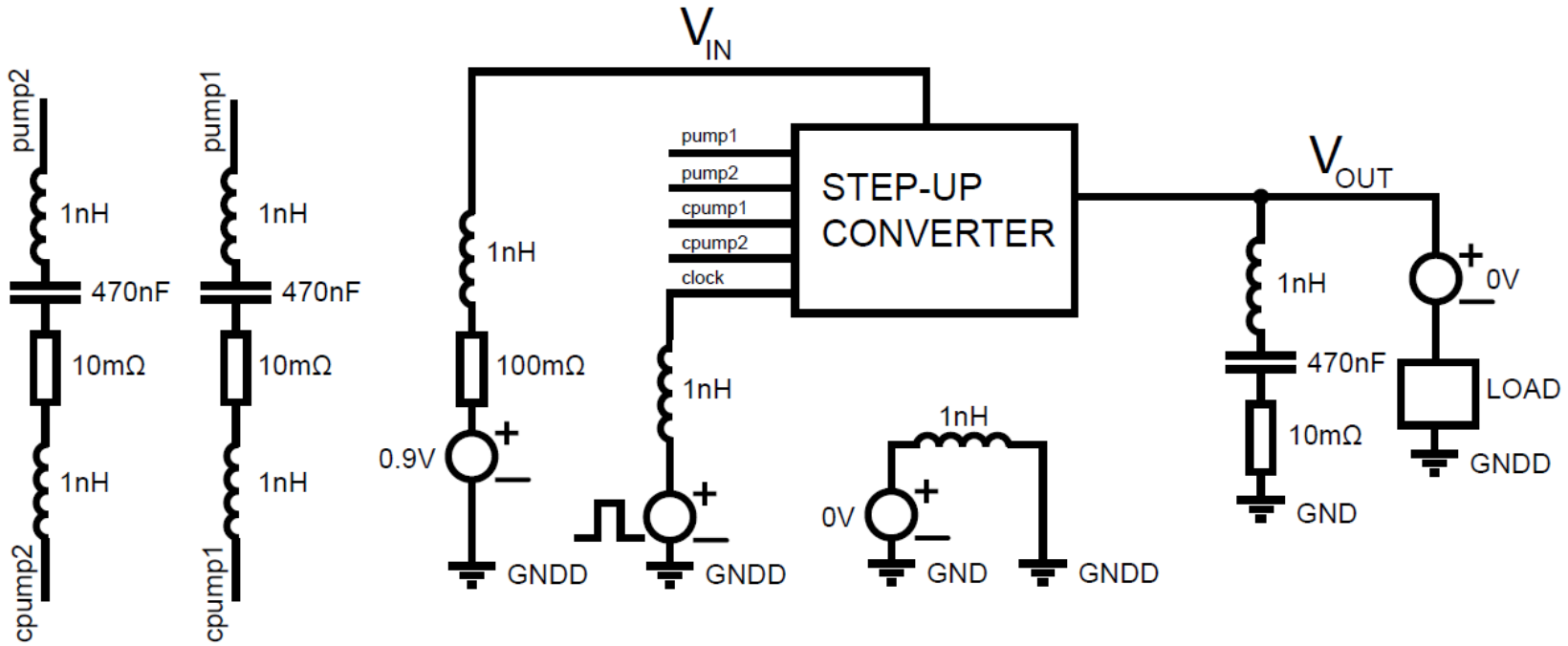


Layout of the charge pump

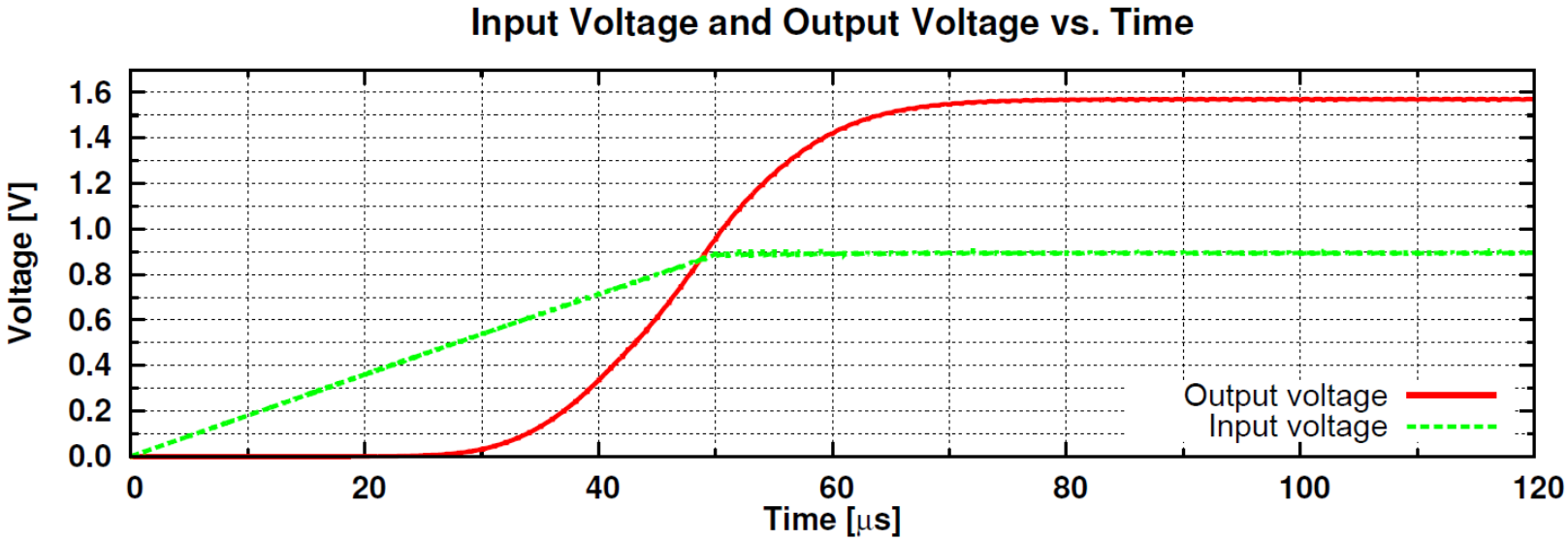


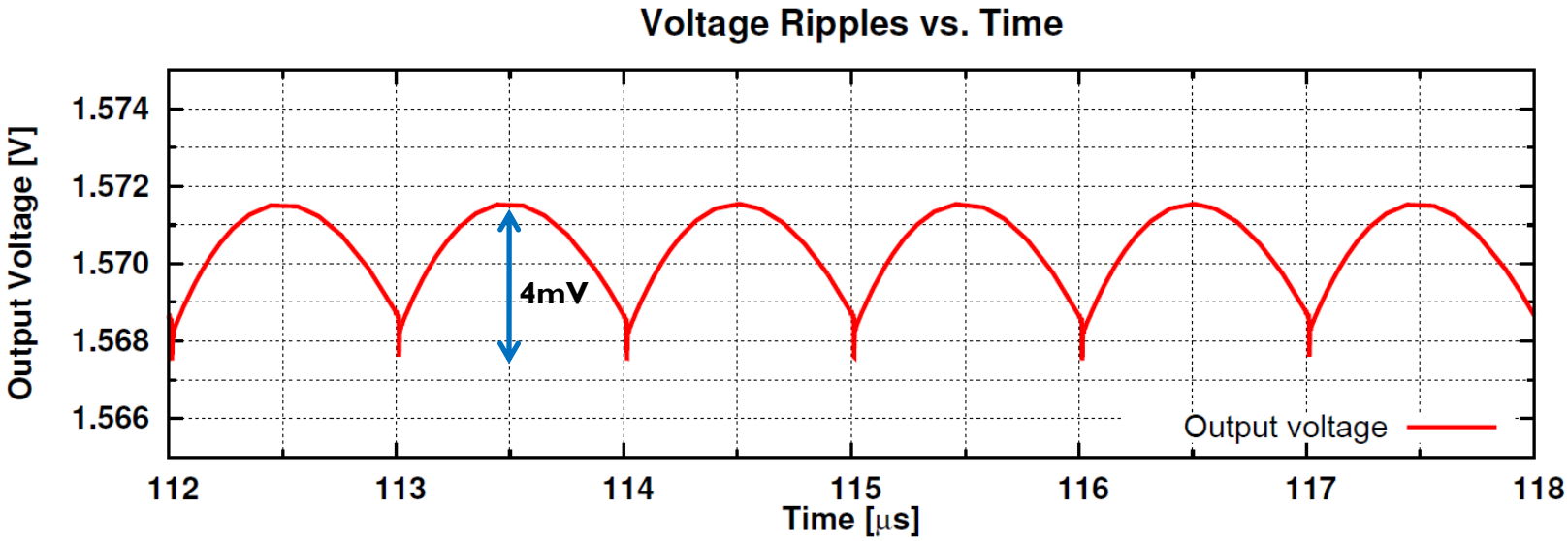
Total area = 0.04 mm²

Simulation cell for the transient analysis (including package components)

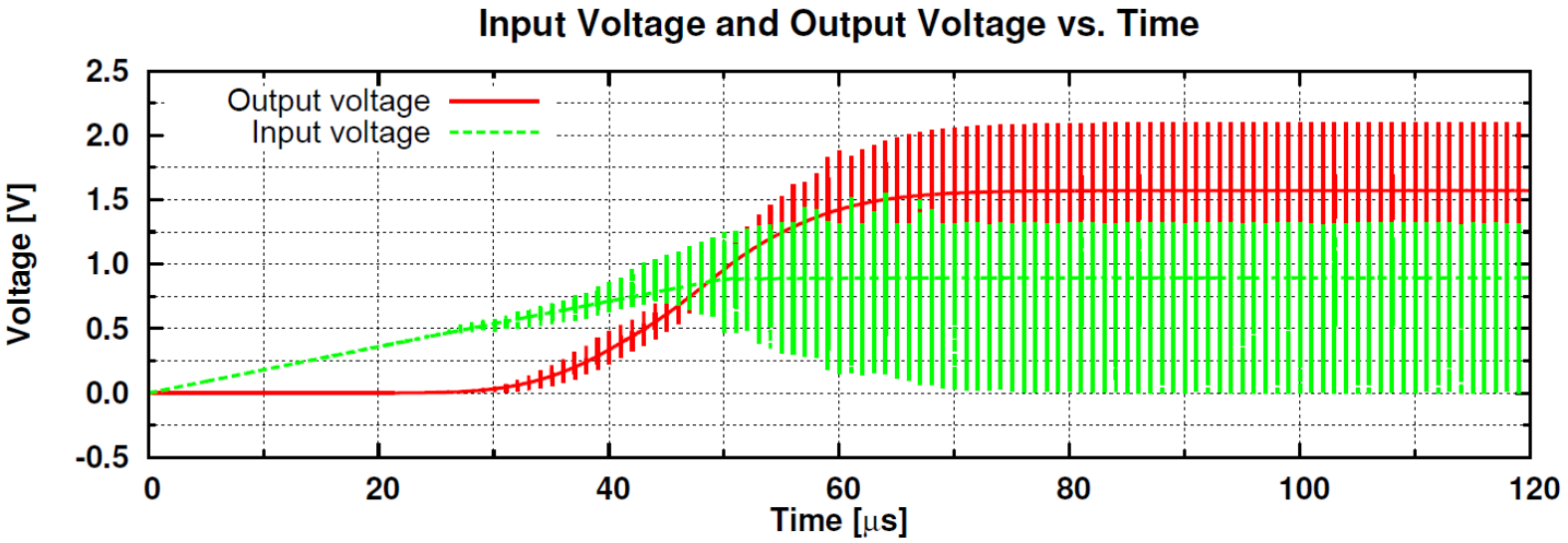


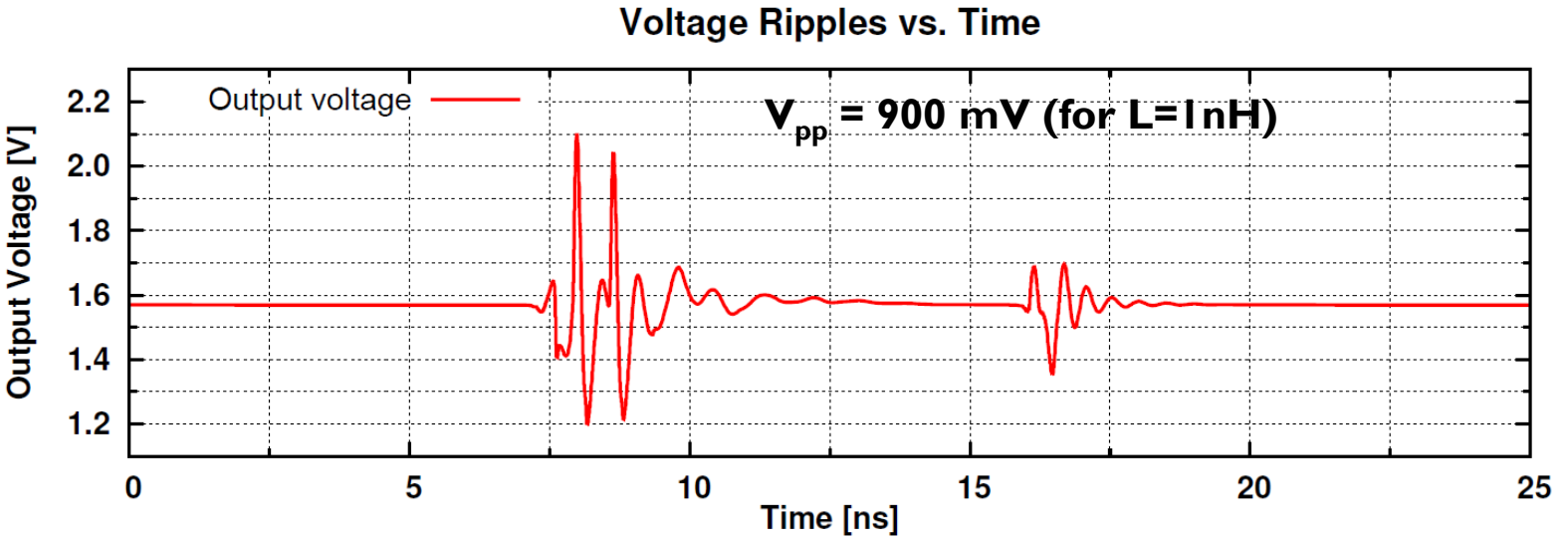
Time response of the step-up converter (no wire bonds)



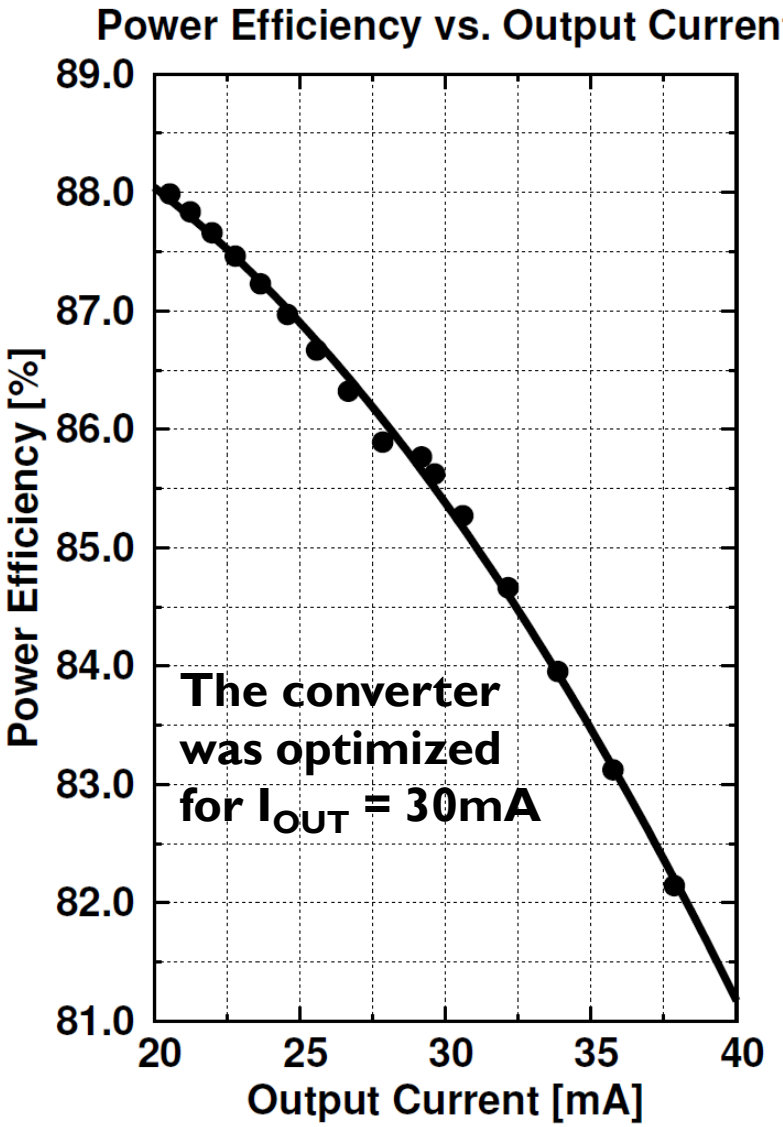


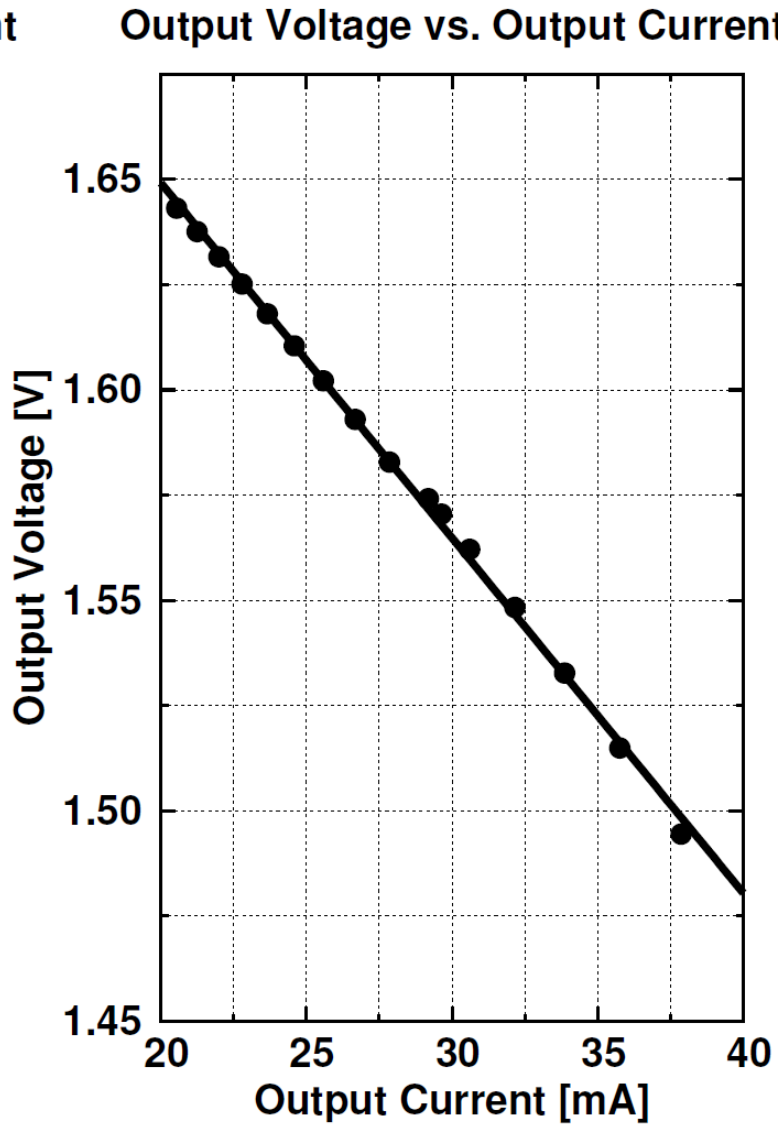
Time response of the step-up (wire bond inductance included)



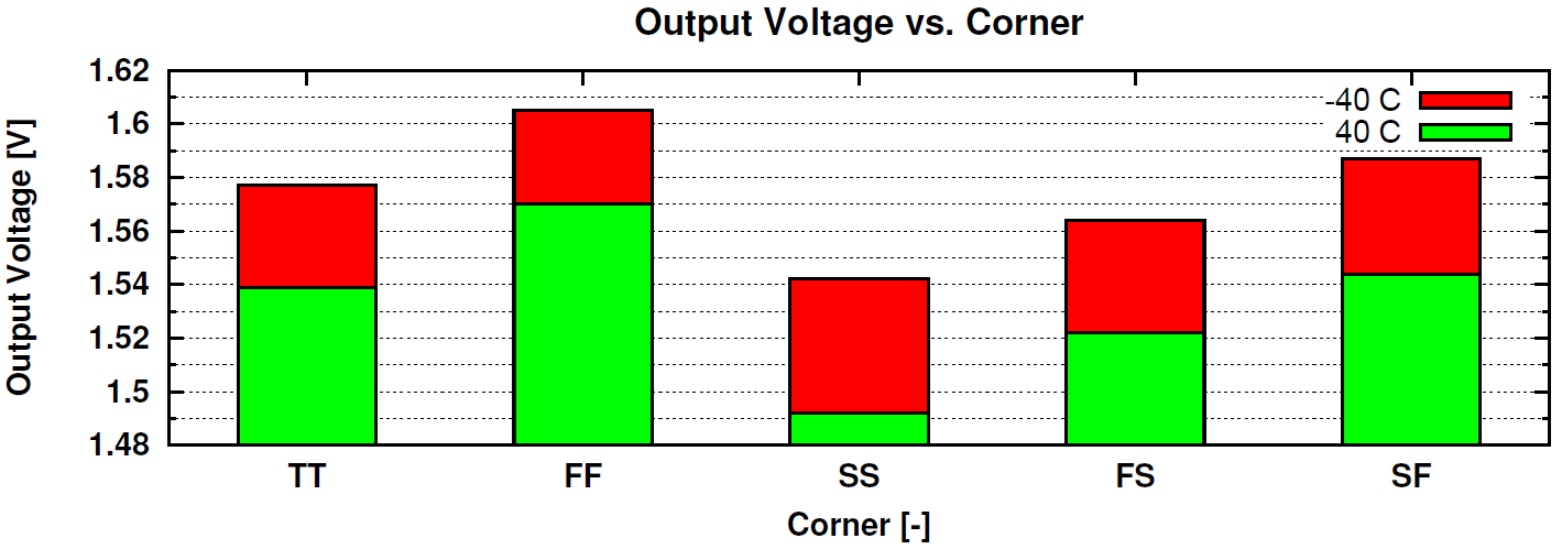


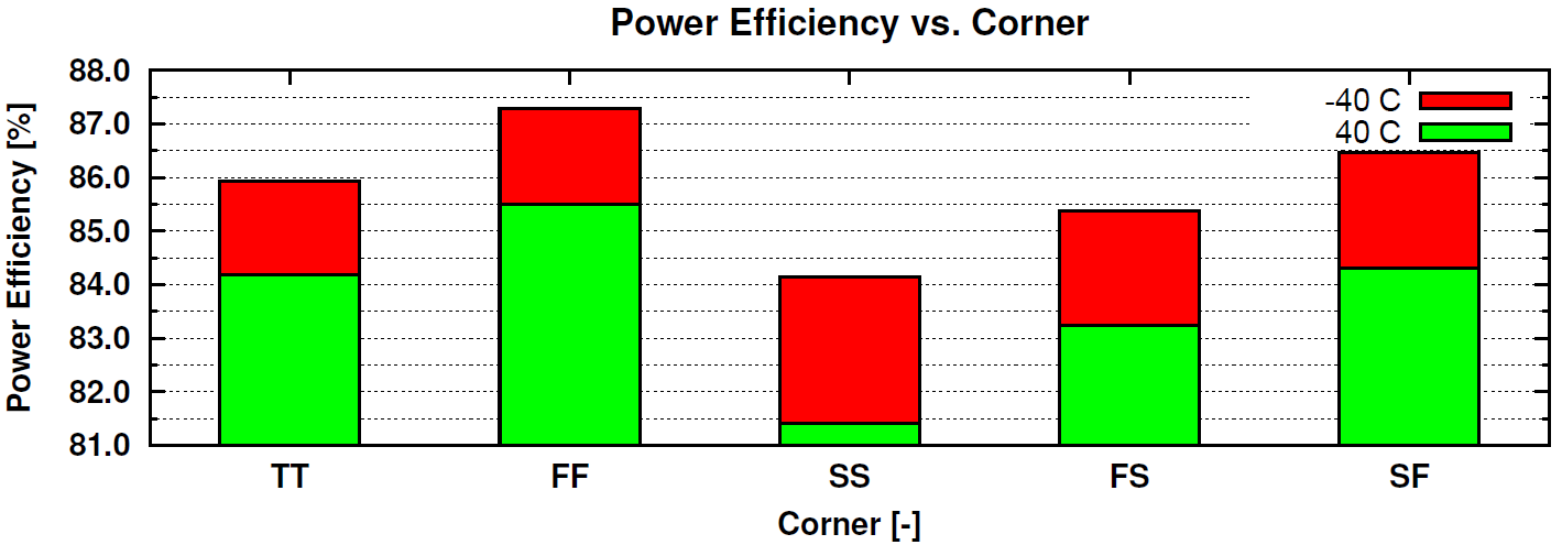
Power efficiency and output voltage vs. output current



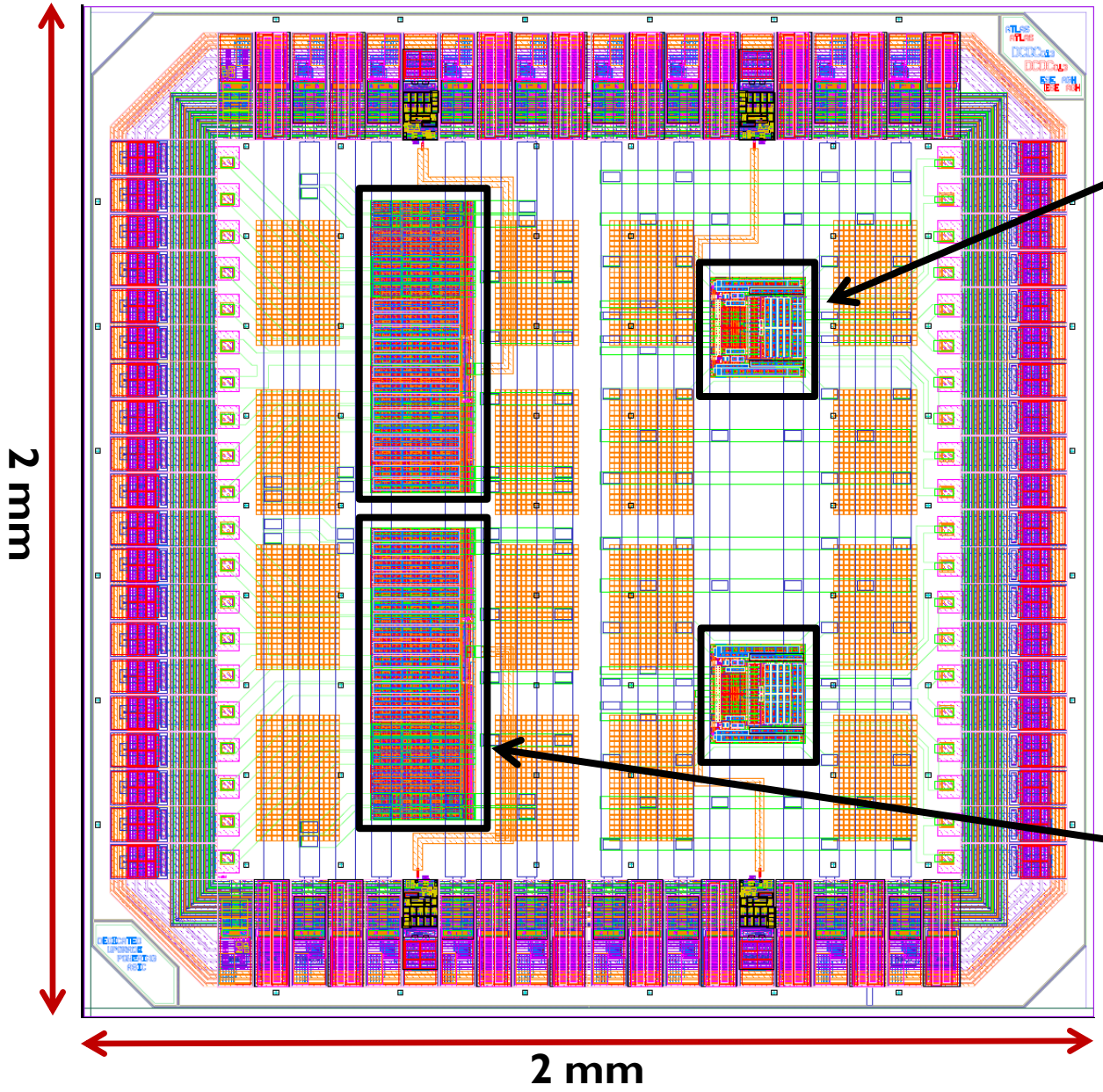


Results from the corner analysis





Layout of the DCDC013



Conclusions

- The results from the Spectre simulations are quite promising:
  - η = 97% for the step-down converter,
  - η = 85% for the step-up converter.

- The inductance of the bond wires causes fast voltage spikes – the padring was designed to reduce the influence of the bond wire inductance.

  Therefore, the use of the DC-DC converters mounted on the **separate chip** with **C4 pads** should be considered.

- The chip was submitted at the end of August 2010.

- The PCB board is now in production and will be ready before the arrival of the chips.

Thank you!

This research project has been supported by a Marie Curie Initial Training Network Fellowship of the European Community's & Seventh Framework Programme under contract number (PITN-GA-2008-211801-ACEOLE)

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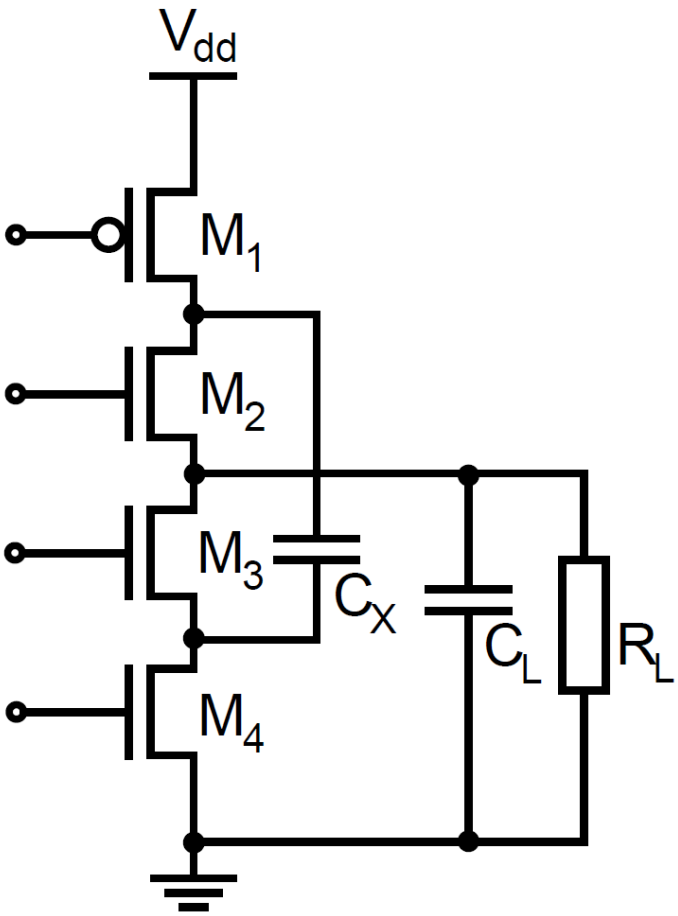
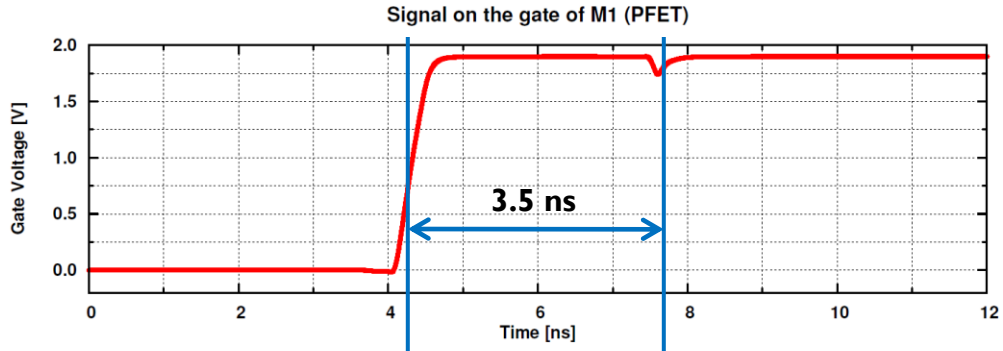
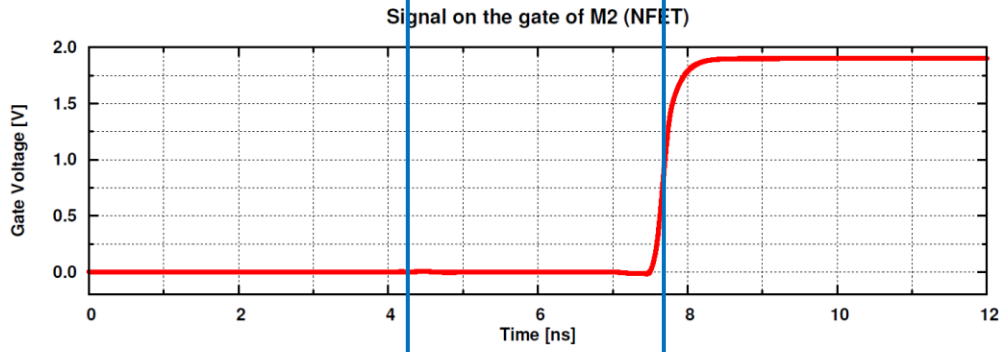
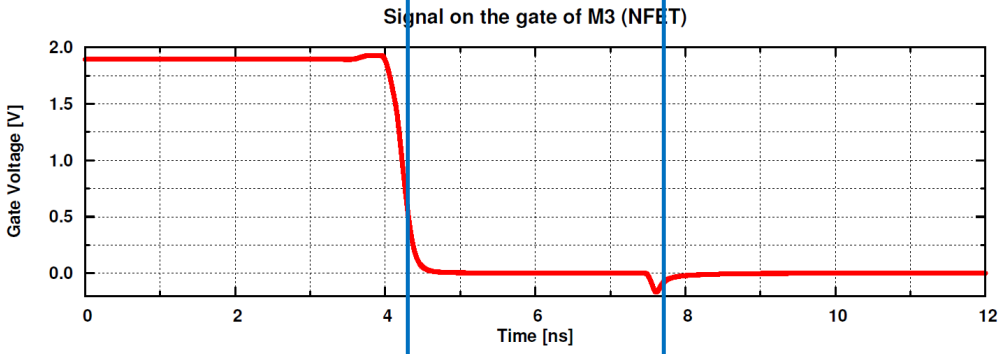
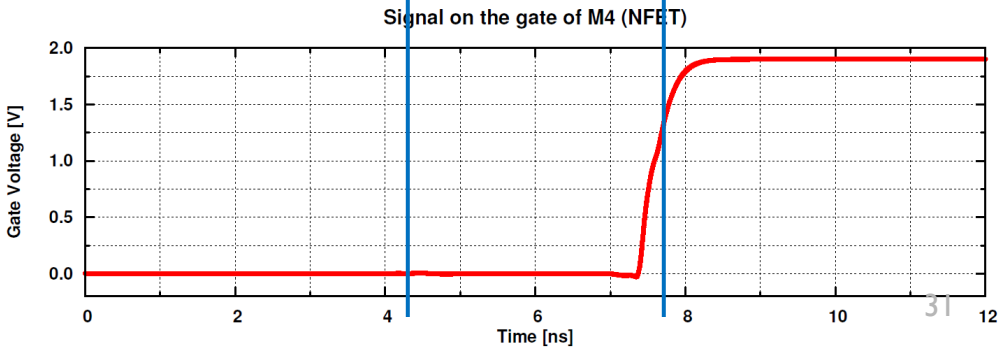
Backup


Vdd
M1
M2
M3
M4
Cx
CL
RL


Signal on the gate of M1 (PFET)
Gate Voltage [V]
Time [ns]
3.5 ns


Signal on the gate of M2 (NFET)
Gate Voltage [V]
Time [ns]


Signal on the gate of M3 (NFET)
Gate Voltage [V]
Time [ns]


Signal on the gate of M4 (NFET)
Gate Voltage [V]
Time [ns]