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Switched capacitor DC-DC converter ASICs for the upgraded LHC trackers

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We present designs and hopefully the first test results of two DC-DC switched capacitor converters developed in 0.13µm technology. Both circuits will be used as the building blocks in the power distribution system proposed for the upgraded ATLAS Inner Detector.

Summary

After the LHC luminosity upgrade, the number of the readout channels in the ATLAS Inner Detector will be increased by one order of magnitude. Due to that fact, delivering power to the front-end electronics will become a critical issue. Therefore, two new approaches for power distribution; serial powering of the chain of modules and parallel powering using DC-DC converters integrated on the module, are now under development. Both schemes being developed assume the use of the switched capacitor DC-DC converters integrated on the front-end chips.

In this paper we present two designs of DC-DC converters in 130 nm CMOS process from IBM; a charge pump based on the voltage doubler concept and a step-down converter.
The step-up converter consists of four main building blocks: clock generator, buffers, level shifters and the voltage doubler itself. The core of the voltage doubler is built of four switches and three external SMD capacitors. The 470 nF capacitors were chosen as a compromise between large capacitance and small SMD package size. To further improve the power efficiency, an auxiliary charge pump was added, which delivers local supply voltage used for biasing the n-wells of the serial switches, to eliminate the parasitic bipolar structures. Due to the fact that it has a capacitive load only, this additional pump can generate a voltage in the range of a few tens of mV higher than the voltage obtained from the output of the main doubler.

The main part of the whole step-up converter is supplied from with 0.9 V. The level shifters are supplied from two power domains (0.9 V and 1.6 V taken from the output) . The nominal output current is specified to be around 30 mA. The calculated power efficiency is in the range of 85% for an optimized clock frequency of 500 kHz. The peak-to-peak value of the voltage ripples seen on the output of the charge pump is less than 15 mV.

The second presented design is the step-down converter. The circuit comprises three main sub-circuits: clock generator, buffers and the core which is built of four stacked transistors (three N-channel FETs and one P-channel FET) and two low-ESR, SMD capacitors. The level shifters are not needed in this case, because the circuit is supplied from 1.9 V. To further improve power efficiency, an optimized new clock buffer architecture is used. This helps to eliminate the cross conduction current flowing through the converter while switching.

The circuit is supplied with 1.9 V. The nominal output current was specified to be around 60mA. The output voltage is around 920 mV. The calculated power efficiency obtained for the optimized switching frequency is 1MHz and for the load current of 60 mA, is up to 96%. The output impedance of the converter is less than 0.5 W. The peak-to-peak value of the output ripples is less than 20 mV.

A chip comprising both prototype circuits has been submitted for an MPW run at IBM. In the paper we will present details of design optimization and hopefully first test results of the prototype chip.

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