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An FPGA based back up version of the TileCal digitizer.

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The ATLAS TileCalorimeter contains some 2000 digitizer boards with 2 TileDMU ASICs on each board. Although we have the agreed number of spares this paper discusses a backup version of the digitizer to be used in case more units are required. The TileDMU has been replaced with a cheap and readily available FPGA (Spartan 6) and we have replaced some components to protect against obsolescence. The focus is on achieving sufficient FPGA radiation tolerance using triple mode redundancy and scrubbing. We have also implemented in system programmability (JTAG) via the TTCrx.

Summary

The ATLAS TileCalorimeter contains some 2000 digitizer boards with 2 TileDMU ASICs on each board. The TileDMUs are responsible for all digital operations on the board except for those taken care of by the TTCrx. We have the agreed number of board and component spares. However, in the unlikely case that we run out spares anyway or if a catastrophic failure occurs due to some unforeseen event it would help to have a backup solution. This paper discusses a backup version of the digitizer. The original version contains both outdated and custom made circuits which are difficult or impossible to find in sufficient numbers. This version have updated components and a cheap off the shelf FPGA (Spartan 6) instead of the ASIC. The FPGA have all the functionality of the TileDMU but will be readily available for a considerable time. It is functionally compatible with the current version and to a large extent uses the same code. The general idea is to leave the digitizer design as intact as possible since it is well tested and well performing. However, we have added some new features on the board that were easy to implement in the FPGA such as voltage monitoring and in system programmability. The ISP is done via TTCrx for both the FPGA and the configuration memory using one way JTAG. This provides a way to recover from radiation damage in the PROM.

The main focus has been to ensure sufficient radiation tolerance. Spartan 6 is not specifically designed for radiation tolerance but there are several techniques available to counteract this such as post CRC check, triple mode redundancy, scrubbing and ECC. Our primary choice is a combination of scrubbing and triple mode redundancy (TMR) in the FPGA. The TMR consists of majority voters in several stages connecting the 3 paths so that it can maintain functionality even with multiple errors as long as the errors occur in separate sections. We use scrubbing for the DRAM, where bad memory cells are corrected by triplicating the memory blocks and continuously testing and rewriting them using a majority voting scheme. For the configuration memory one can either order a reset via the TTCrx or use the built in automatic post CRC checker that is a standard feature in all Spartan 6 devices. The optimal solution depends on the radiation level, required up time of the digitizer and the amount of resources available in the FPGA. Further redundancy can include triplicating the component pins which we chose not to do due to routing constraints.

The radiation tolerance of the board will be tested where we compare between FPGAs with different radiation mitigation techniques and FPGAs without. The study of radiation tolerance in commercial FPGAs has a broad interest since, while their use is becoming widespread in high energy physics and space applications, there are still unknowns about the radiation effects in modern semiconductor technologies as feature sizes, layouts and materials change. This work will also give us useful experience for the ATLAS upgrade.

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