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Characterisation Of The NA62 GigaTracker End Of Column Readout ASIC

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The architecture and characterisation of the End Of Column readout chip for the NA62 GigaTracker hybrid pixel detector will be presented.This chip must perform time stamping to 100 ps (RMS) or better, provide 300 μm pitch position information and operate with a dead time of 1% or less for 800 MHz-1 GHz beam rate. The demonstrator ASIC comprises a full test column with 45 pixels alongside other test structures. Current results indicate the pixel operates with a jitter of 40.2 ± 0.3 ps (RMS) for a 2.5fC input charge. The time to digital converter operates with a 97 ps time bin and exhibits a differential non-linearity of 0.17 ± 0.03 LSBs and an integral non-linearity of 0.27 ± 0.05 LSBs.

Summary

The NA62 GigaTracker (GTK) hybrid pixel detector comprises three stations situated early in the decay line, designed to measure the momentum, angle and traversal time of the incident particles entering the decay line from the target. The requirements on these parameters are driven by the demanding background rejection level necessary for the rare kaon decay measurement. In total, the beam rate incident on the GigaTracker is expected to be around 800 M Hz − 1 GHz, which equates to approximately 140 kHz per pixel in the centre, where the intensity is the highest. The total dead time of the detector is expected to be less than 1%.

Each detector instruments an area of 60 mm x 27 mm and consists of an array of 18000 pixels, each one nominally 300 x 300 μm^2 . Time stamping is required to the level of 150 ps (RMS) for the GigaTracker as a whole. The front end must accommodate a range of input charges from 5000 e− to 60000 e− .

A demonstrator ASIC has been designed and fabricated in 130 nm CMOS technology. The architecture of the implemented design employs a pixel array operating asynchronously with a single-threshold discriminator output, driving an End Of Column (EOC) Delay Locked Loop (DLL) based Time-to-Digital Converter (TDC) via calibrated transmission lines. This proof of concept ASIC has a full column of 45 pixels alongside test structures to validate and characterise individual components of the design. The time bin of the TDC is nominally 97 ps, achieved by feeding a low jitter 320 MHz clock into a delay line with 32 contributing delay cells. Time-walk compensation of the discriminated detector signal is foreseen using a Time-Over-Threshold (TOT) approach, where timestamps from the leading and trailing edges of the discriminated pixel output contribute to an off-detector look-up of the corrected time. In-depth testing of this ASIC is underway and the performance, as measured so far, is consistent with the design specifications. Detailed results on the performance of both the analogue front end and the TDC will be presented.

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