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Status Report on a MicroTCA Card for HCAL Trigger and Readout at SLHC

Wednesday 22 September 2010 11:00 (25 minutes)

We will discuss our recent experiences designing and testing a prototype MicroTCA card for HCAL Trigger and Readout at SLHC. Our second generation prototype uses a Xilinx XC5VFX70T FPGA to perform the high-speed communication and data processing for up to 8 Readout Module fibers that are streaming data at 4.8 Gbps each. The FPGA also uses two SFP+ optical interfaces at 6.4 Gbps each for data transfer to the Trigger System. A local DAQ interface in the FPGA communicates via Gigabit Ethernet with the MicroTCA MCH. We will discuss results from our Bit Error Rate Tests under a variety of challenging clocking environments including a legacy TTC system and our own 40 MHz "spread spectrum" clock generation boards. Results from the 2010 LHC Test Beam demonstrations will include issues arising from integration with legacy hardware and the level of success achieved in meeting performance expectations for future SLHC architectures.

Author: Prof. MANS, Jeremiah (University of Minnesota/CMS)

Co-author: Mr FRAHM, Erich (University of Minnesota/CMS)

Presenter: Mr FRAHM, Erich (University of Minnesota/CMS)

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