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A 3D vertically integrated deep n-well CMOS MAPS for the SuperB Layer0

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This work is concerned with the design of analog circuits for processing the signals from deep n-well (DNW) monolithic CMOS sensors. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively large area (as compared to standard MAPS) read out by a classical processing chain for capacitive detectors. Recently, a very promising approach based on the use of a vertically integrated CMOS technology (3D) has also been considered. Vertical integration processes may be very effective in providing increased functional density and charge collection efficiency. The purpose of the final paper is to describe the features of the front-end electronics with the first experimental results from the test of 3D DNW MAPS.

Summary

Experiments at future colliders, such as the SuperB factory and the International Linear Collider, will require charged particle tracking systems able to operate at high rate with excellent position resolution and low material budget. CMOS monolithic active pixel sensors (MAPS), which were first developed for imaging applications, may satisfy these demanding requirements since they combine a very high granularity sensor with the readout electronics on the same substrate. Deep n-well (DNW) CMOS MAPS were proposed a few years ago to enable the design of large, highly granular matrices of thin charged particle detectors with fast readout architecture based on sparsification techniques. These devices integrate, in the same substrate, a relatively (as compared to conventional MAPS with 3-transistor readout scheme) large collecting electrode featuring a buried n-type layer and a fully CMOS processing chain including a low noise charge preamplifier, a shaper and a threshold discriminator followed by a digital section for binary information storage and time stamping. The Apsel series chips were designed and fabricated in a 130nm CMOS technology, aiming at the development of thin tracking systems for high energy physics. The last prototype, Apsel5T, a shaper-less version with improved charge detection efficiency, has been fabricated and tested. Recently, new DNW MAPS have been designed in a vertically integrated CMOS technology. Vertical integration processes (also known as 3D), by stacking two or more standard CMOS layers one on top of the other, provide increased functional density, physical separation of the analog blocks from the digital blocks and reduction of the area covered by competitive n-wells in the sensor layer. A 3D version of the Apsel5T (Apsel5T3D) chip has been designed in a 130nm CMOS, two-layer, vertically integrated technology. The discussion of the experimental results of the 3D DNW MAPS prototype along with their comparison with the performance of the 2D version of the sensor will be provided in the conference paper.

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