SEU tolerant cells developed for the FEI4 chip

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TWEPP 2010

Aachen - 22 September 2010

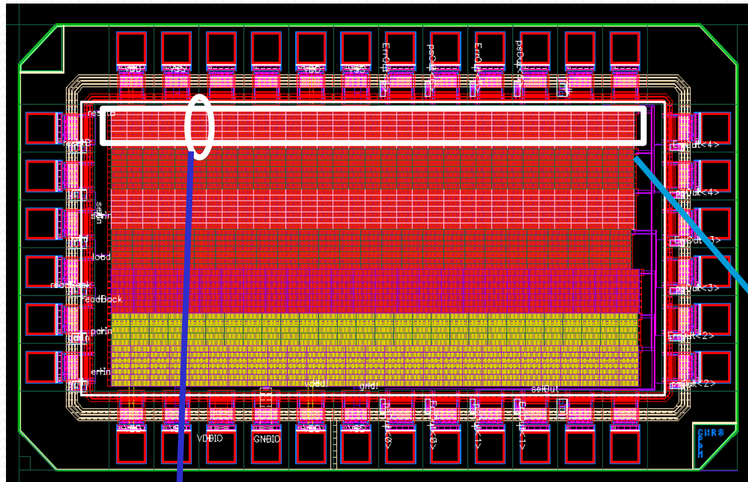
Outline

- Introduction
- Description of the SEU test chip and Experimental Test set up
- Structure of the studied latches and the different implemented layouts
- Implementation in the FEI4 chip :
  - The implementation for the pixel configuration
  - The Memory block for the global configuration
- Conclusion and perspectives

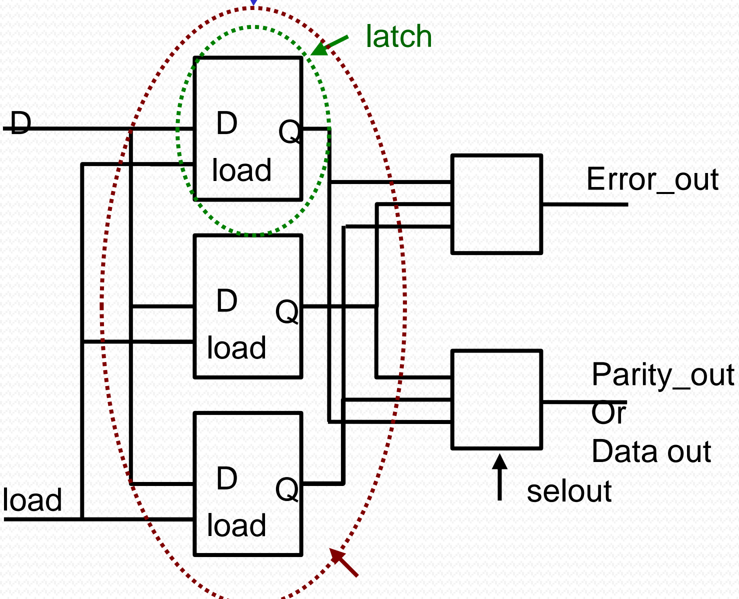
Introduction

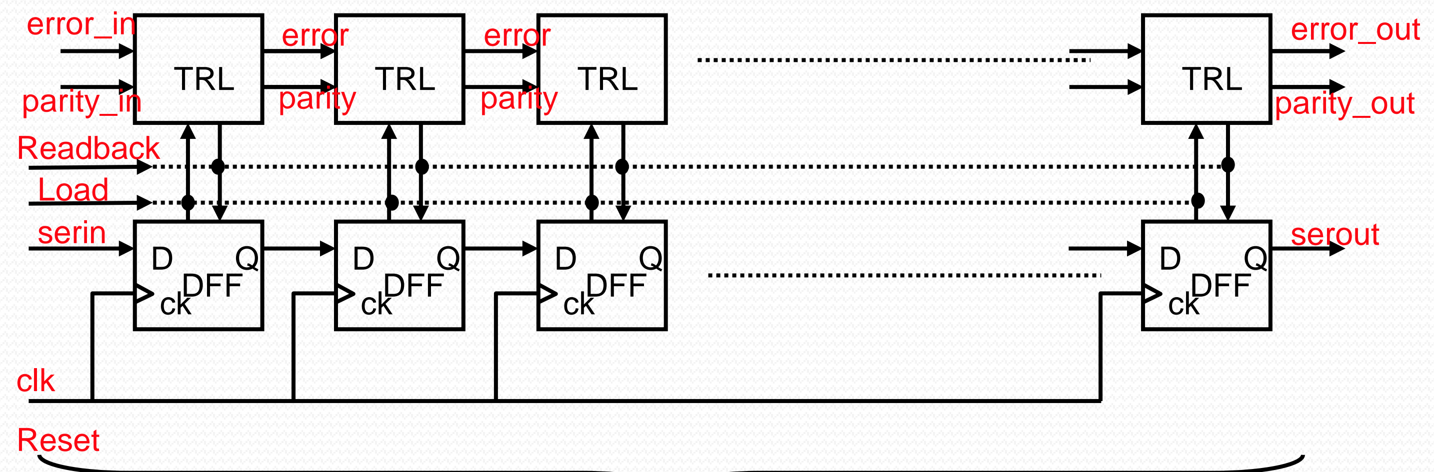
- Hardened By Design (HBD) approaches are used to reduce the effect of single bit upsets.
- Dual Interlocked Cell (DICE) latches have redundant storage nodes “dual node” and theoretically restores the original state when an upset occurs in one node.
- The upset may appear if the charge collected in two nodes exceed the critical value
- Test circuits using the130 nm CMOS process has been designed in order to study the effect of layout techniques on the tolerance of the DICE latch to single event upsets.
- Irradiation tests were carried out using IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN. The test beam provides a beam of 24 GeV protons
- We will show the structure used for the Pixel configuration block in the FEI4 chip and the other one used in the memory block used for the global configuration

SEU test chip



- Each bloc of cells have it's own error flag, parity flag and output data.
- Each tested cell is composed of 3 latches connected in triple redundancy structure.
- A logic bloc generates two flags per bloc of cells: the error flag and the parity flag.
- The error flag signal switches from 0 to 1 when the content of one latch of the bloc is corrupted. This flag indicates a single latch upset.
- The parity flag state changes when 2 latches from the same cell are corrupted. This indicates the error in the triple redundancy cell





Experimental Test set up

- Irradiation tests were carried out using IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN. The test beam provides a beam of 24 GeV protons
- It contains several spills of particles The duration of each spill is 400 ms and the intensity can be tuned typically from 5 10^{10} to 1.5 10^{11} protons/spill
- The chip is controlled and read out by a DAQ system based on a PCMCIA card . It is controlled via a PC laptop.
- An interface board located in the computing area converts 5V TTL signals to LVDS signals.
- Differential buffers drive a 20 meters twisted pair cable to transmit and receive pattern data and control signals in differential mode.
- An intermediate board located in the irradiated zone is connected with a 5 meters flat cable to the board under test.

Experimental Test Set up

Control room

Irradiation zone

Irradiated Sample In the beam

TTL to LVDS translator

LVDS to LVTTL translator

LVDS signals

Single ended

~20 meters

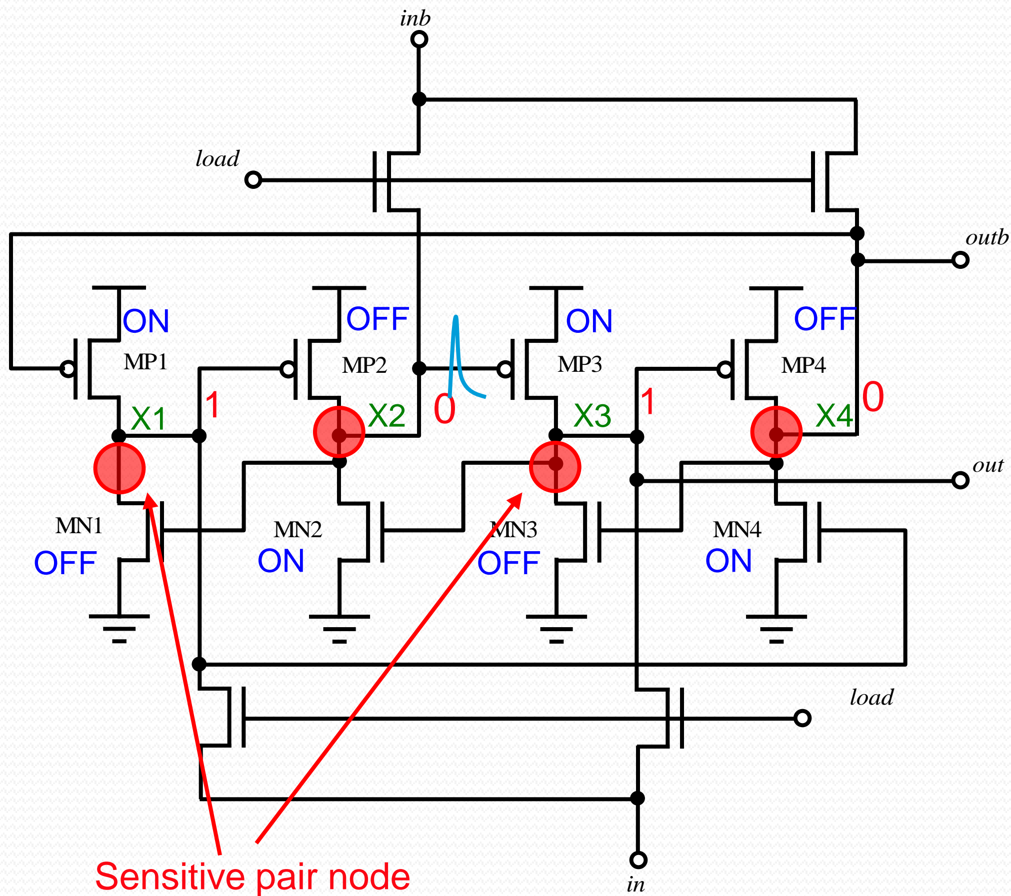
~4 meters

Outside the beam

PCMCIA Acquisition Card
LabWindows software

Power Supply

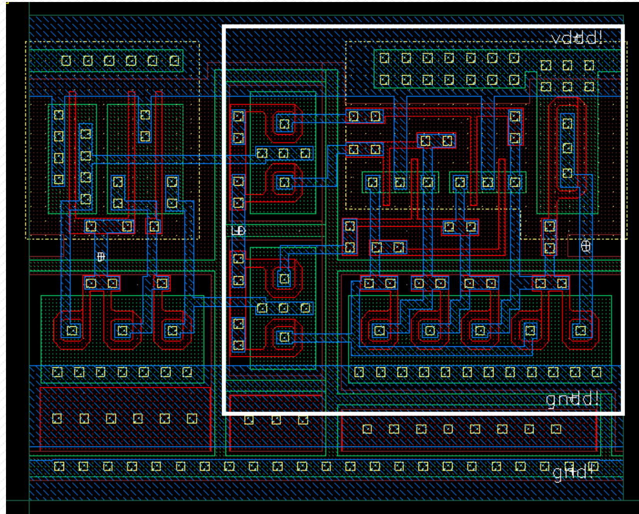
Dice Latch description



- The DICE latch is based on the conventional cross coupled inverter latch structure
- If we assume a positive upset pulse on the node X2
  - MP3 is blocked (ON -> OFF) avoiding the propagation of this perturbation to the node X3 and X4
    - The critical charge is very high
  - If 2 sensitive nodes of the cell storing the same logic state (X1-X3) or (X2-X4) are corrupted due to the effect of a single particle impact, the immunity is lost and the Dice latch is upset.
    - The critical charge becomes low (~40 fC) when a charge from upset is collected by a sensitive node pair
- For out =1
  - X1=X3=1 and X2=X4=0
  - Sensitive area corresponds to the OFF transistor drain area
- Spatial separation for the drain of MN1 and MN3
- Contacted guard ring and nwell separation for pmos MP1 and MP4 for isolation

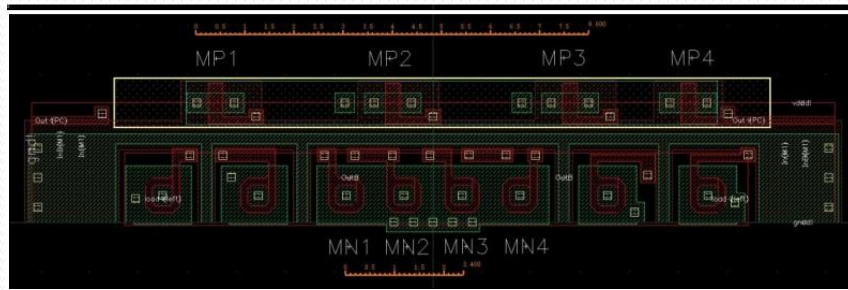
Layouts implemented in the chip SEU1

FEI3_DICE latch (latch 1)



Latch Area = 54 µm²

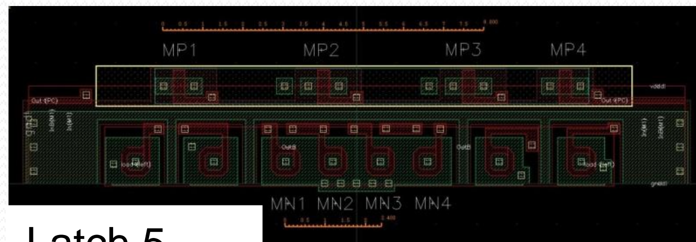
Improved DICE latch (latch 5)



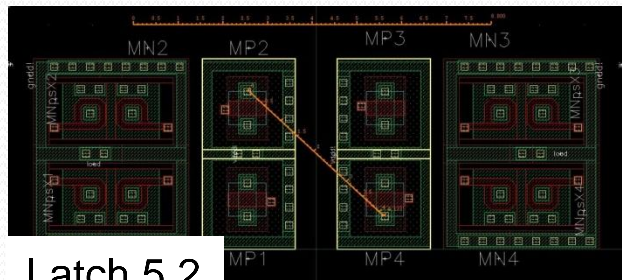
Latch Area = 48 µm²

- Measurements made in 2007 for the chip SEU1 showed that the cross section is improved by a factor ~5 just with reorganizing the layout

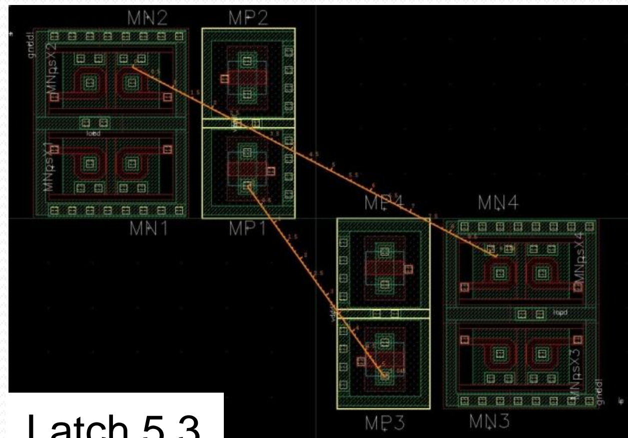
Layouts implemented in the chip SEU2



Latch 5

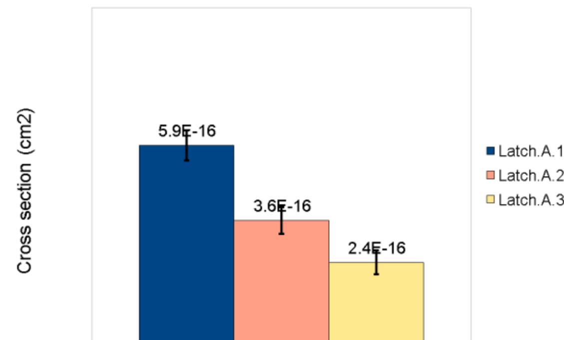


Latch 5.2



Latch 5.3

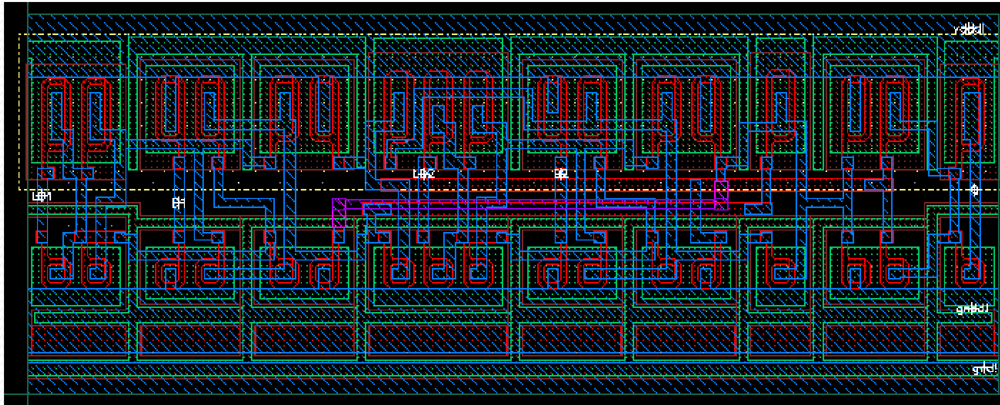
Latch type	area	Cross section cm²/bit		
		1->0	0->1	1->0 and 0->1 (*)
Latch 5	48 µm²	$(1.5 \quad 0.1).10^{-15}$	$(2.2 \quad 0.3).10^{-16}$	$(5.9 \quad 0.5).10^{-16}$
Latch 5.2	48 µm²	$(3.4 \quad 0.6).10^{-16}$	$(4.2 \quad 0.4).10^{-16}$	$(3.6 \quad 0.5).10^{-16}$
Latch 5.3	48 µm²	$(3.0 \quad 0.6).10^{-16}$	$(3.3 \quad 0.3)10^{-16}$	$(2.4 \quad 0.5).10^{-16}$



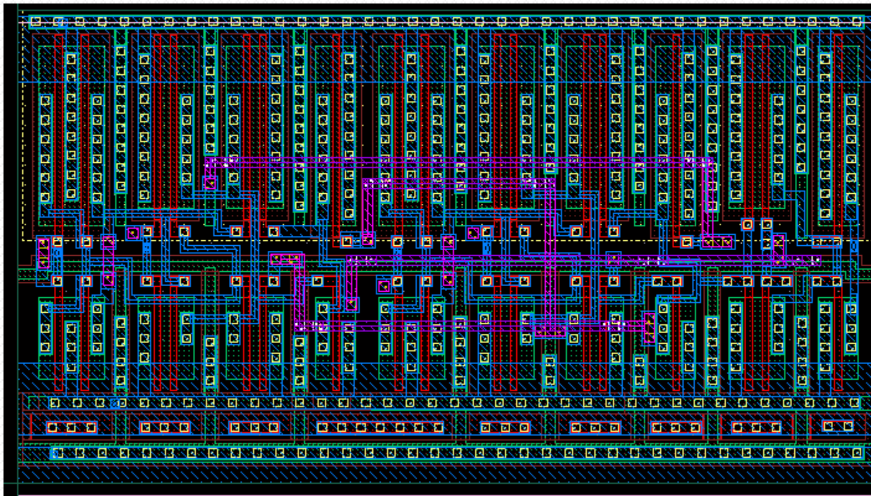
Measurements made in 2008 for the chip SEU2

- Different layout versions were implemented in the SEU2 chip
  - Same schematic but different layout
- The latch 5.3 is 2.5 times tolerant to SEU than the latch 5
- This result shows the importance of separating sensitive nodes

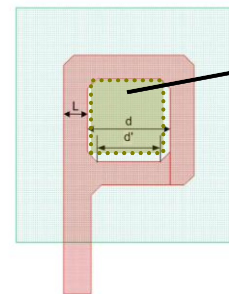
Why using enclosed layout for SEU?



Latch type	number of Transistors	size	area	Cross section cm²/bit
Design with enclosed transisors	34	23µm 9µm	207 µm²	3.0E-16
Design with linear transistors	34	18µm 10µm	180 µm²	9.0E-16

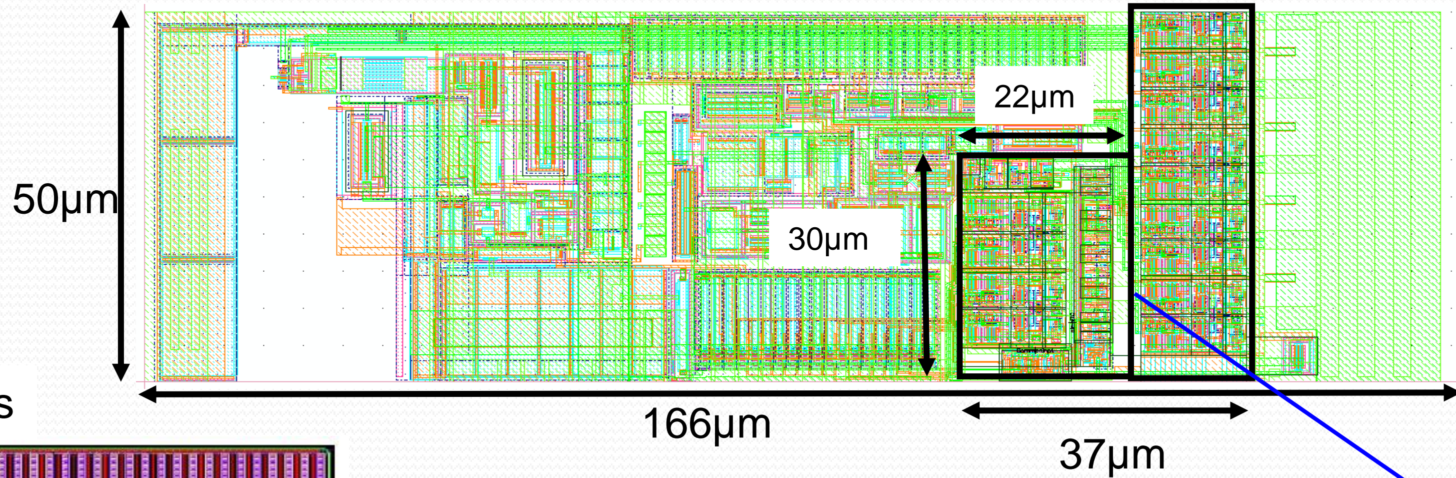


- The design with enclosed devices more tolerant to SEU
- For this structure, enclosed devices allow more tolerance against SEU
  - For a device with the same W/L, the drain diffusion area is lower for the Enclosed device



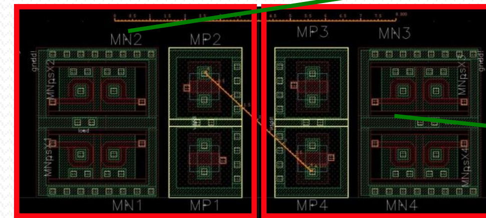
Limited sensitive area

Pixel Configuration Bloc

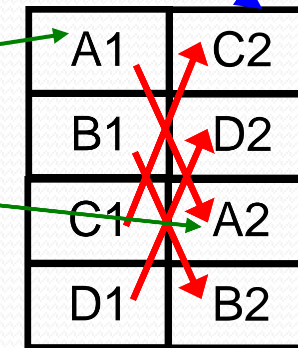


336 80 pixels

A1	C2
B1	D2
C1	A2
D1	B2
E1	G2
F1	H2
G1	I2
H1	E2
I1	F2



A1 A2
DICE latch

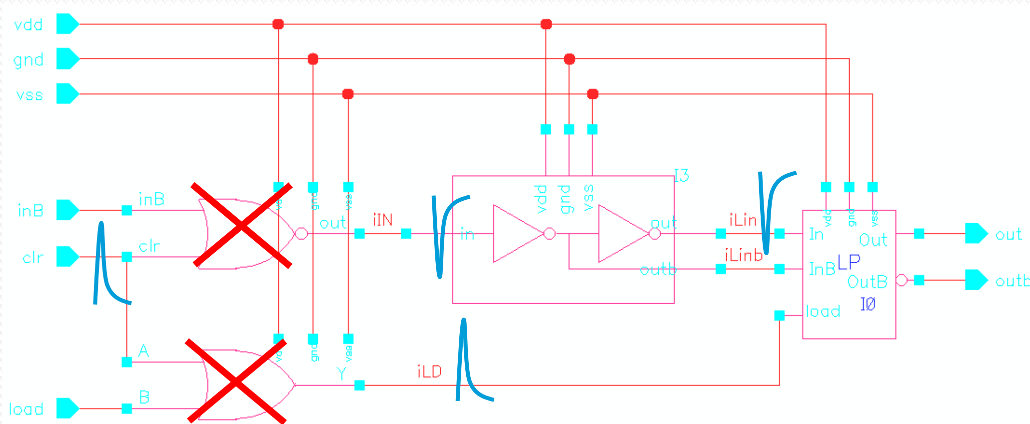


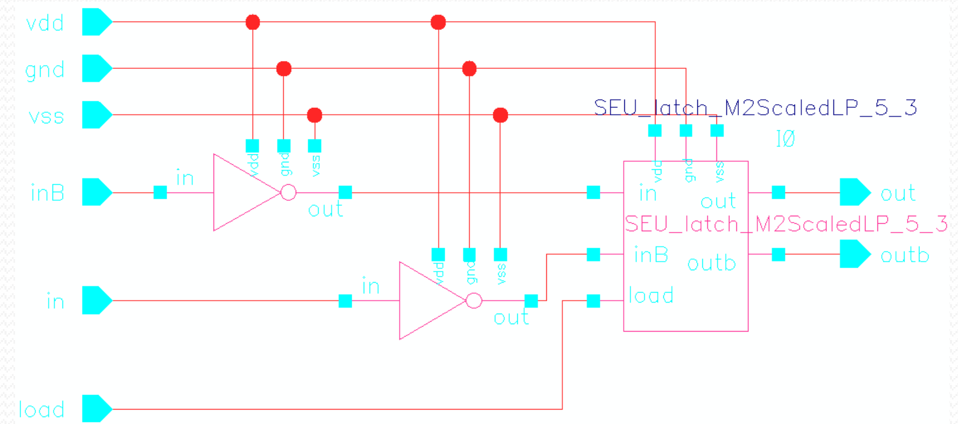
Interleaved structure

1 elementary cell

- The DICE latch is used as the elementary memory cell for the pixel configuration memory
- In order to improve the SEU tolerance, we used interleaved layout for each latch in the pixel configuration bloc

The global clear





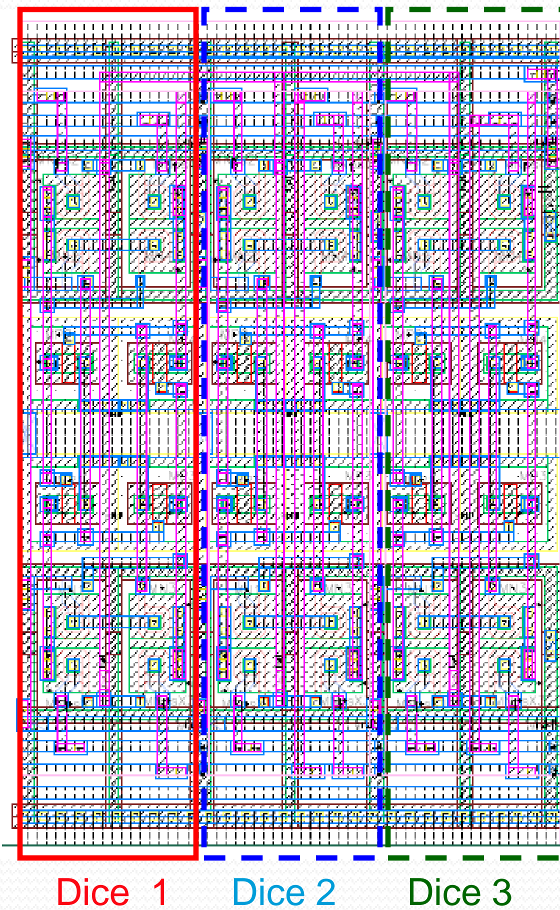
- During the FEI4 proto chip SEU tests, we observed some events where all latches are corrupted
- This is attributed to the global clear signal path
- The design was modified for the FEI4 chip where :
  - We removed the « latchclear » signal
  - We kept only 2 input buffers
- The “latch clear” is done by loading 00…00 pattern

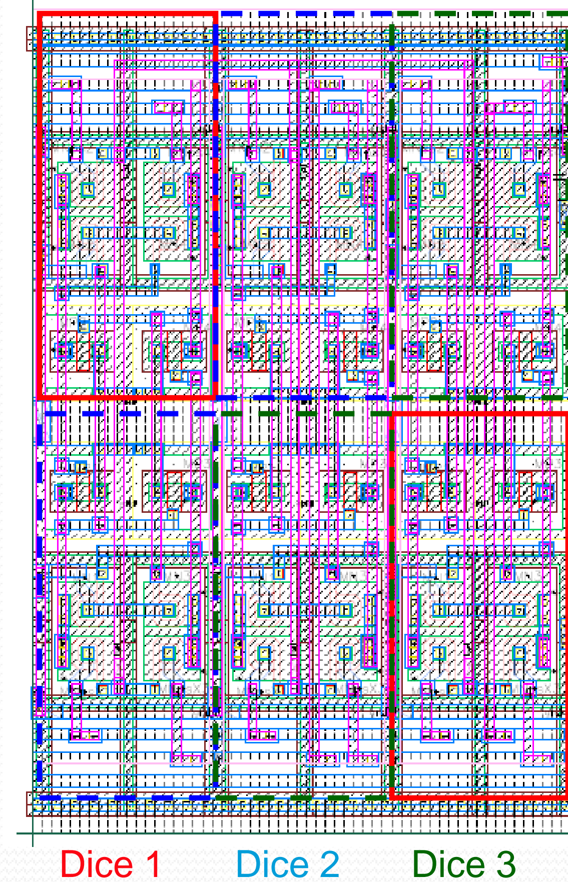
Error rate estimation for the pixel configuration in the FEI4 chip

- The SEE fluency is calculated by summing the rates of charged particles (hadrons) and neutrons with kinetic energies > 20MeV.
- the estimated SEE rate based on simulations for the LHC, is 0.23 10^{15} particle/cm²/year for the pixel B-layer
- For the B-Layer upgrade, the luminosity is 3 times higher than at the start of the LHC. If we consider 1 year =10^{7} sec and we apply a safety factor, the rate is estimated to 3.0 10^{8} part/cm^{2}.s

	Number of latches per FEI4 chip	Latch cross section (cm²/bit)	Mean time between 2 errors for one FEI chip (sec)
Pixel configuration	349 440	3.0E-16	32 sec

Layout of the triple redundant cell



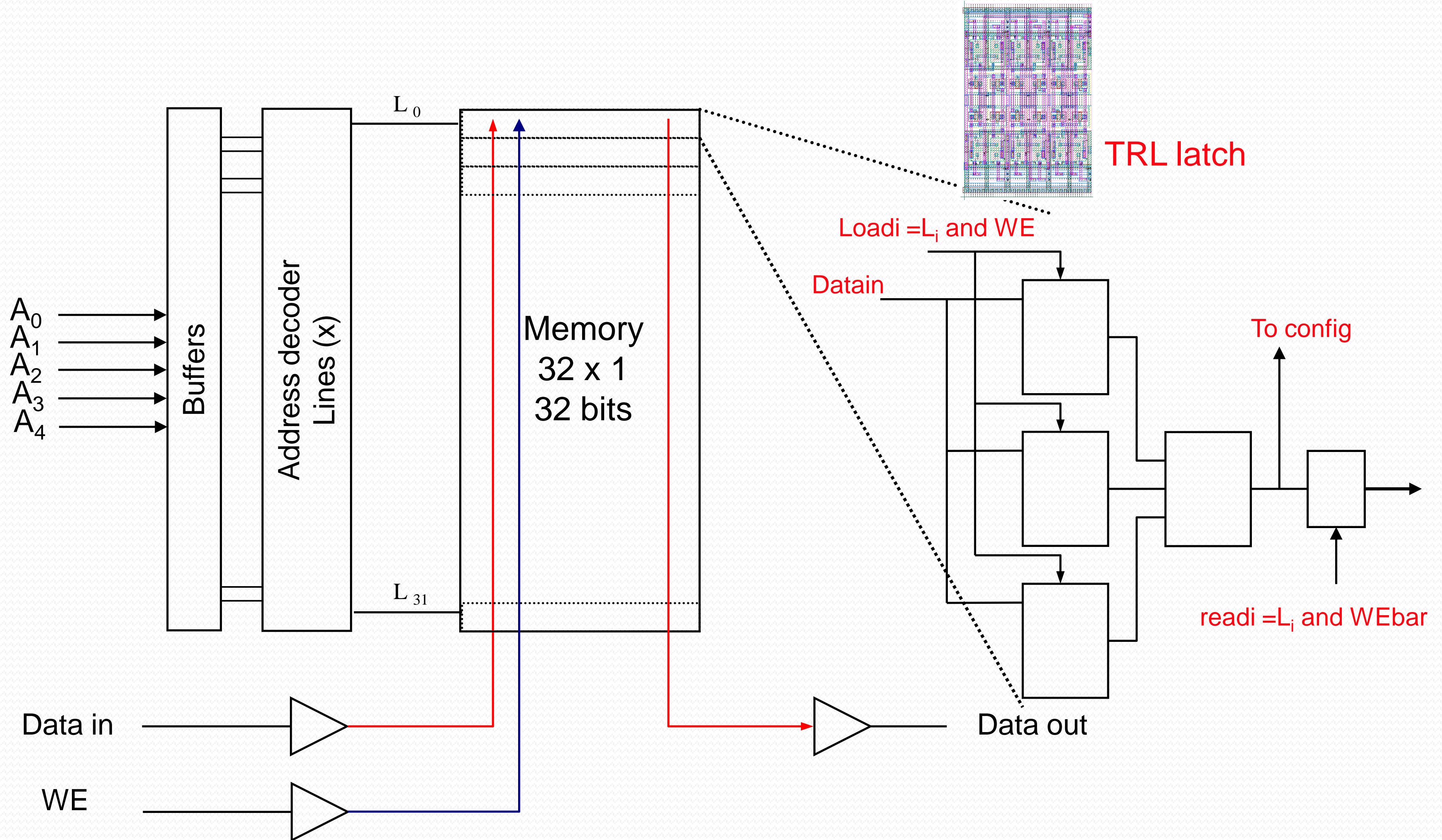


- To separate sensitive pair node we use a TRL with interleaved layout

SEU tolerance of the Triple Redundant cell

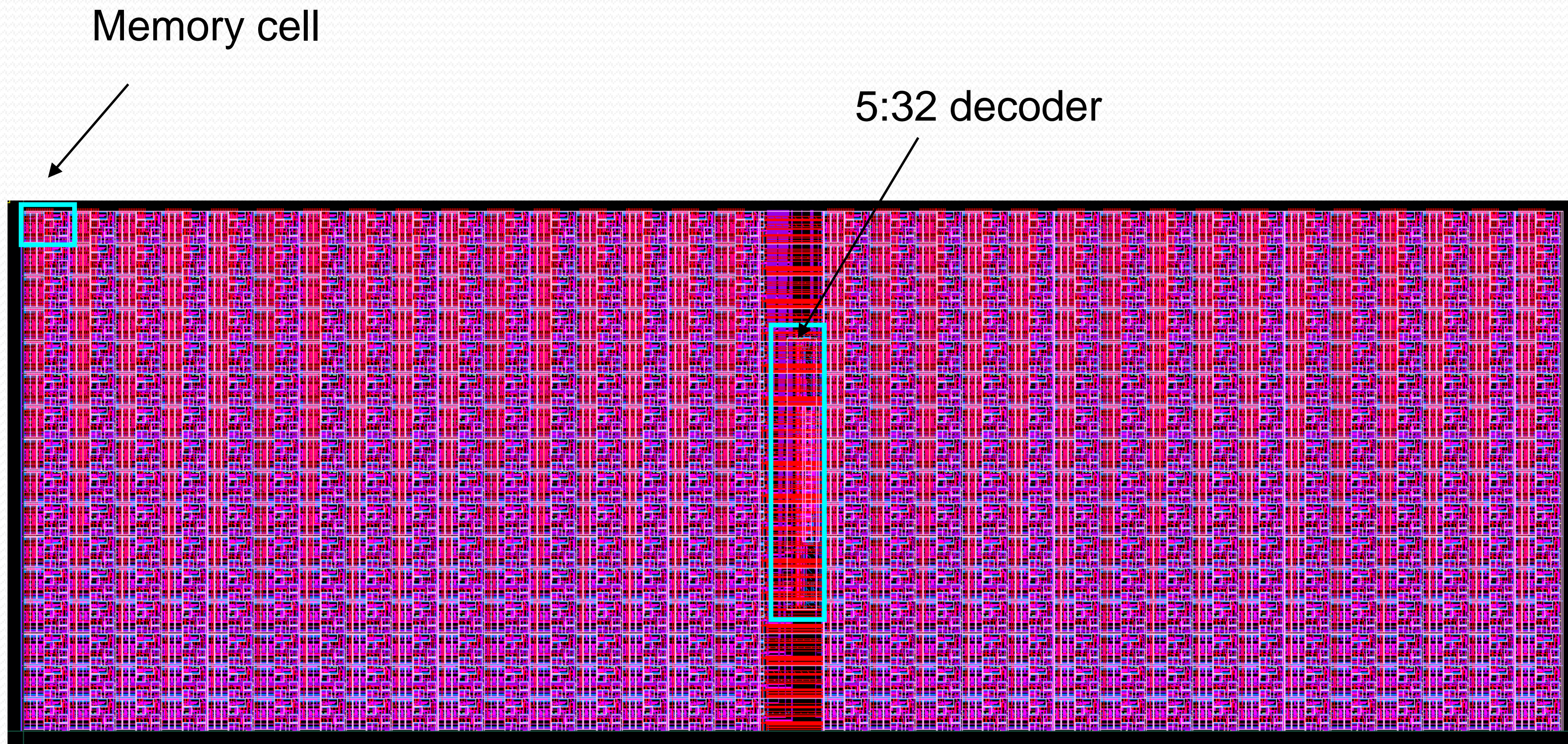
- The parity flag is used to detect a TRL cell error
- To verify that the change in the parity flag corresponds to a TRL upset
  - We check that the error flag is changed
  - Read -back data is compared to the loaded data
- For a total fluency of 6.5 10^{14} protons/cm² :
  - No errors were observed for the used TRL cells
  - The cross section for the TRL cell based on the different studied latches could be estimated to be lower than 10^{-17}/cm²
- During this test set-up, the total ionizing dose received by the tested chip is estimated around 300 Mrad. The chip is still working correctly
- Triple Redundancy Latches is used as elementary cell for the global configuration memory

Memory for global configuration



- Address : 5 bits
- Memory for 1 bit data
- Can be easily extended to 16 bits data

Memory for global configuration



16 rows by 32 columns
All inputs and outputs pins are on the top side
Block dimensions : 900µm   360µm

Conclusion and perspectives

- Several layout versions of the DICE latch were implemented and tested
  - separating sensitive nodes
  - Minimize the drain active area of the sensitive transistors
- The FEI4 chip, designed for B-Layer upgrade and submitted July 2010
- The DICE latch is used as the elementary memory cell for the pixel configuration memory
  - We kept also the standard implementation of this configuration memory in some columns
  - The new implementation will be tested and compared to the standard one
  - We can have enough statistics (~600 000 latches per chip)
- A triple redundancy was adopted for the global memory
  - We did not implement a correction logic in this version of the chip
  - This function will be tested and implemented in the next version
  - This bloc is implemented over the T3 for isolation
    - The effect on the SEU is not yet estimated

Thank you