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A Silicon Pixel Readout ASIC with 100 ps time resolution for the NA62 Experiment

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The silicon tracker of the NA62 experiment requires the measurement of the particles arrival time with a resolution better than 200 ps rms and a spatial resolution of 300 um.
A time measurement technique based on a Time to Amplitude Converter has been implemented in an ASIC in order to prove the possibility of integrate a TDC with resolution better than 200 ps in a pixel cell. Time walk problem has been addressed via the Constant Fraction Discriminator technique. The ASIC has been designed in a CMOS 130 nm technology with single event upset protection of the digital logic.

Summary

The silicon tracker of the NA62 experiment consists of 3 silicon pixel stations covering an area of 27 mm x 60 mm each, with an expected particle rate of 10^9 particles/s. The required pixel size, 300 um x 300um, is fairly large compared with other pixel readout ASICs; however, in order to cope with such an high rate, the particle arrival time has to be measured with a resolution of 200 ps rms per station.
Three main problems have to be faced in order to meet that specifications : compensation of the comparator time walk, design of an ultra-compact TDC and fast data transmission to keep the dead time below 1%. In addition, given the high particle rate, radiation effects have to be taken into account.
The first problem has been addressed by using a Constant Fraction Discriminator (CFD). By comparing the input signal with its delayed copy after an attenuation, it is possible to obtain a commutation which is almost independent from the input signal, thus preserving the initial time precision without adding extra information for correction.
The time measurement has been implemented in the pixel cell by the combination of two measurements. A global time stamp, synchronous with the 160 MHz master clock, is distributed over the pixel matrix. When the comparator fires the time stamp value is stored into an internal register, thus giving the coarse measurement. In parallel, an analog ramp is started by steering a calibrated current in a capacitor. The ramp is stopped at the successive clock rising edge, and then discharged with a current 128 times smaller than the charging one. The time stamp values at the start and at the end of the discharging ramp are stored and then subtracted in order to obtain the fine measurement. The reference clock for the fine measurement is in fact the master clock divided by two. Therefore the LSB of the coarse counter and the MSB of the fine counter correspond to the same time information, thus giving the possibility to correct for misalignment between the two circuits. The fine measurement resolution is therefore 97.65 ns. In order to allow the transients at the ramp start to settle before the measurement is made, an artificial 1 clock cycle delay is introduced.
A 4-level buffer has been implemented in the pixel cell in order to de-randomize the data. Therefore the column read-out can be made via a simple token ring protocol while keeping the dead time below 1%.
All digital registers both in the pixel cell and in the end of column logic has been designed with Hamming encoding in order to protect them from SEU.
A prototype ASIC with two full pixel column and end of column logic has been designed in a commercial CMOS 130 nm technology in order to prove the effectiveness of the technique. Overall architecture, design details and test results will be presented.

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