TWEPP 2010 Topical Workshop on Electronics for Particle Physics

Thursday, September 23, 2010

POSTERS Session - Aula (4:00 PM - 6:00 PM)

-Conveners: Mitch Newcomer

[id] title	presenter	board
[91] LVDS tester: A systematic test of cable signal transmission at the ALICE experiment	Dr TAPIA TAKAKI, Daniel	
[53] Status of the Medipix MCP-HPD development	Dr TICK, Timo	
[114] Power Supply Distribution System for Calorimeters at the LHC beyond the nominal luminosity	Mr SPIAZZI, G.	
[25] Mechanics and detector integration in the PANDA Micro-Vertex-Detector	WÜRSCHIG, Thomas	
[45] R&D Towards Cryogenic Optical Links	Mr LIU, Chonghan	
[82] CO2 Cooling for the CMS Tracker at SLHC	MERZ, Jennifer	
[33] Development of an Universal ROC	Mr MANZ, Sebastian	
[3] Subnano Time to Digital Converter implemented in PARISROC_V2 for PMm² R&D program	Mr DROUET, Sebastien	
[135] R&D towards the Module and Service Structure design for the ATLAS Inner Tracker at the Super LHC (SLHC)	IKEGAMI, Yoichi	
[12] Reliability and Performance Studies of DC-DC Conversion Powering Scheme for the CMS Pixel Tracker at SLHC	Mr PROSSER, Alan	
[93] MICROROC: MICROMEsh GAseous Structure Read-Out Chip	MARTIN-CHASSARD, Gisèle	
[131] Low Voltage Power Supply Using Step-Down Piezoelectric Transformer	UNNO, Yoshinobu	
[47] Parallel Optics Technology Assessment for the Versatile Link Project	Mr PROSSER, Alan	
[138] First experiences with the LHC BLM sanity checks	Mr EMERY, Jonathan	
[60] MAROC, a generic photomultiplier readout chip	Ms BLIN, Sylvie	
[55] Upgrade of the PreProcessor System for the ATLAS Level-1 Calorimeter Trigger	KHOMICH, Andrei	
[116] A 4.9-GHz Low Power, Low Jitter, LC Phase Locked Loop	LIU, Tiankuan	
[118] Design Studies of the ATLAS Muon Level-1 Trigger based on the MDT Detector for the LHC Upgrade	SASAKI, Osamu	
[97] Design and characterization of an SEU-robust register in 130nm CMOS for application in HEP ASICs	Dr BONACINI, Sandro	
[133] Performance of a new Preamplifier-Shaper-Discriminator chip for the ATLAS MDT Chambers in 130 nm IBM technology	Mr WEBER, Brad	
[124] ATLAS Silicon Microstrip Tracker Operation and Performance	Dr HAEFNER, Petra	
[137] Performance of the Fast Beam Conditions Monitor BCM1F of CMS in the first running periods of LHC	Mr SCHMIDT, Ringo	
[96] FPGA-based readout for double-sided silicon strip detectors	Mr SCHNELL, Robert	
[151] Front end electronics for Hybrid Avalanche Photo Diode	Mr SELJAK, Andrej	

[139] Overview of High Level Synthesis tools	Mr GEORGAKAKIS, Spyridon	
[66] A Tezzaron-Chartered 3D-IC electronic for SLHC/ATLAS hybrid pixel detectors	Mr PANGAUD, Patrick	
[27] Response of a commercial 0.25 µm Thin-Film Silicon-on-Sapphire CMOS Technology to Total Ionizing Dose	KING, Michael	
[48] Free-Space Optical Interconnects for Cableless Readout in Particle Physics	Mr PROSSER, Alan	
[104] A pixel read-out architecture implementing a two-stage token ring, zero suppression and compression	Mr HEUVELMANS, Sander	
[69] Radiated Electromagnetic Emissions of DC-DC Converters - Measurements and Simulations	Mr SAMMET, Jan	
[140] CMS Pixel Detector with new Digital Readout Architecture	MEIER, Beat	
[103] The Phase 1 Upgrade of the CMS Pixel Front-End Driver	FRIEDL, Markus	
[50] ATLAS IBL: Integration of new hw/sw readout features for the additional layer of pixels	Dr GABRIELLI, Alessandro	
[81] Performance Evaluation of Zero- Biased VCSEL for High Speed Data Transmission	Mr SILVA, Sergio	
[44] FPGA based data-flow injection module at 10 Gbit/s reading data from network exported storage and using standard protocols	Mr LEMOUZY, Benjamin	
[64] Measurement of the thermal resistance of VCSEL devices	Dr FLICK, Tobias	
[89] Design and Verification of a Bit Error Rate Tester in Altera FPGA for Optical Link Developments	XIANG, annie	
[9] Study of the electronics architecture for the mechanical stabilization of the quadrupoles of the CLIC linear accelerator	Mr FERNANDEZ CARMONA, Pablo	
[34] Design of a Small-Dimension Low-Noise Dropout Regulator Built-in Monolithic Active Pixel Sensors (MAPS) for STAR Experiment	WANG, Jia	
[83] Electronics and Cooling for the Silicon Vertex Detector of the Belle II Experiment	Mr IRMLER, Christian	
[77] Modelling radiation-effects in semiconductor lasers for use in SLHC experiments	Mr STEJSKAL, Pavel	
[99] Design and development of micro-strip stacked module prototypes for tracking at S-LHC	FIORI, Francesco	
[71] Use of Triple Modular Redundancy (TMR) technology in FPGAs for the reduction of faults due to radiation in the readout of the ATLAS Monitored Drift Tube (MDT) chambers	Mr FRAS, Markus	
[4] PMm2: A R&D on a triggerless acquisition for next generation neutrino experiments	Mr WANLIN, Eric	
[54] Detailed Performance Study of ATLAS Endcap Muon Trigger with Beam Collision Data	Mr HAYAKAWA, Takashi	
[42] The electro-mechanical integration of the NA62 Giga Tracker time tagging pixel detector	MOREL, Michel	
[11] Upgrade of the CSC Muon Port Card at the CMS Experiment	Mr MATVEEV, Mikhail	
[37] A 10Gb/s Serial Communication Transceiver in 0.13µm CMOS for a 2m Micro Twisted-Pair Cable	Dr MENSINK, Eisse	
[35] Components for the Control System of a Future Pixel Detector	Ms BECKER, Kathrin	

[130] Architecture and Instrumentation of a Silicon Strips Test Beam Telescope for the Institute for High Energy Physics, Beijing	Mr PROSSER, Alan	
[29] Digital part of PARISROC2: a photomultiplier array readout chip	Dr MARTIN-CHASSARD, Gisèle	
[122] Global noise studies for the CMS Tracker system upgrage	Dr ARTECHE, Fernando	
[123] Associative Memory design for the Fast TracK processor (FTK) at Atlas	BERETTA, Matteo	
[58] Development of a beam test telescope based on the Alibava readout system.	MARCO HERNANDEZ, Ricardo	
[52] SPACIROC: Rad-Hard Front-End Readout chip for the JEM-EUSO telescope	Mr AHMAD, Salleh	
[80] Electronics to support studies of SiPMs for High Energy Physics	Dr RUBINOV, Paul	
[84] The TOTEM T1 ReadOutCard motherboard	Dr MINUTOLI, Saverio	
[36] Developments for the upgrade of the CMS HCAL front-end electronics	GRASSI, Tullio	
[90] High speed data transfer with FPGAs and QSFP+ modules	Dr SALAMON, Andrea	
[94] The Gigabit Link interface Board (GLIB), a flexible system for the evaluation and use of GBT-based optical links	BARON, Sophie	
[43] Charge Sensitive Amplifier (CSA) in cold gas of Liquid Argon (LAr) Time Projection Chamber (TPC)	MATHEZ, Herve	
[149] An FPGA based back up version of the TileCal digitizer.	Mr ERIKSSON, Daniel Paer Erik	
[144] Development and Online Operation of Minimum Bias Triggers in ATLAS	Mr MARTIN, Tim	