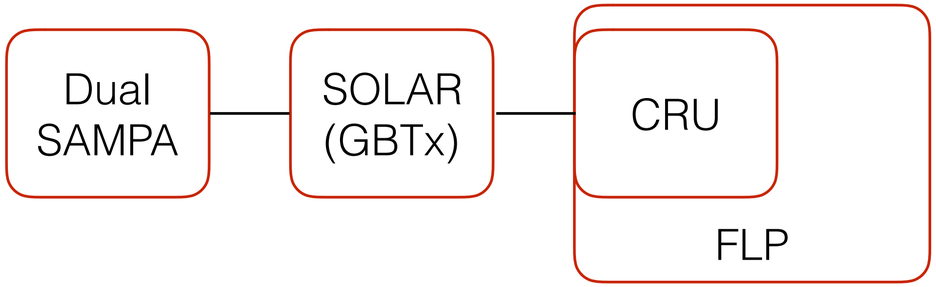
MCH CRU firmware

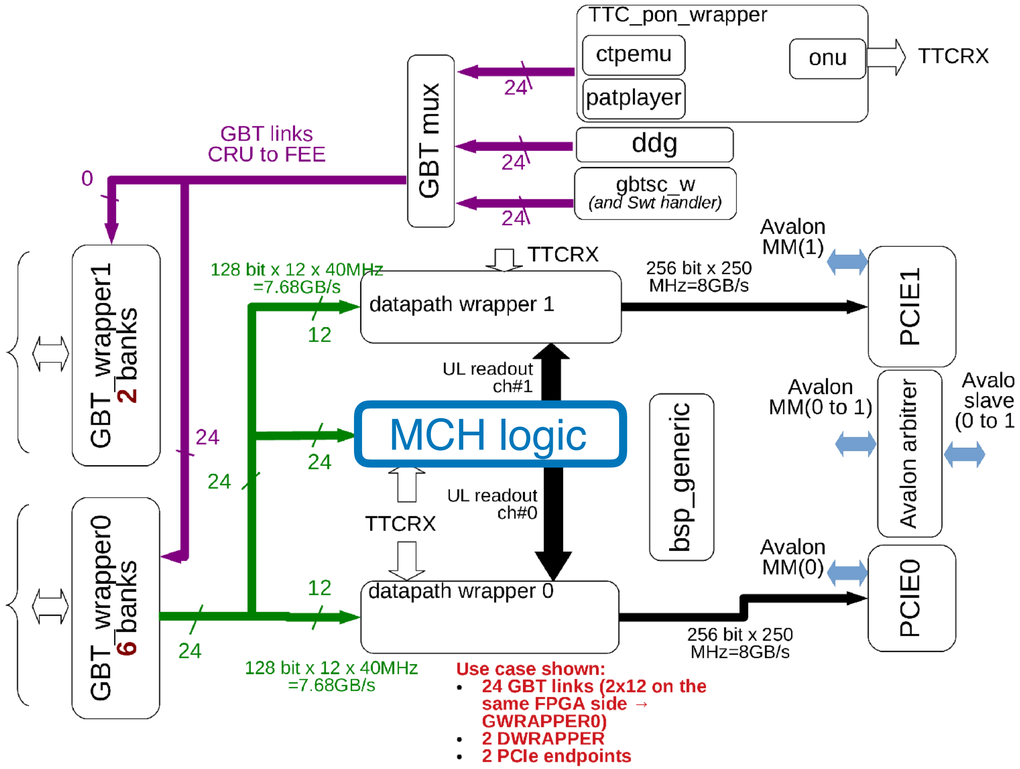
Özgür Sahin
On behalf of CEA Saclay - Irfu

Outline:

- Common readout unit
- MCH CRU functionality
- Status and test plans
- Outlook

MCH CRU firmware





The MCH CRU firmware is based on a central baseline firmware.

The MCH CRU firmware functionality:

- Takes input from 24 GBTx (each has 40 dual-SAMPA channels) links
  - Form SAMPA words,
  - Remove the SAMPA synch words,
  - Insert error checks and conditions,
- Insert TTC words to the stream,
- Sends formed MCH words to DMA (to be sent to FLP).

Two operation modes:

- Continuous
- Triggered

MCH CRU firmware

- Each e-link connected to SAMPA chips corresponds to 2-bit in the GBT word.
- e-link bits are deserialized and 10-bit SAMPA frames are formed.
  - From the SAMPA frames, 64-bit self contained SAMPA words are formed.
- SAMPA Header and Synch words are detected. Consecutive synch words are removed from the stream,
  - **Reduces the data rate to a level that can be digested by the ALICE DAQ, particularly in continuous mode.**

- GBT link ID [63-59]
- SAMPA channel ID [58-53]
- Error indicator bits [52-50]
- Payload [49-0]

MCH CRU firmware

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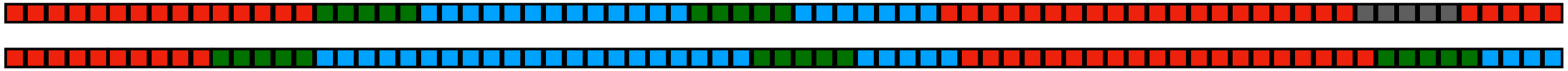
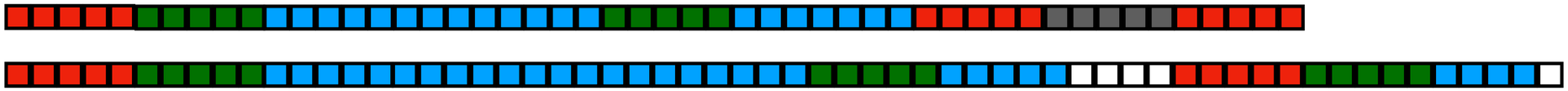
  - From the SAMPA frames, 64-bit self contained SAMPA words are formed.
- SAMPA Header and Synch words are detected. Consecutive synch words are removed from the stream,
  - **Reduces the data rate to a level that can be digested by the ALICE DAQ, particularly in continuous mode.**

10 bit synch word
10 bit data word
10 bit header word
10 bit unknown word

Input



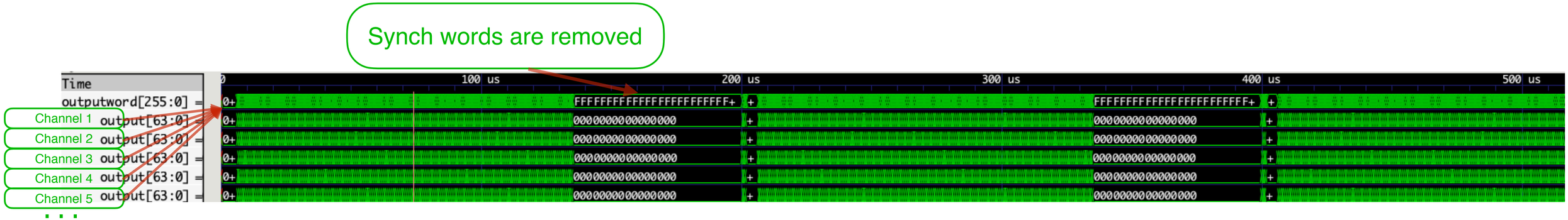
Output



MCH CRU firmware status

Tests performed:

- We use data (GBT words) collected from G-RORC and CRU raw recorder to perform simulations.
- The simulated MCH CRU firmware results are checked with a python framework.



Current status:

- Logic to send a single link is ready:
  - Software verification of the logic is ongoing - so far everything works as expected,
  - The hardware tests starts next week.

Data rate calculations

- The GBT words are received at 40 MHz (40*80 Mb/s). Each eLink is connected to a single dual SAMPA board, therefore 2 bit per GBT word reserve a single MCH Sampa frame.
- A 64 bit MCH Sampa word consists of 50 bit payload: to form a Sampa word 150 cycles at 240 MHz is necessary and hence to fill a full frame of 256 bits from a single link, 600 cycles are necessary.
  - Once the 50 bit payload is filled, a bit raised to indicate that the word is ready to be sent. The mux Sampa logic forming 256-bit word checks whether the ready bit is set and take the word to from 256 bit frame. The next word will be formed earliest in 150 cycles (at 240 MHz), the mux Sampa logic will check for the next word latest at 80 cycles.
- There are two data-wrapper instances to handle 24 GBT links received by the MCH user logic. Each instance can handle 256 bit words at 240 MHz. For each 248 256-bit words, 11 word spacing is required.
  - After mux Sampa logic forms the 256-bit word, it raises a ready bit. Mux links logic visits instances of Mux Sampa logic (an instance for each link) and add the RDH information.

Outlook

- After the single link firmware is tested in the hardware, the multilink simulation tests will be performed.
- Triggered readout needs to be implemented (requires minor modifications).
- Currently, only few error conditions are covered.
  - We plan to cover a wide range of error conditions,
- The logic uses a small amount of buffer as recommended by the central group:
  - Events with occupancies above 20% (significantly higher than expected 3%) will not be sent to FLP.