RD53A – PIXEL CHIP

RD53A COMMAND CHAIN

LVDS route can be configured to repeat CMD signal on output lane 1.

<table>
<thead>
<tr>
<th>Code</th>
<th>LVDS_0</th>
<th>LVDS_1</th>
<th>LVDS_2</th>
<th>LVDS_3</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>CMD data</td>
<td>160 MHz Clk</td>
<td>40 MHz Clk</td>
<td>Matrix reset</td>
</tr>
<tr>
<td>010</td>
<td>Cal. Edge</td>
<td>Cal. Aux</td>
<td>Matrix Trig.</td>
<td>Hit-OR 3</td>
</tr>
<tr>
<td>011</td>
<td>64 MHz Clk</td>
<td>640 MHz Clk</td>
<td>160 MHz Clk</td>
<td>160MHz delayed</td>
</tr>
<tr>
<td>111</td>
<td>0001 pattern</td>
<td>0001 pattern</td>
<td>0001 pattern</td>
<td>0001 pattern</td>
</tr>
</tbody>
</table>

CMD IN -> CMD OUT
Command lanes are daisy chained. Each chip still requires its own receiver on the bdaq53 board!
REAL SETUP
Were able to configure the chips at every position! – Digital Scans were conducted!
ERROR EVENT ANALYSIS

Histograms uninterpretable data during digital scan
Received invalid words

Total Errors discovered during analysis

RX Errors received during scan per chip

Chain starts producing significant amounts of corrupted data.
Signal degradation expected at every chip due to resampling of the CMD with the chip internal CDR clock! – Signals sampled at each individual single chip card!
Peak to Peak value
QUALITATIVE ANALYSIS

CMD Peak to Peak

Aurora Peak to Peak

Histogram peak to peak [ps]

Chip No.

1.28 GHz

640 MHz

Non gaussian Histogram

Output link specification: < 200 ps!
• Command forwarding in RD53A was proven a valid concept, but:
• Signal quality degrades significantly with each chip in line
• Feasibility can only be evaluated with RD53B due to significant architectural difference
• Measurements did not take low mass cables into account
• BDAQ53 Multichip firmware works like a charm!
Backup
CHIP1 @1.28 GHZ

CMD

AURORA
CHIP2 @1.28 GHZ

CMD

AURORA
CHIP4 @1.28 GHZ

CMD

AURORA

19.08.2019

RD53B – Pixel Chip - M. Standke

17
CHIP5 @1.28 GHZ

CMD

AURORA
CHIP6 @640 MHZ

CMD

AURORA
CHIP7 @ 640 MHz

CMD

AURORA