RD53 Status ans Plans

Pixel readout integrated circuits for extreme rate and radiation

6th LHCC Report- Sept. 11, 2019
M. Garcia-Sciveres (LBNL) on behalf of the RD53 Collaboration
Previously on RD53

- Focused R&D to develop pixel chips for both ATLAS and CMS upgrades
- Established in 2013 recognizing that HL-LHC pixel requirements were extremely challenging, yet very similar for both experiment, and a joint effort was the best way to meet them
- Successful R&D culminated in the RD53A prototype chip, fabricated at the end of 2017. This fulfilled the original mandate of RD53.
  - RD53A continues to be extensively used by both experiment to prototype their HL-LHC detectors. 110 RD53A wafers have been purchased to date – 3x as many pixels as current ATLAS and CMS combined.
- At the request of the experiments, last year the mandate of RD53 was extended to design the final production chips for ATLAS and CMS
  - Keep the design team together.
  - Pursue as much as possible a common design to serve the needs of both experiments.
- RD53 has 22 collaborating institutes and many Guests
  - ~100 conference talks/proceedings/papers to date
The Most Important Aspect of RD53

The people
RD53 Designs and Chips

- RD53A is the existing prototype
- RD53B is not a physical chip. It is a design library / environment
- The first incarnation of RD53B will be RD53B-ATLAS (which ATLAS calls ItkPix-V1) To be fabricated this fall.
- The second incarnation will be RD53B-CMS, to be fabricated in 2020 (may be able to take advantage of initial RD53B-ATLAS test results)
- Each chip is made of two RD53B elements: the chip bottom and a matrix of identical “cores”. Each core has 64 pixels.

The main difference between ATLAS and CMS is the number of cores. The analog front end inside the core is also different. The environment was designed to handle such variation.
One Core

One flat synthesized circuit
~ 200k transistors
64 pixels in 16 “analog islands”
Whole core is stepped and repeated to make the pixel matrix

Hand-drawn transistors
“compiled software”
Chip size: 20.066 x 11.538 mm$^2$
400x192

- Aug. 31, 2017: Submission
- Dec. 6, 2017: First chip test
- Mar. 15, 2018: 25 wafers ordered
- Apr. 13, 2018: First bump-bonded chip test

Chip doc on CDS: http://cds.cern.ch/record/2287593
20 x 21 mm²
## RD53B Basic Specs

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td><strong>Pixel size</strong></td>
<td>50x50 um² &amp; 25x100 um²</td>
</tr>
<tr>
<td><strong>Pixels (ATLAS/CMS)</strong></td>
<td>400 x 384 = 163,600 / 432 x 336 = 145,152</td>
</tr>
<tr>
<td><strong>Detector capacitance</strong></td>
<td>&lt; 100 fF (200 fF for edge pixels)</td>
</tr>
<tr>
<td><strong>Detector leakage worst case</strong></td>
<td>&lt; 10n A (20 nA for edge pixels)</td>
</tr>
<tr>
<td><strong>Detection threshold</strong></td>
<td>&lt; 600 e-</td>
</tr>
<tr>
<td><strong>In-time threshold</strong></td>
<td>&lt; 1200 e-</td>
</tr>
<tr>
<td><strong>Noise hits</strong></td>
<td>&lt; 10^-6</td>
</tr>
<tr>
<td><strong>Hit rate</strong></td>
<td>&lt; 3 GHz/cm² (75 kHz avg. per pixel)</td>
</tr>
<tr>
<td><strong>Trigger</strong></td>
<td>1 or 2-level configurable. Tag-based</td>
</tr>
<tr>
<td>Max. 1-level readout rate</td>
<td>&gt; 4 MHz</td>
</tr>
<tr>
<td>Max. 2-level readout rate</td>
<td>~ 1 MHz</td>
</tr>
<tr>
<td>1-level max. latency</td>
<td>12.5 us</td>
</tr>
<tr>
<td>2nd level max. latency</td>
<td>25 us</td>
</tr>
<tr>
<td><strong>Hit loss at max hit rate</strong></td>
<td>≤ 1%</td>
</tr>
<tr>
<td><strong>Charge readout / resolution</strong></td>
<td>4 bit readout / 6-bit to 4-bit @ 80 MHz</td>
</tr>
<tr>
<td><strong>Readout data rate</strong></td>
<td>1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s</td>
</tr>
<tr>
<td><strong>Radiation tolerance</strong></td>
<td>500 Mrad at -15°C</td>
</tr>
<tr>
<td><strong>SEU affecting whole chip</strong></td>
<td>&lt; 0.05 /hr/chip at 1.5GHz/cm² particle flux</td>
</tr>
<tr>
<td><strong>Power consumption at max hit/trigger rate</strong></td>
<td>&lt; 1 W/cm² including ShLDO losses</td>
</tr>
<tr>
<td><strong>Pixel analog/digital current</strong></td>
<td>3-5uA/3uA</td>
</tr>
<tr>
<td><strong>Temperature range</strong></td>
<td>-40°C ÷ 40°C</td>
</tr>
</tbody>
</table>

See requirements doc: https://cds.cern.ch/record/2663161 and manual: https://cds.cern.ch/record/2665301
ATLAS: 400 columns x 384 rows
CMS: 432 columns x 336 rows
New Feature Highlight

- Encoding with lossless compression used to send data off chip.
  - Custom serial stream encoding to achieve compression AND be tolerant of corrupted fragments
- Important because, thanks to serial power, services volume (and mass) is dominated by data cables.

CMS Example

(note compressed data is independent of pixel shape)
RD53B Status

- All design work getting finishing touches this month
  - Very significant amount of design work done - not just cut and paste from RD53A
  - Almost every circuit has been touched at some level and several new functions (not in RD53A) have been added
- Verification is critical. Advanced, but not yet completed
- Must reach a high level of confidence through verification in order to submit
  - 143K lines of System Verilog code to verify 26.5K lines of chip code
  - RD53 internal workshop in progress at CERN to check design and pour over all simulation and verification results
- ATLAS Final Design Review of ITkPix-V1 is on Friday
  - Also must be completed before order for wafer run can be placed.
  - [https://indico.cern.ch/event/835605/](https://indico.cern.ch/event/835605/)
Verification / Simulation examples

RD53B Full chip digital

RD53B Full core Analog (with parasitics)

ToT [ns] for Qin = 1200 e-

Core row
0 1 2 3 4 5 6 7

Core column
0 2 4 6

+0.3ns
max
45.46ns
min
-0.3ns

RD53 Report to open LHCC – M. Garcia-Sciveres
Circuits Validated in Silicon

SLDO Testchip A
Submitted on August 2018

SLDO Testchip B
Submitted November 2018

SLDO Testchip C
Submitted February 2019

Bandgap Test Chip
Submitted Aug. 2018

CDR/PLL Test Chip
Submitted Aug. 2018

Ring Oscillator Test Chip
Submitted Nov. 2018

ADC Chip
Submitted Aug. 2018

SEU Test Chip
Submitted Aug. 2018
Single Event Effect Testing

Laser Injection on test chips

Whole VCO scanned in one run, focus closer to M1

Ions on test chips

Charge injection in simulation

Single DFF

\[ \sigma_{\text{meas}} = 7.19 \times 10^{-9} \text{ cm}^2 \]

\[ \text{LET}_{\text{th}} = 1.40 \text{ MeV} \]

\[ W = 14.02 \]

\[ S = 1.00 \]
Conclusions

- RD53 collaboration mandate has been extended to design the production pixel readout chips for ATLAS and CMS
- Configurable design called RD53B
  - Will be instantiated first for ATLAS (submission this fall)
  - ATLAS Final Design Review this Friday
  - CMS chip submission will follow in 2020
- RD53B contains new features needed for production
- Extensive simulation and verification program significantly expanded relative to what was done for RD53A
- More info at cern.ch/RD53
BACKUP
Design Team

RD53 design framework for final pixel chips: Flavio Loddo, Bari; Deputy: Tomasz Hemperek, Bonn

Floorplan/integration:
Flavio Loddo, Bari
- Pixel array, Bump pad, EOC, Power distribution, Bias distribution, Analog/digital isolation, Integration, Verification

Digital integration:
Tomasz Hemperek, Bonn; Luca Pacher, Torino
- Simulation Framework:
  Sara Marconi, CERN;
  - Framework, Hit generation/Import MC, Reference model/score board, Monitoring/Verification tools, Readout rate estimations, Behavioural pixel chip, SEU injection.
  - Pixel array logic:
    Sara Marconi, CERN
    - FE interface, Latency buffer, Core/column bus
  - Digital chip bottom:
    Roberto Beccherle, Pisa; Francesco Crescioli, LPNHE;
    - Configuration, Control interface, Readout data format/protocol, Compression

- Verification:
  Sara Marconi, CERN; Attiq Rehman, Bergen,
  Joel De Witt, Santa Cruz
  Cesar Gonzales-Renteria, LBNL
  Peilin Liu, LBNL
  SEU: Pedro Leitao, CERN; Rafael Girona, Sevilla
  SET: Fernando Munoz Chavero, Sevilla
  LPGBT: Pedro Leitao, CERN
  Mixed signal: Luca Pacher, Torino;
  Aikaterini Papadopoulou, LBNL
  - Functional, SEU, Interfaces, specifications

- Library cells:
  DICE: Denis Fougeron, Mohsine Menouni, CPPM
  Timing characterization: Sandeep Miryala, FNL

Serial Power:
SLDO: Michael Karagounis, Andreas Stiller, Dortmund.
Bandgap: Gianluca Travarsi,
Verification: Alvaro Pradas, ITAINNOVA;
Stella Orfanelli, CERN; Dominik Koukola, CERN
- Shunt-DO integration, On-chip power distribution, Optimization for serial powering, System level power aspects, Power Verification

Design for testability:
Giuseppe De Robertis, Bari
- Scan path, BIST, production test patterns, Fault simulation, Bump bonding testing

IPS: Support and possible updates
Current DAC: Bari
Voltage DAC: Prague
ADC, mux, temp: CPPM
Power on reset: Seville
Ring oscillator: LAL
Analog buffer: RAL

Support and services:
Tools, design kit: Wojciech Bialas, CERN
Repositories: Flavio Loddo, Bari; Luca Pacher, Torino; Tomasz Hemperek, Bonn
Radiation model: Mohsine Menouni, CPPM; CERN

Names in bold: Member of RD53 management board

Testing: Timon Heim, LBNL
YARR system: Timon Heim, LBNL
BDAQ53 system: Marco Vogt, Michael Daas, Yannik Dieter, Hans Krueger, Tomasz Hemperek, Mark Standtke Bonn
Radiation test: Luis Miguel Jara Casas, CERN, Mohsine Menouni, CPPM.
Plus many ATLAS/CMS groups not formally part of RD53

Pixel sensor and bump-bonding:
Fabian Huegging, Bonn (ATLAS), Georg Steinbrueck, Hamburg (CMS)
RD53B New Features

- Selected Diff. Front End for ATLAS, Lin. FE for CMS
- Added edge, top, and corner pixel biases
- Upgraded calibration injection & corrected column variation
- New hit synchronization and ToT with 6b-to-4b compression
- Redesign of the startup and generation of reference voltages
- Improvement of SLDO and addition of low power mode
- Addition of overcurrent and overvoltage protection
- Redesigned PLL for lower jitter and robust locking
- Added trigger tags and new readout format with compression
- Added 2-lever trigger for ATLAS and self-trigger
- Added suppression of low charge isolated hit backgrounds
- Added data aggregation between chips
- Changed reset scheme to synchronous and added CMD activity reset
- Extensive triplication and SEU hardening
- Added new resistive temperature sensors and E-fuses for SN
- Added precision ToT and ToA
- Enlarged wire bond pads
RD53B-ATLAS & CMS side-by-side

20 x 21 mm²

21.6 x 18.6 mm²
RD53A Database

- Database of RD53A chips in use at cern.ch/rd53a-chips

Current Wafer: 3

[Diagram showing the distribution of RD53A chips on a wafer]

[Table showing serial number, diced location, diced date, thickness, bumped status, sensor type, flip date, board number, board date, status history, location history, radiation (Mrad), chip comment, board comment, and board type]
RD53A Wafer Probing

- Wafer Probing
  - Probed 58 wafers in total
    - 41 in Bonn (for RD53 and ATLAS)
    - 17 at CERN (for CMS)
  - 89 chips per wafer: Over 5000 chips for statistical analysis
  - Designated in parts for RD53, ATLAS and CMS

- Test procedure very stable
- Results look as expected