LS2 upgrades:

ITS – Norwegian (Bergen) activities

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CCNU-UIB collaboration - 20 years of joint-research,
UiB, Bergen 22nd and 23rd of August 2019

UNIVERSITY OF BERGEN

Bergen Staff

- Scientific staff: Dieter Röhrich, Kjetil Ullaland, Johan Alme
- Engineering staff: Attiq ur Rehman, Ganesh Tambave, Shiming Yang
- PhD candidates:
  - Simon Voigt Nesbø (→ May 2020)
  - Magnus Rentsch Ersdal (→November 2021)
  - Shiming Yuan (→ January 2022)

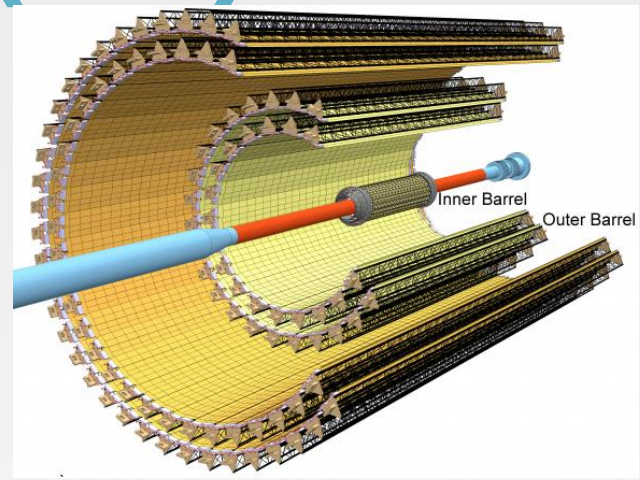
Projects

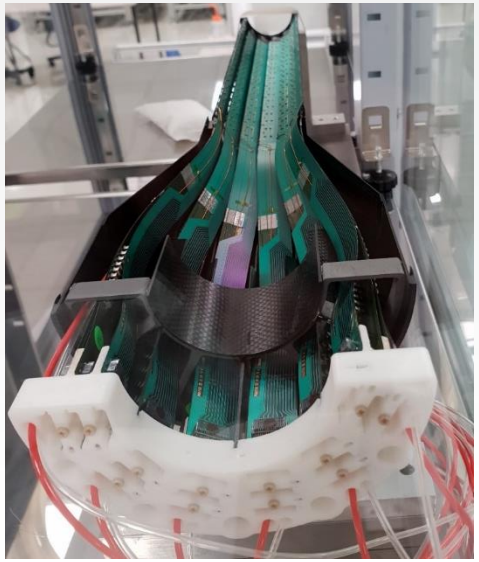
- Primary activity:
  - Working group 10 - development of readout electronics and related software
- Other activities:
  - Working group 5 & 6 – ALPIDE testing and HIC/stave testing
  - Commissioning

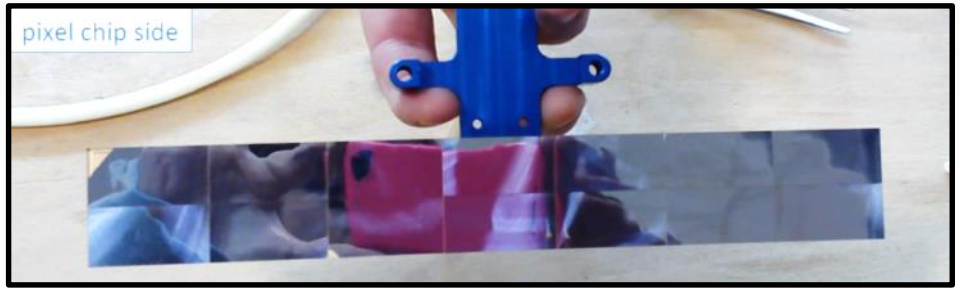
ALICE Inner Tracking System (ITS)

- Pixel detector - 12.5 Gpixel camera (~10 m^2)
  - 7 layers – 24 142 ALPIDEs
  - 192 Staves with 9 to 196 ALPIDEs depending on layer

- ALPIDE CMOS MAPS sensor chip
  - 512x1024 pixels – 30x15 mm^2
  - Digital periphery for data offloading and configuration
  - 1.2 Gbps high speed link
  - Data compression algorithms implemented

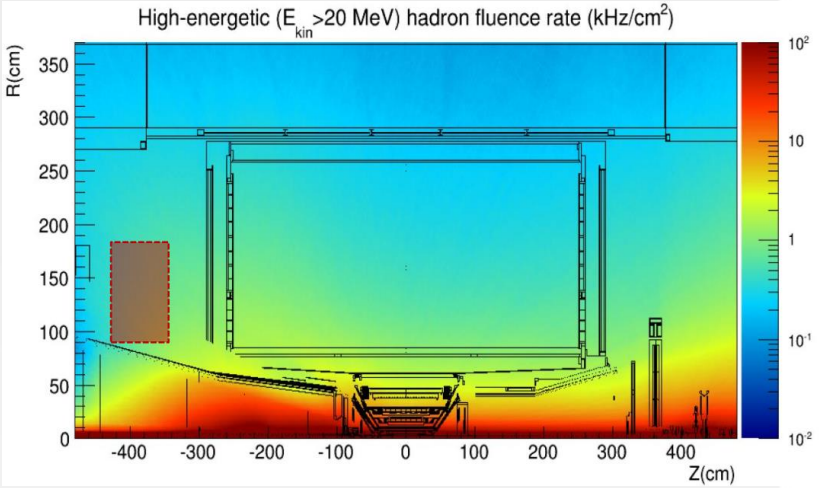


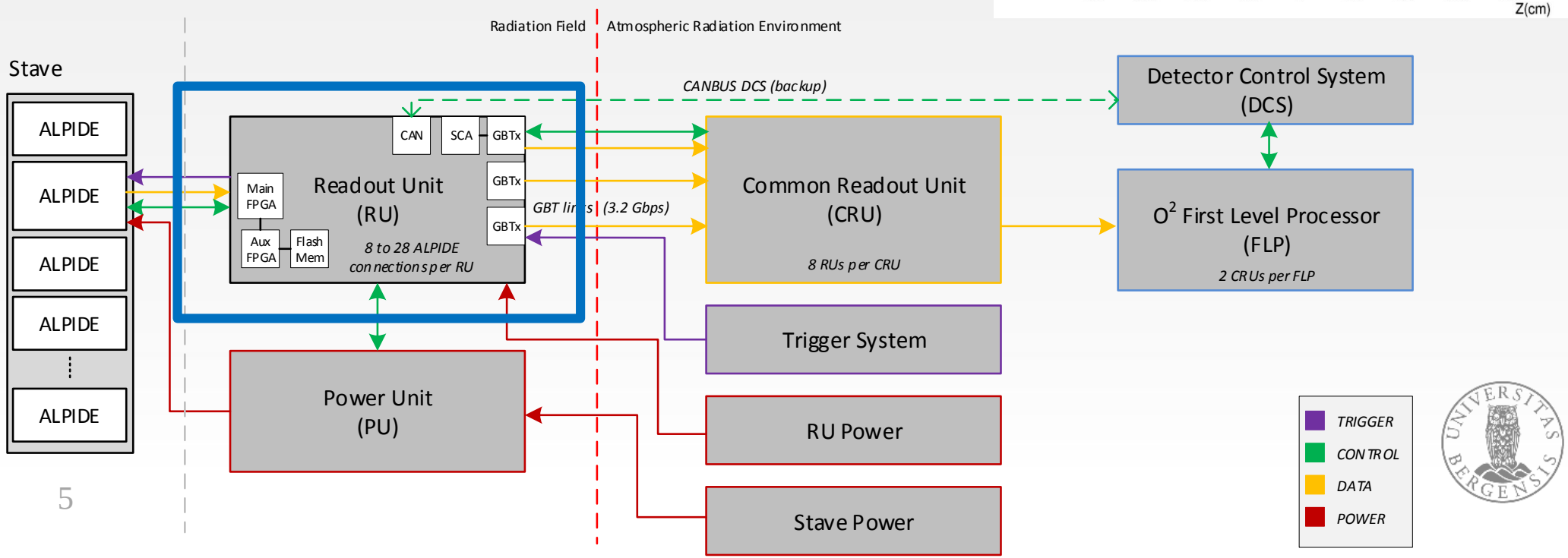




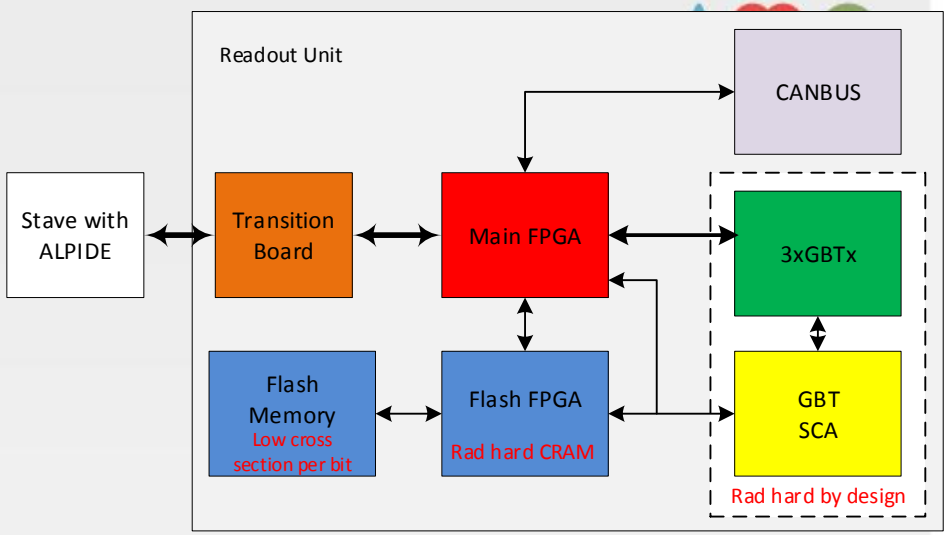
Readout Electronics in the Radiation Environment

- 192 Staves – 192 Readout Units.
- Installed in racks ~3 meters from the interaction point
- High Energy Hadron flux $\phi_{E_{kin}>20MeV} \approx 1\ kHz/cm^2$
  - Will cause single event upsets in memory elements!
- Dose effects not considered to be a problem

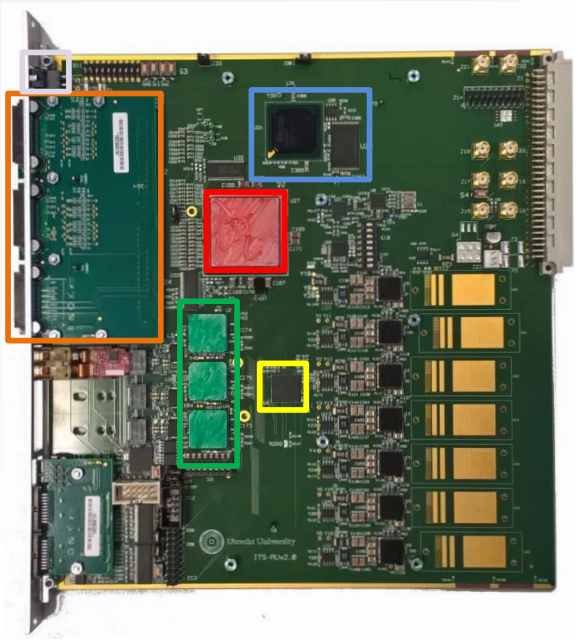




Readout Unit



- Xilinx Ultrascale XUv40
  - Main FPGA
  - Data flow (ALPIDE -> XU -> GBTx -> CRU)
  - Control of ALPIDEs (GBTx/CANbus)
  - Configuration elements: SRAM based
    - Must be protected against single event upsets in configuration memory
- Microsemi proASIC3L 600
  - Support FPGA
  - Initial configuration & scrubbing of Xilinx Ultrascale
  - Configuration elements: flash based
    - Considered to be immune to single event effects
- Samsung Flash Memory K9KAG08U0M
  - 8Gb Flash Memory – 2 internal ICs – common interface
  - Irradiation campaigns have shown a (low) susceptability towards SEUs



Requirements for External Scrubber

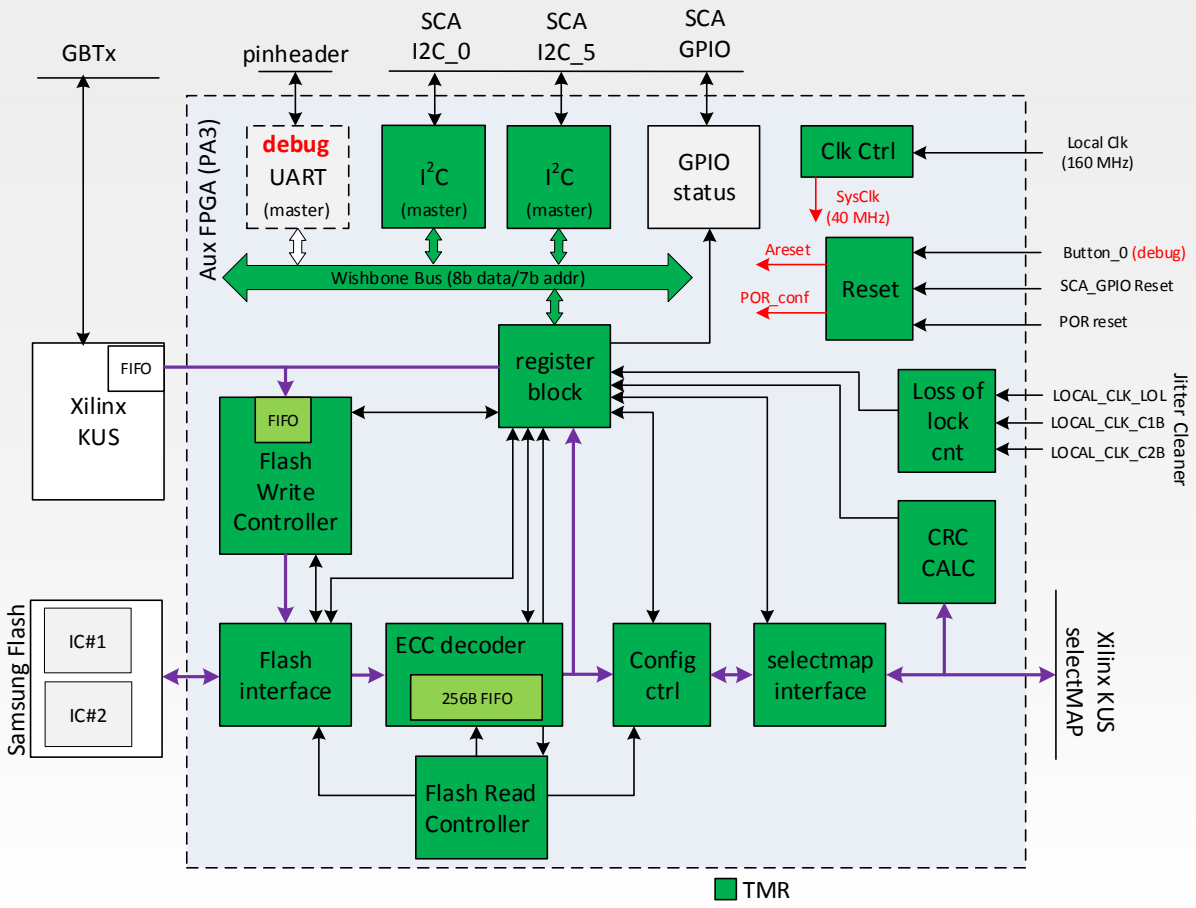
- Initial configuration of Xilinx Ultrascale (XU - main fpga) using configuration stored in on-board flash memory, using SelectMAP bus
- Scrubbing of XU configuration Memory (using SelectMAP bus)

- Additional requirements:
  - Scrubbing and initial configuration must be «fast enough»
    - Scrubbing cycles should have a significantly higher frequency than SEU rate, rule of thumb: 10x (xapp216*)
    - Worst case SEU rate: ~0.0006 SEU/s per Readout Unit. (450/h for all 192 RUs)
  - Radiation tolerant
  - Efficient control interface
    - Two I^2C interfaces are available in Hardware
  - Efficient upload of files

- Commisioning feature:
  - Fault injection implemented in HW to test radiation tolerance of Xilinx design

*https://www.xilinx.com/support/documentation/application_notes/xapp216.pdf

External Scrubber Design

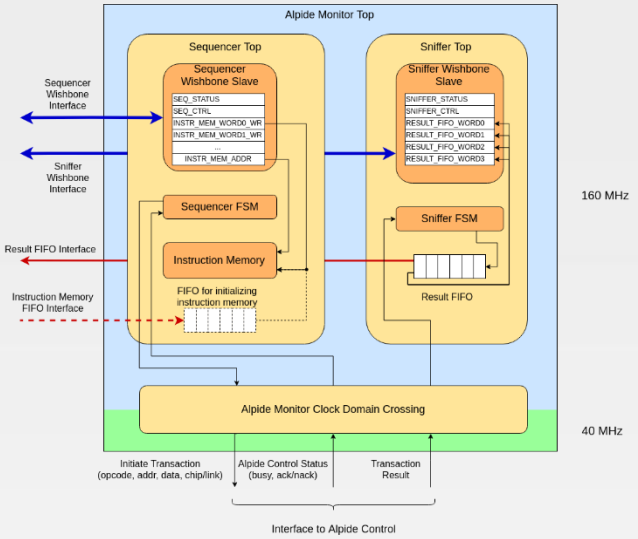


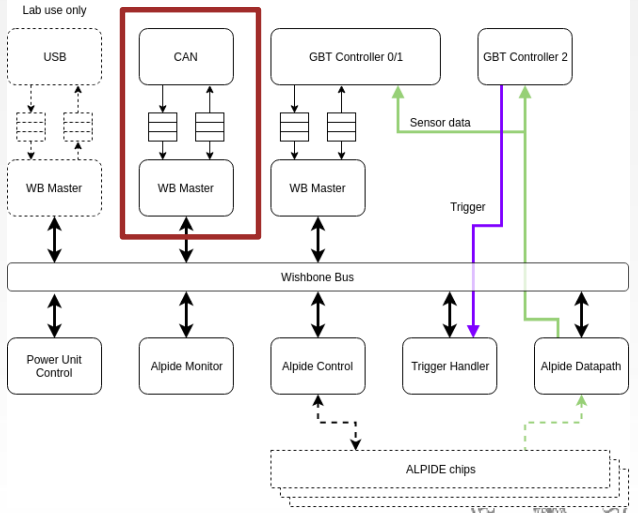
Key numbers:

- Initial config : ~2s
- Scrubbing : ~1.7s
- Writing to flash memory done via scripts
  - I^2C: ~230 kbps
  - SWT (Xilinx FIFO): ~4 mbps
- Resource utilization
  - Logic cells: 79%
  - RAM: 4 of 24

Xilinx Design components

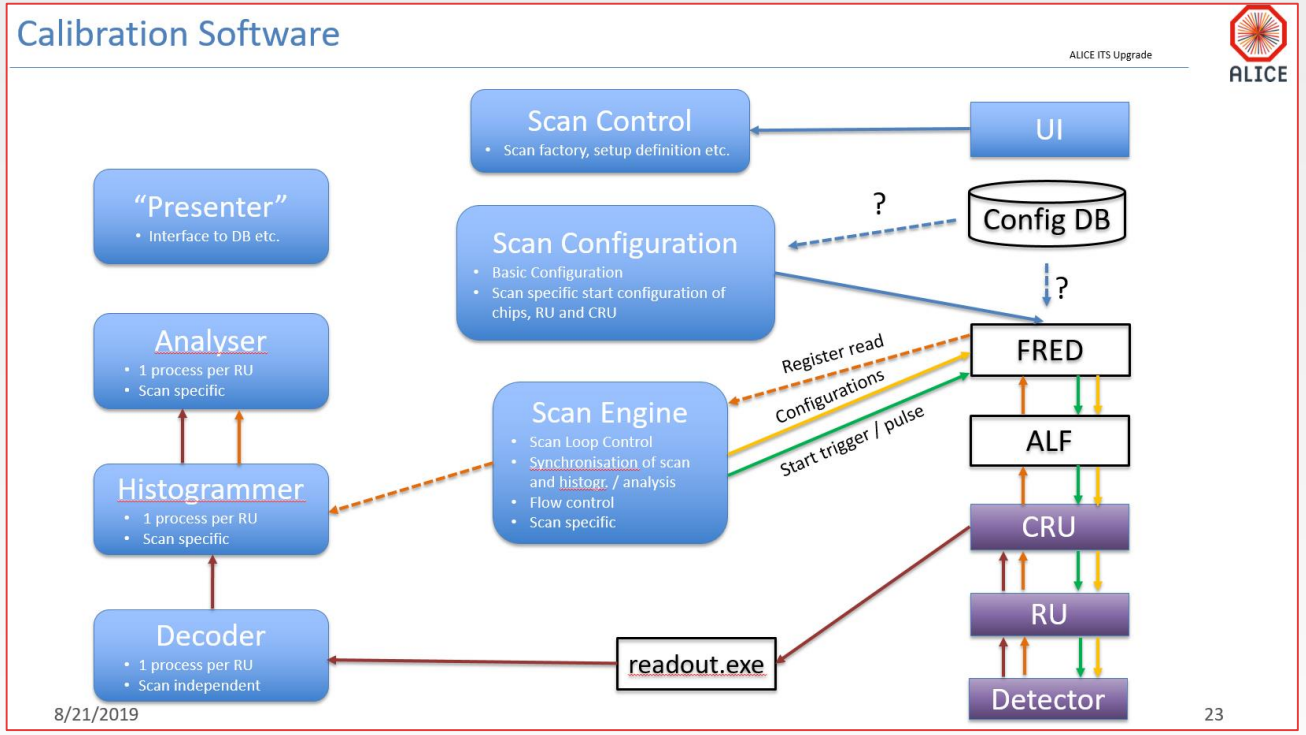
- ALPIDE Monitor Module
  - Sequencer/result memory for ALPIDE communication
  - Synchronized to send commands only in abort gaps
- CANbus Interface
  - Backup interface to RU/ALPIDEs if GBT-link is down.
- Wishbone to FIFO interface for fast uploading of files to Flash





Calibration Software

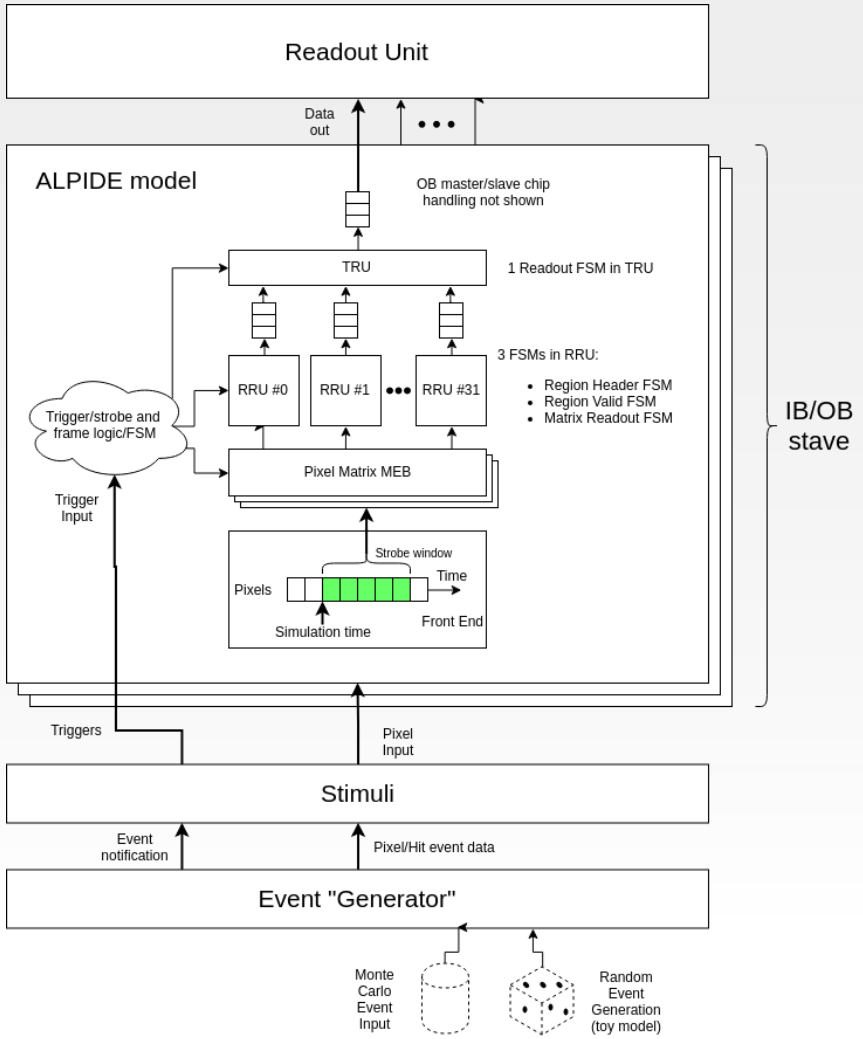
- Just involved in this project.
- Idea is to integrate/rewrite existing calibration tools (threshold scan etc) in deployed system
- These should be run during i.e. MDs to get information about the state of the detector (dead/noisy pixels etc).



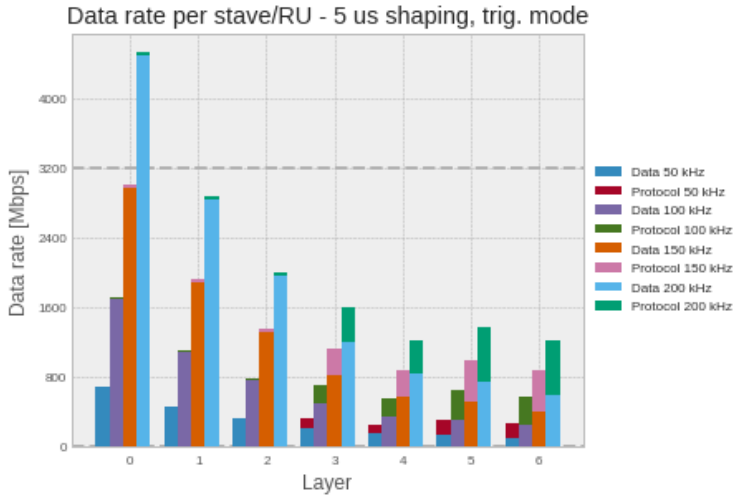
Markus Keil: https://indico.cern.ch/event/817544/

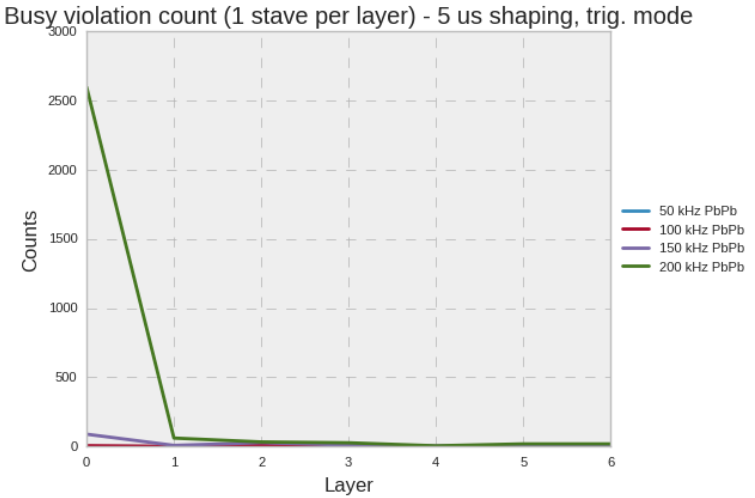
ITS System Simulations

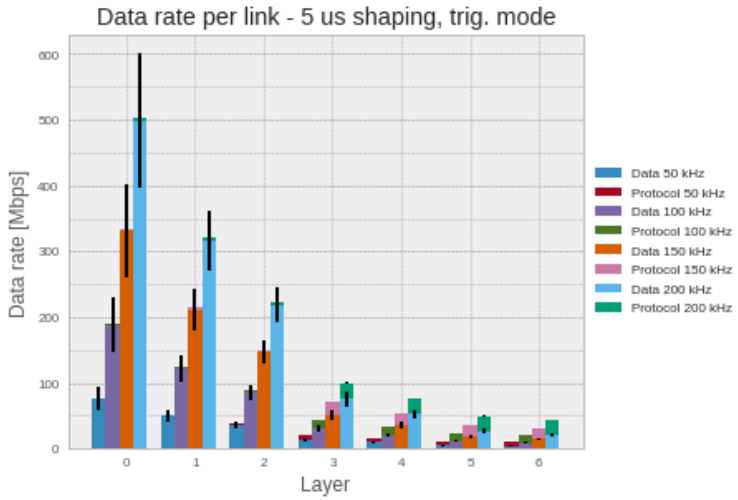
- Simulation model written in C++/SystemC
- Abstract model of ALPIDE, relatively accurate model of readout FSMs/logic
- Can simulate ITS/ALPIDE under various conditions
- Has also been used for:
  - pCT
  - FoCAL

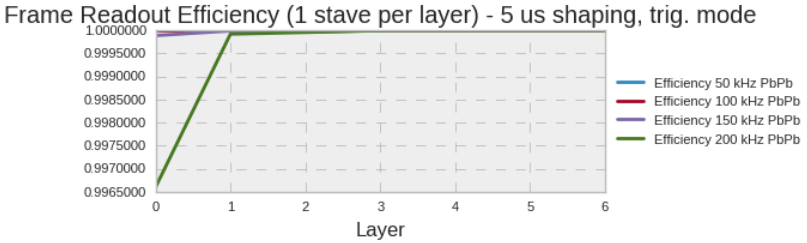


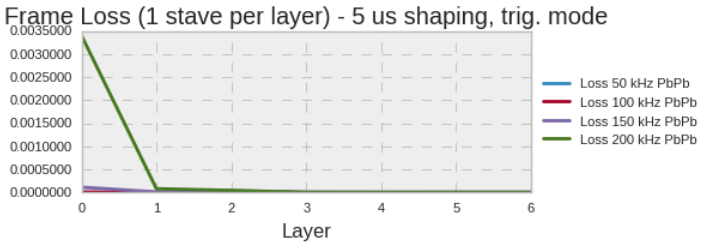
Simulation results – PbPb







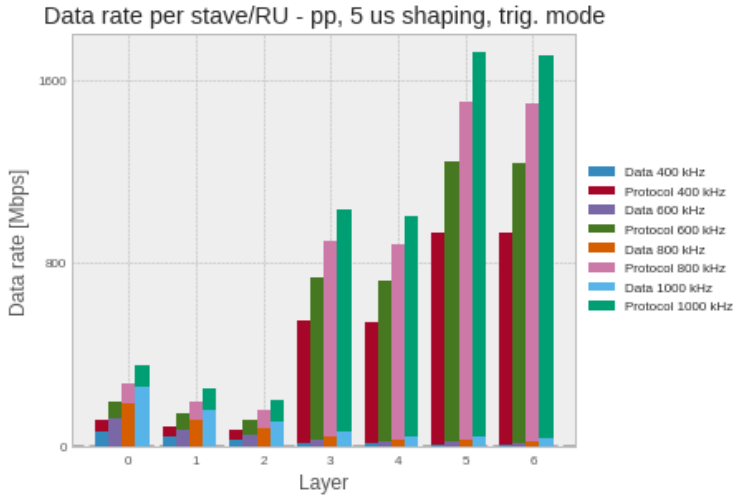


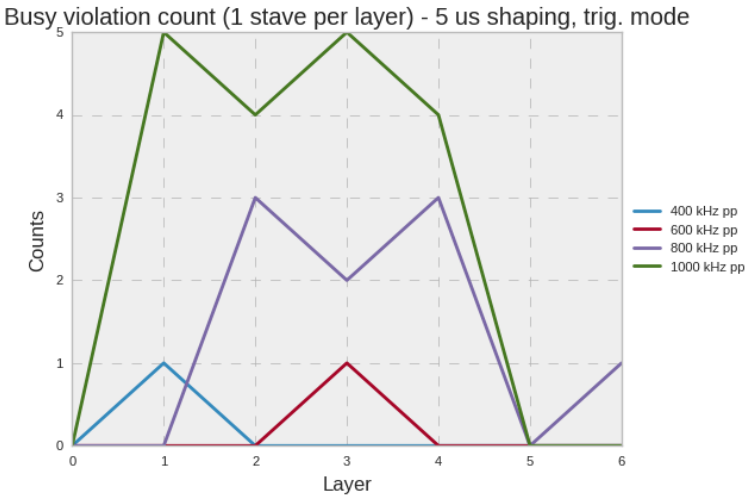


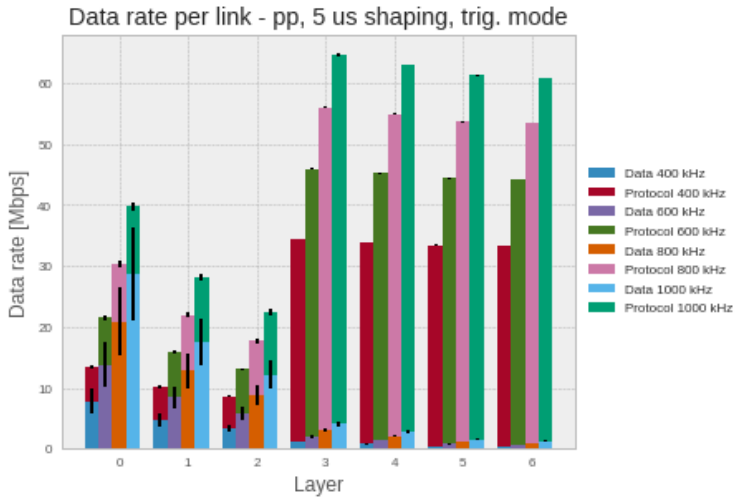
- Triggered mode
- 100k events simulated
- MC event input (generated with AliRoot)

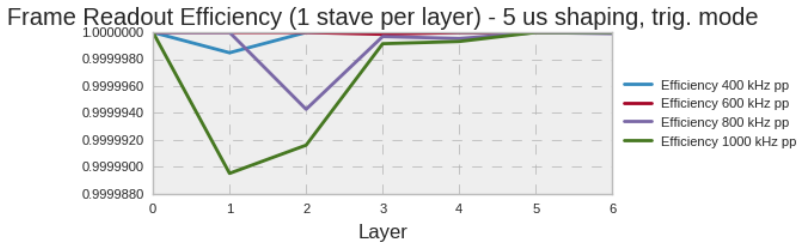
- (Seems a bit too optimistic currently.. Will have to check events/re-run simulations)

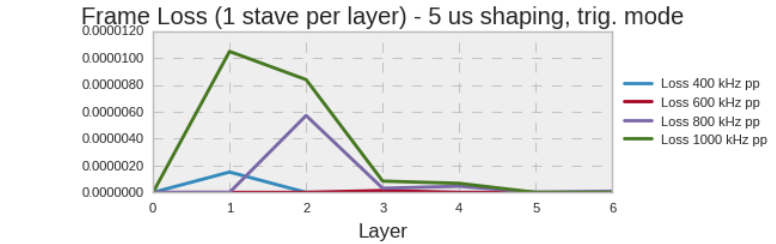
Simulation results – pp











- Triggered mode
- 100k events simulated
- MC event input (generated with AliRoot (Pythia))

- (Seems a bit too optimistic currently.. Will have to check events/re-run simulations)

Where do we go from here?

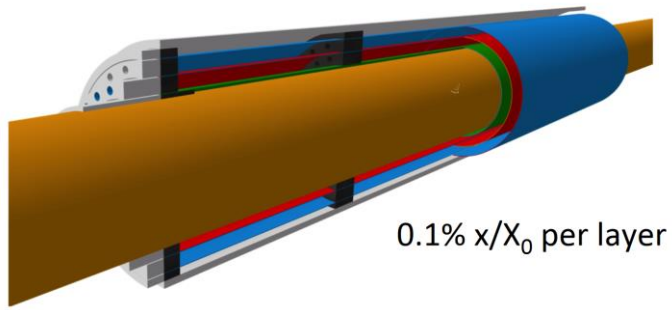
A next-generation LHC heavy-ion experiment

List of authors in appendix

Abstract

The present document discusses plans for a compact, next-generation multi-purpose detector at the LHC as a follow-up to the present ALICE experiment. The aim is to build a nearly massless barrel detector consisting of truly cylindrical layers based on curved wafer-scale ultra-thin silicon sensors with MAPS technology, featuring an unprecedented low material budget of 0.05% X_0 per layer, with the innermost layers possibly positioned inside the beam pipe. In addition to superior tracking and vertexing capabilities over a wide momentum range down to a few tens of MeV/*c*, the detector will provide particle identification via time-of-flight determination with about 20 ps resolution. In addition, electron and photon identification will be performed in a separate shower detector. The proposed detector is conceived for studies of pp, pA and AA collisions at luminosities a factor of 20 to 50 times higher than possible with the upgraded ALICE detector, enabling a rich physics program ranging from measurements with electromagnetic probes at ultra-low transverse momenta to precision physics in the charm and beauty sector.

Truly cylindrical vertex detector



0.1% x/X_0 per layer