

# SiW ECAL Studies for FCC-hh and Their Implications for FCC-ee



P. Allport<sup>1</sup>, S. Benhammadi<sup>2</sup>, R. Bosley<sup>1</sup>, J. Dopke<sup>2</sup>, S. Flynn<sup>1</sup>, N. Guerrini<sup>2</sup>, L. Gonella<sup>1</sup>, I. Kopsalis<sup>1</sup>, K. Nikolopoulos<sup>1</sup>, P. Phillips<sup>2</sup>, T. Price<sup>1</sup>, A. Scott<sup>2</sup>, I. Sedgwick<sup>2</sup>, E.G.Villani<sup>2</sup>, M. Warren<sup>3</sup>, N. Watson<sup>1</sup>, F. Wilson<sup>2</sup>, A. Winter<sup>1</sup>, S. Worm<sup>1</sup>, Z. Zhang<sup>2</sup>

<sup>1</sup>School of Physics and Astronomy, University of Birmingham, United Kingdom

<sup>2</sup>STFC Rutherford Appleton Laboratory, Didcot, United Kingdom

<sup>3</sup>Department of Physics and Astronomy, University College London, United Kingdom

## 3<sup>rd</sup> FCC Physics and Experiments Workshop (CERN, 16/01/2020)

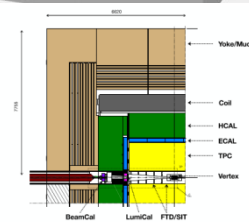
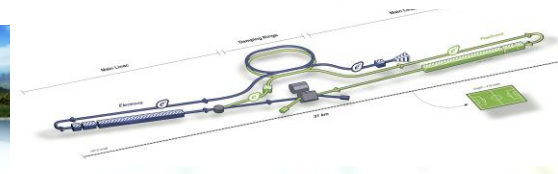
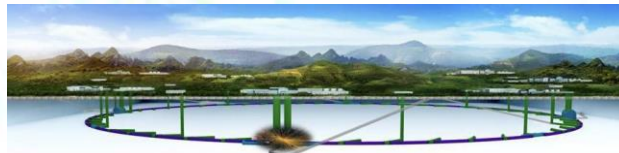
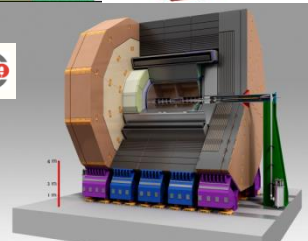
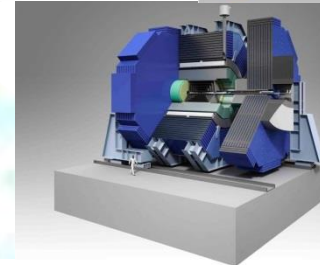
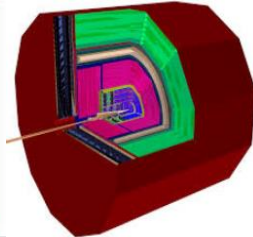
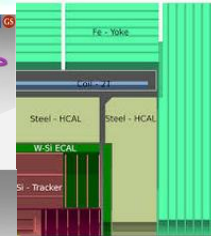
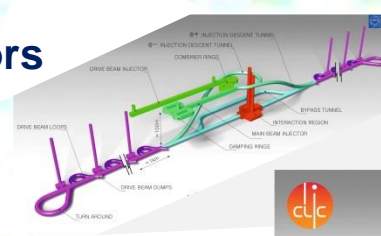
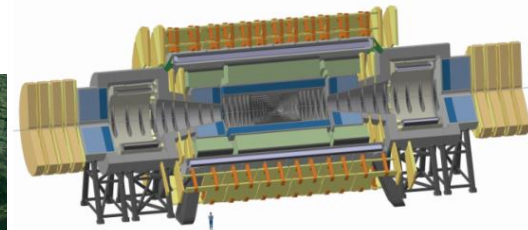
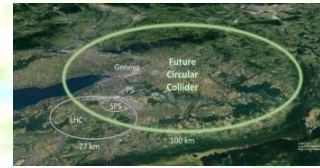
### • Introduction

- Historical Perspective
- Silicon - Tungsten\Lead Calorimetry
- Performance Simulation
- CMOS Monolithic Active Pixel Sensors
- ALICE FOCAL Beam Tests

### • Prototype CMOS Sensor Design

- Reconfigurable MAPS Concept
- Layout and Design
- Device Performance

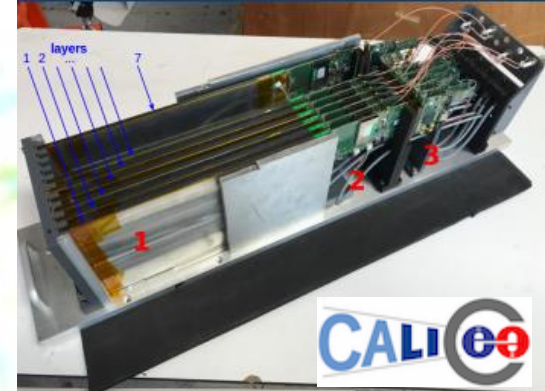
### • Conclusions and Observations



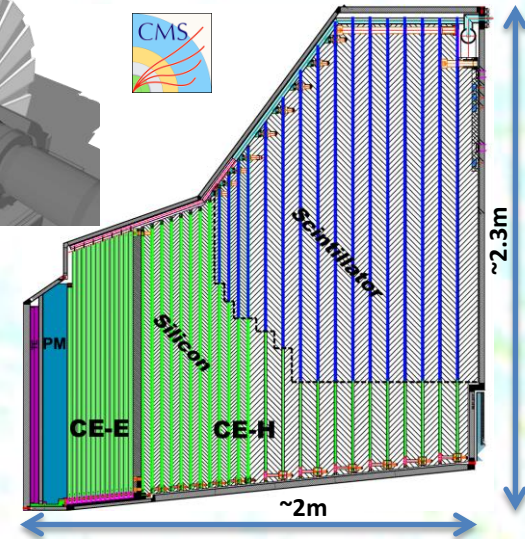
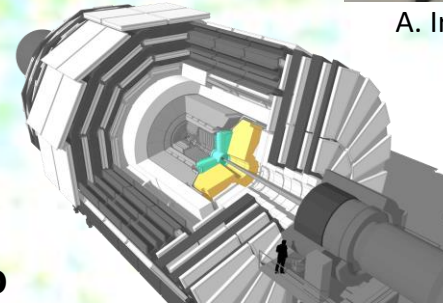
- The concept of SiW (or SiPb) calorimetry has long been under consideration as a possible option within the CALICE collaboration as offering unprecedented granularity for PFA and has been the focus of extensive prototyping and test beam activities

➤ See other presentations in this session

- For high radiation environments, CMS has developed the High Granularity Calorimeter (HGCAL) as the upgrade path for their forward calorimetry at HL-LHC
- The HGCAL will have  $\sim 600\text{m}^2$  of silicon sensors ( $\sim 500\text{m}^2$  of scintillators) with 6M Si channels, 0.5 or 1.1  $\text{cm}^2$  cell size and overall  $\sim 27000$  silicon modules
- The ECAL has 28 layers with Si + Cu/CuW/Pb absorbers giving 26  $X_0$  and  $\sim 1.7\lambda$



A. Irlles et al. Arxiv:1902.00110

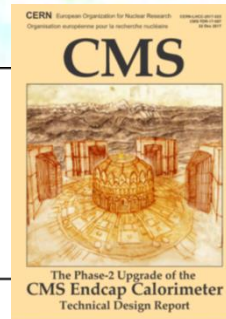


D. Barney, <https://indico.cern.ch/event/718124/>

1.3, 1.4 Silicon sensors and modules

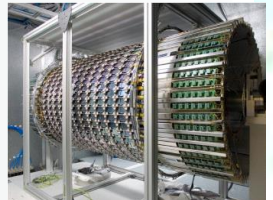
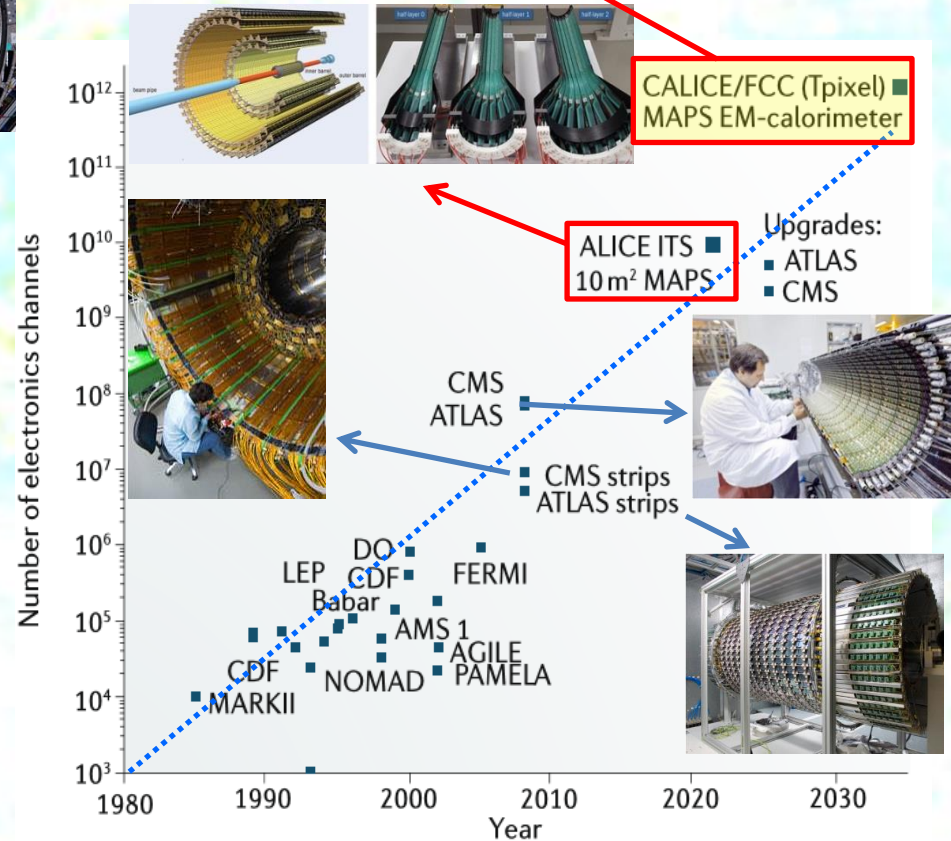
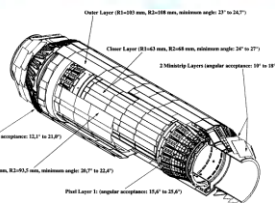
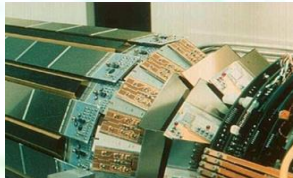
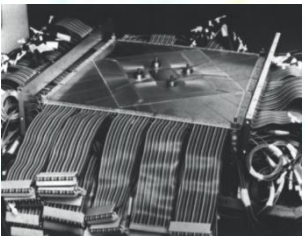
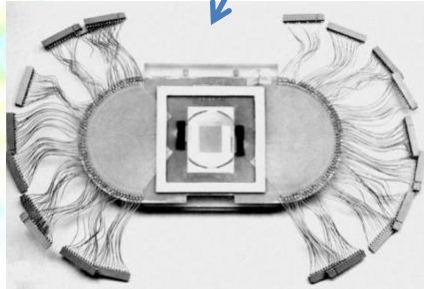
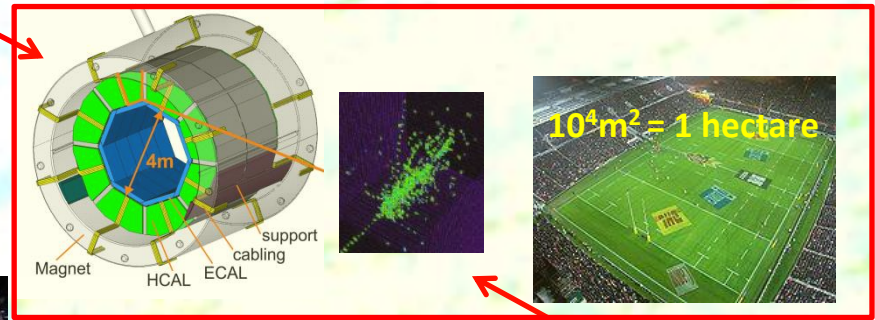
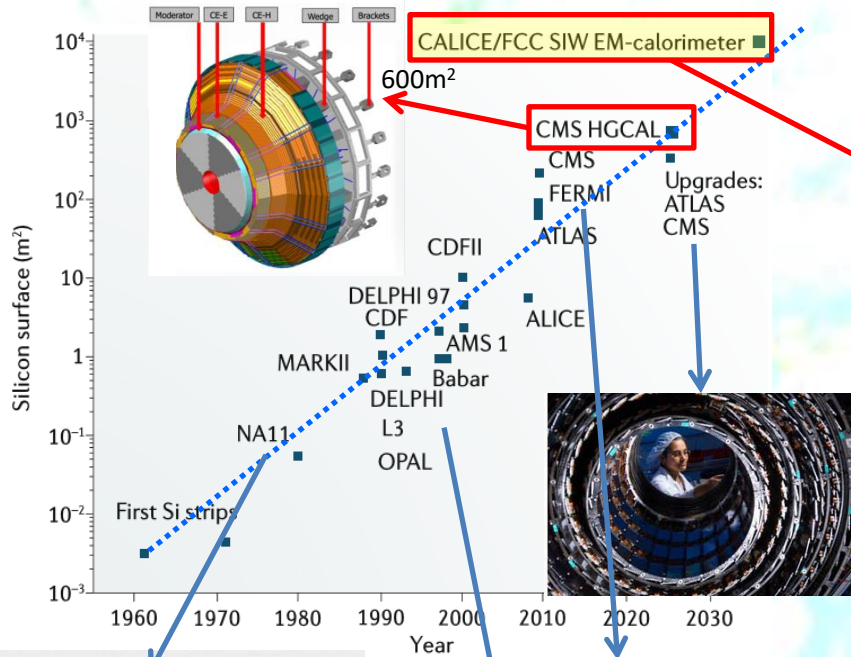
- Silicon module costs  $\sim 4\text{CHF/cm}^2$

GRAND TOTAL



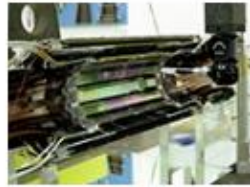
26 514  
67 153

# Historical Development of Silicon Sensor Arrays



Many different silicon detector technologies for particle tracking have been developed over the last four decades.

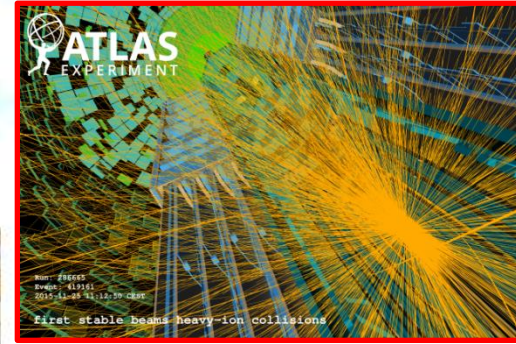
- Silicon strips
- Multiplexing ASICs
- CCDs



DELPHI



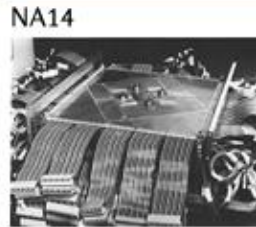
CDF



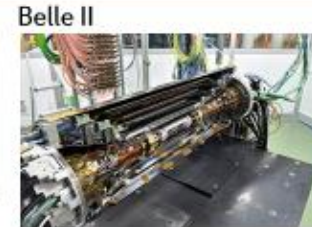
- CMOS MAPS
- Silicon-on-insulator pixels
- Vertical 3D integration



CMS



- Hybrid planar pixels
- Drift detectors
- DEPFET
- Hybrid 3D pixels



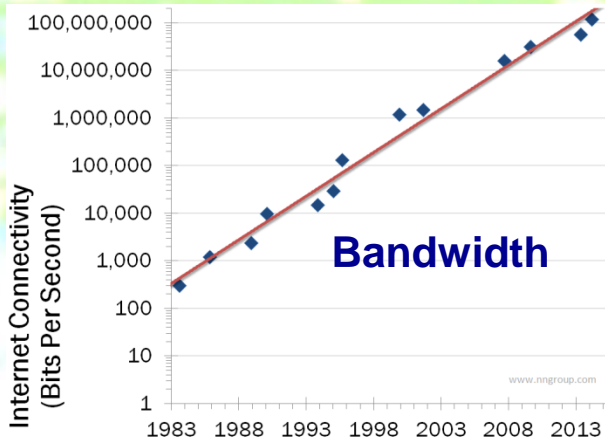
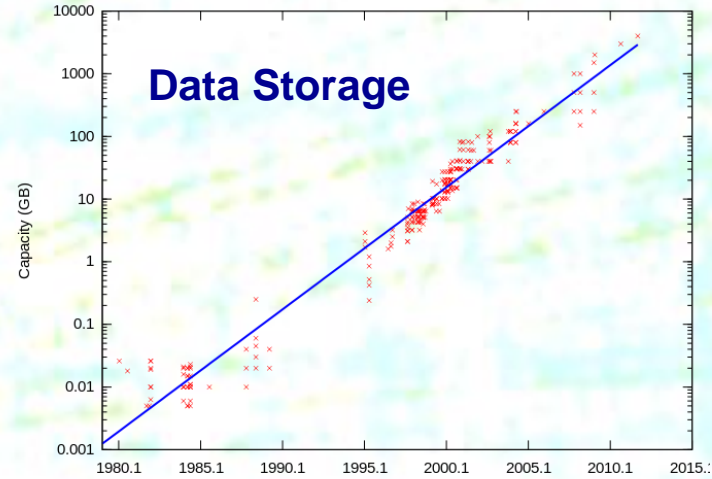
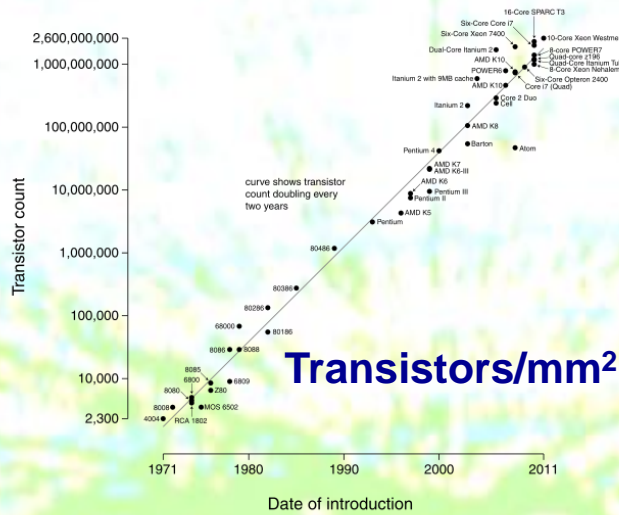
- Depleted MAPS
- Fast-timing detectors
- Hybrid MAPS

Applications of silicon strip and pixel-based particle tracking detectors - Nature Reviews Physics - <https://doi.org/10.1038/s42254-019-0081-z> Allport2019ER

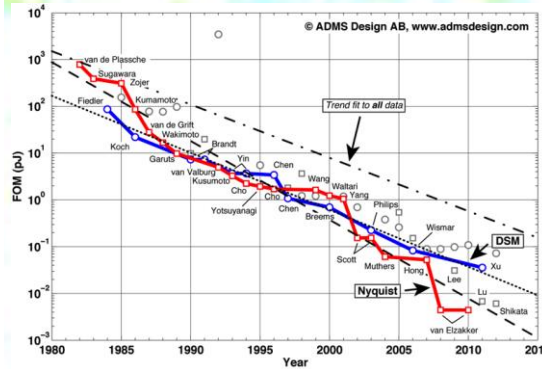
What is remarkable is that **every decade** the instrumented areas have increased by a **factor of 10** while the numbers of channels in the largest arrays have increased by a **factor of 100**.

**This despite other specifications for readout speed, spatial resolution, reduced multiple scattering (minimal total material including cooling and services) and radiation hardness also becoming much more demanding**

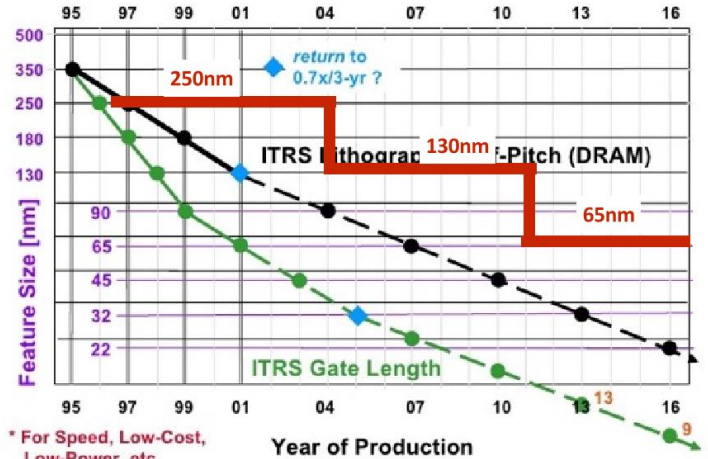
Microprocessor Transistor Counts 1971-2011 & Moore's Law



**ADC pJ/conversion**



**Scaling -- Traditional Enabler of Moore's Law\***



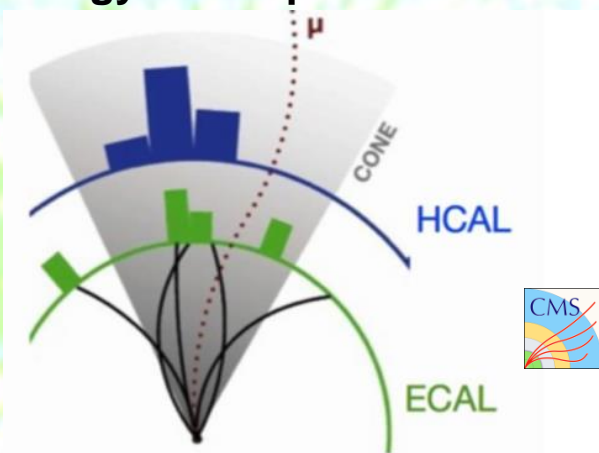
Historically showed doubling times of < 2 years but now slowing.

However, particle physics lags significantly behind commercial state-of-the-art because of additional constraints

F Faccio: <https://indico.cern.ch/event/468486>

# Particle Flow Calorimetry (PFA)

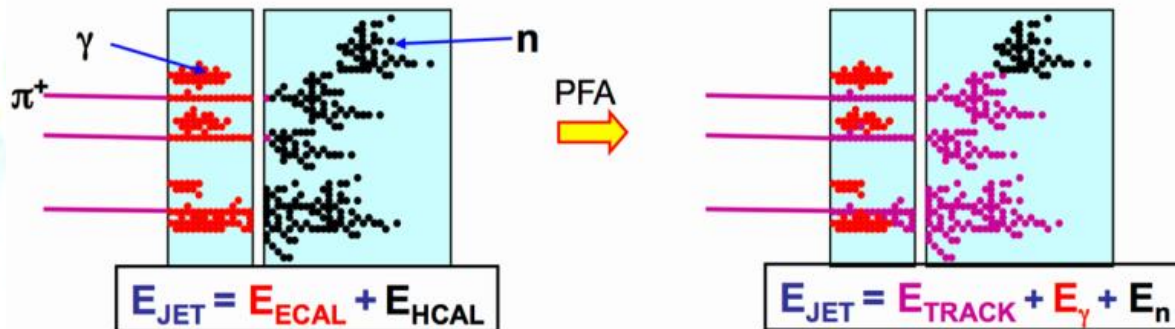
- Concept of a high granularity calorimeter with PFA capabilities widely studied as an option for calorimetry both for  $e^+e^-$  (see other presentations in this session) and hadron colliders (see for example EP Seminar <https://indico.cern.ch/event/718124/>)
- In the HL-LHC/FCC-hh context, improving calorimetry targets multi-jet final states, missing energy and separation of heavy bosons in hadronic decays



“Typical” jet:

- ~62% charged particles (mainly hadrons)
- ~27% photons
- ~10% neutral hadrons
- ~1% neutrinos

- Idea of PFA is to measure each individual particle in a jet using the detector system that provides best energy/momentum determination for that particle type.

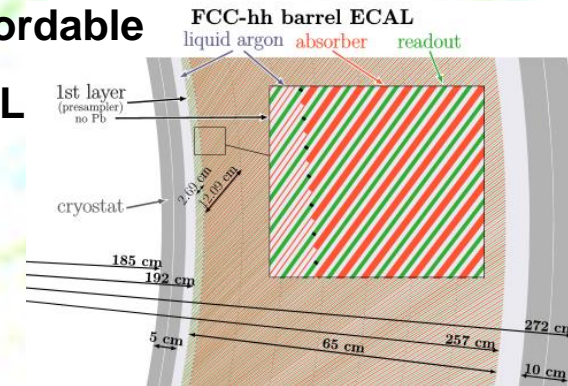


# SiW ECAL CMOS MAPS Motivation



- CMS HGCal silicon costs  $\sim 4\text{CHF}/\text{cm}^2$  would still need to come down even more for many thousand  $\text{m}^2$  ( $\gg 10^7\text{cm}^2$ ) array to become affordable

- NB partially mitigated by cost savings from reducing ECAL thickness for FCC-hh to  $< 20\text{cm}$  and removing need for cryostat with respect to LAr. (Reduces total cost of HCal, magnet system and muon spectrometer)



11th FCC - ee Workshop — M. Aleksa

- Excellent PFA capabilities but difficult to match LAr for radiation-hardness and EM energy resolution
- For a hybrid silicon system (such as the HGCal), at some stage the price of polished high- $\rho$  wafers could set a lower limit to what overall costs might be possible with separate thick depleted silicon substrate (but other options may exist)
- Alternatively, CMOS Imaging Sensors represent a  $\sim 20\text{B}\$$  business internationally (<https://www.marketsandmarkets.com/Market-Reports/cmos-image-sensor-market-252212367.html>) and market expected to continue growing rapidly driving down prices for such detectors
- Although current CMOS sensor array (such as for ALICE ITS Monolithic Active Pixel Sensor) cost estimates can currently be  $\sim$ ten times\* those for CMS HGCal, expect prices will be much lower for larger orders and as a function of time, while integration of electronics within the sensor also reduces cost of full system \* A. Andreazza this morning
- Prototypes (see below) demonstrate concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to  $> 10^{15}\text{n}_{\text{eq}}/\text{cm}^2$

R COLLIDER (FCC) STUDY PUBLISHED ITS CONCEPTUAL DESIGN REPORT IN JANUARY 2019, DESCRIBING TANTALIZINGLY MORE POWERFUL PARTICLE COLLIDERS FOR THE POST-LHC PARTICLE PHYSICS.

**Count pixels above threshold within each 5mm×5mm pad**

RO WORK GET A COPY PRESS KIT

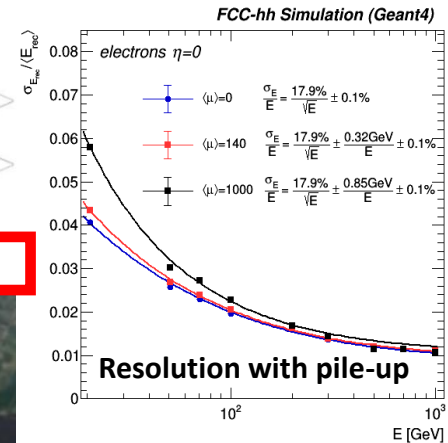
Conceptual Design Report Volumes

FCC LEPTON COLLIDER **FCC HADRON COLLIDER** HIGH-ENERGY LHC

European Strategy Update Documents

INTEGRATED PROJECT FCC LEPTON COLLIDER FCC HADRON COLLIDER



5.1 Silicon Tungsten Calorimeter

5 Alternative Technology for the EM Barrel Calorimeter

FCC Week (1/6/17) T. Price

Abada, A., Abbrescia, M., AbdusSalam, S.S. et al. Eur. Phys. J. Spec. Top. (2019) 228: 755. <https://doi.org/10.1140/epjst/e2019-900087-0>

Idea initially in context of CALICE but then adapted to FCC-hh environment.

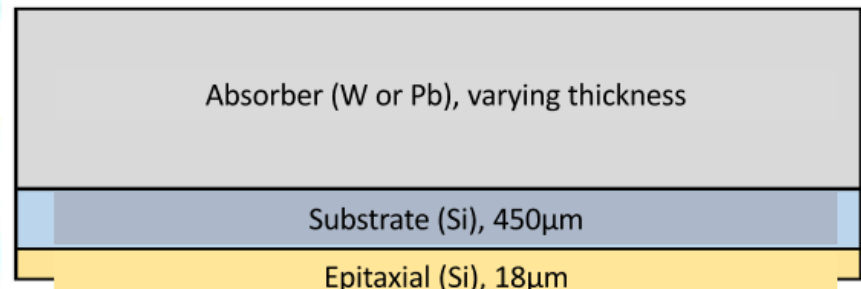
Simulated 4 different geometries:

30 Layers, 3.5mm W ( $30 \times 1.0 X_0$ )

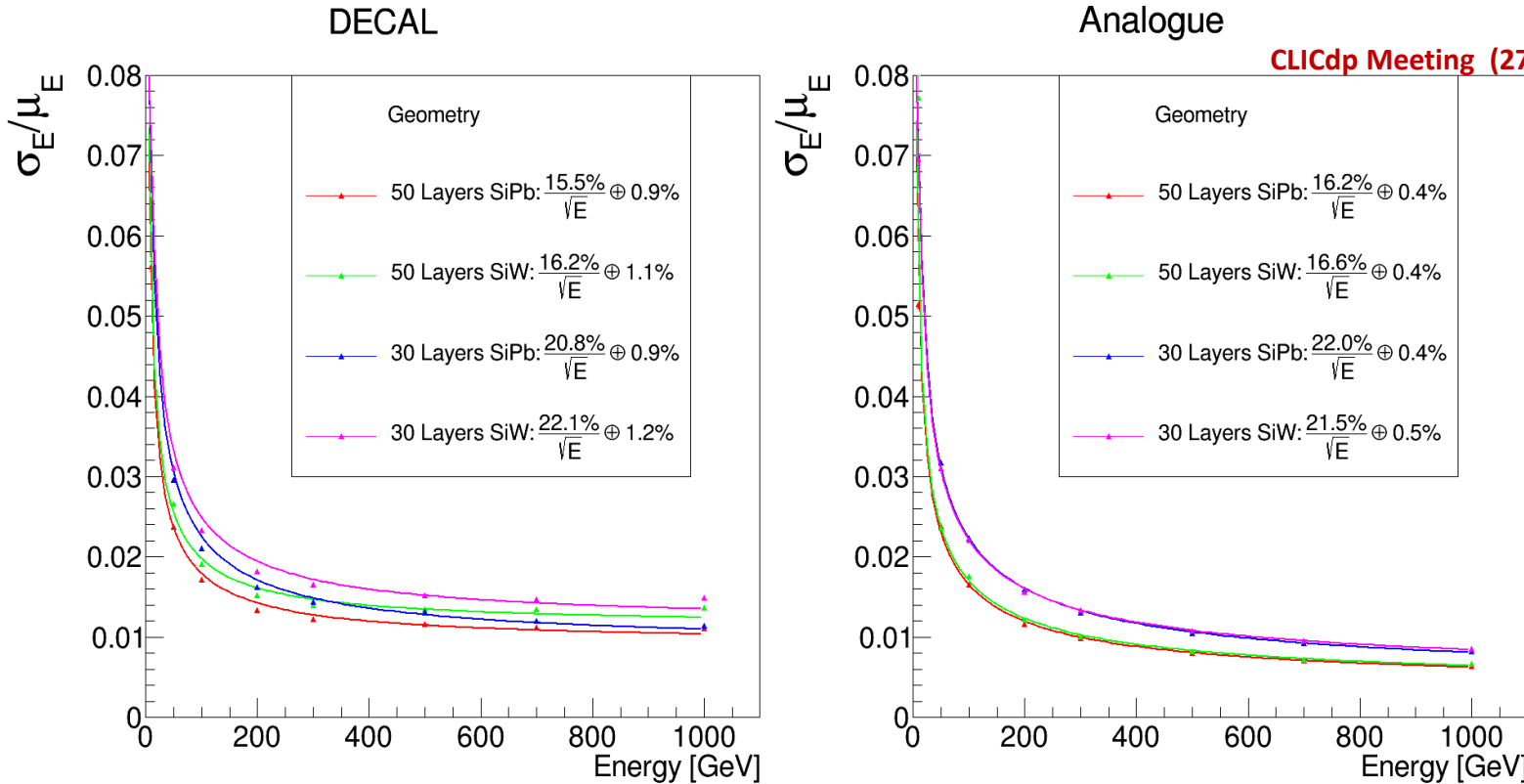
5.6mm Pb

50 Layers, 2.1mm W ( $50 \times 0.6 X_0$ )

3.4mm Pb





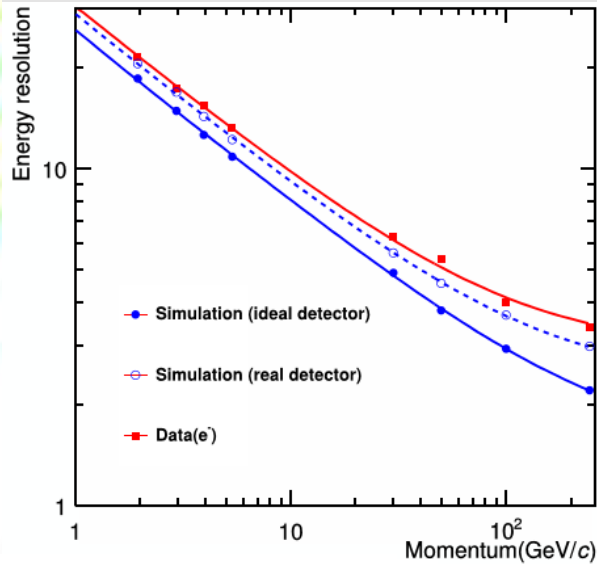
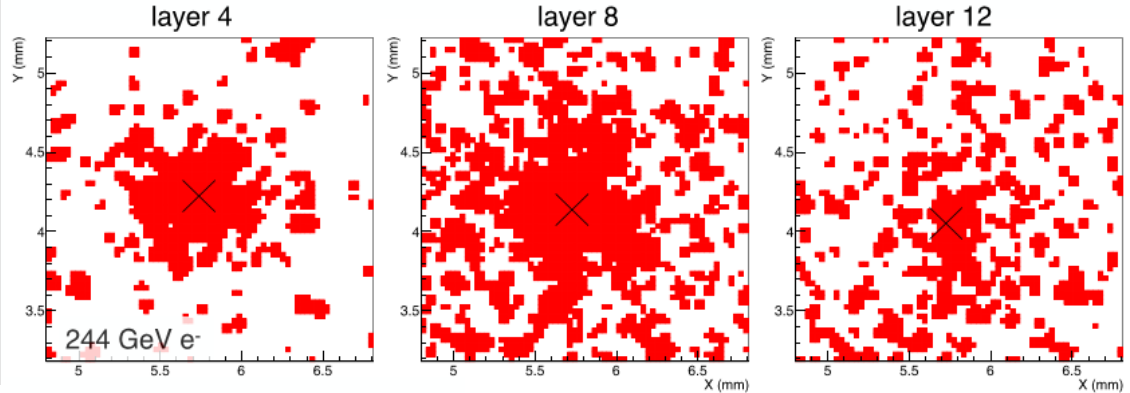
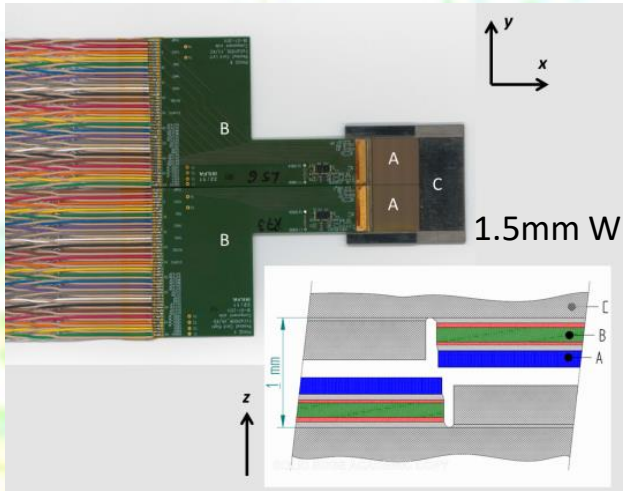


- For single electrons, similar performance of Digital ECAL (with realistic channel threshold per pixel of  $480e^*$ ) and Analogue ECAL (with perfect performance and full substrate signal per pad) up to around 300GeV (4T field without pile-up)
- Above this energy, saturation (more than one hit per  $50\mu\text{m} \times 50\mu\text{m}$  pixel) starts to impact performance of digital compared with analogue ECAL

*\* $6 \times \sigma$  assuming noise of  $\sigma = 80e$*

T. Peitzmann: International Workshop on Forward Physics and Forward Calorimeter Upgrade in ALICE (Tsukuba, 08.03.2019)

## 24 layer MIMOSA CMOS sensor calorimeter Si-W stack



$$\frac{\sigma_E}{E} = a \oplus \frac{b}{\sqrt{E/\text{GeV}}} \oplus \frac{c}{E/\text{GeV}}$$

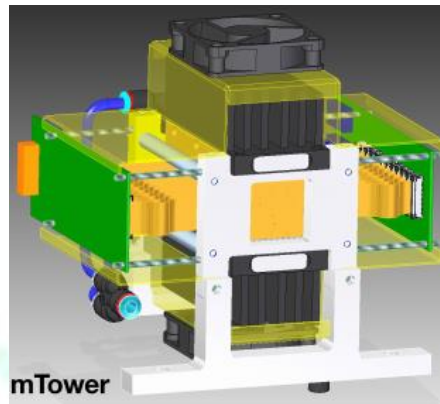
$$a = (2.95 \pm 1.65)\%$$

$$b = (28.5 \pm 3.8)\%$$

$$c = 6.3\%$$

**244 GeV electron: very high single particle hit rate in shower core**

**Good energy resolution but lower than simulations, particularly at higher energies**



**New ALPIDE CMOS sensor based 3cm×3cm area 24 layer stack**

**Looking forward to results from test-beams with this system**

# DECAL (4mm×4mm Array) Prototype Chip

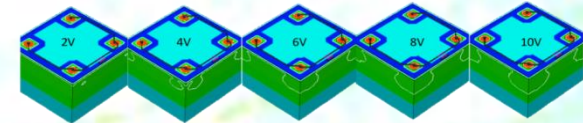
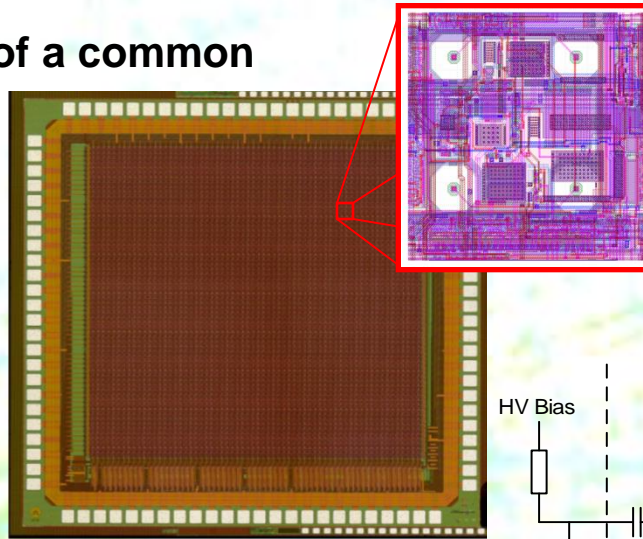


Concept in FCC-hh context of a common silicon development for:

- Outer tracking
- Pre-shower
- EM calorimeter

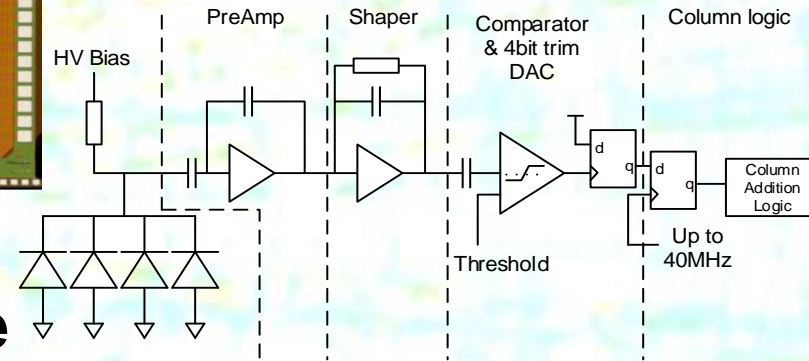
Reconfigurable sensor as:

- 5mm×50µm strips
- 5mm×5mm pad



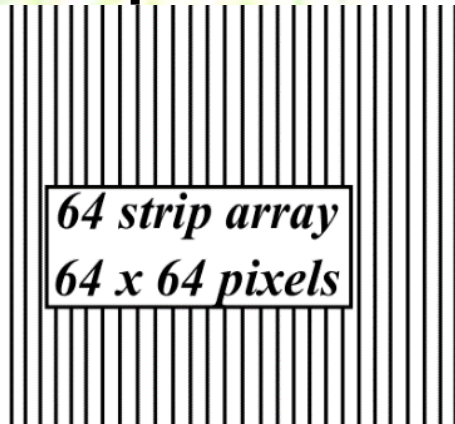
4 Diode TCAD Simulation: Giulio Villani

Prototype as proof of concept (180nm CMOS\*)



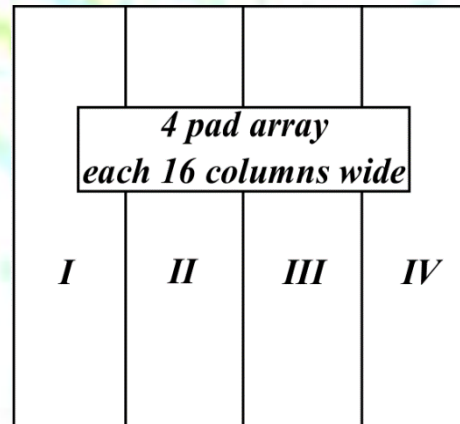
TWEPP (4/9/19) S.Benhammadi

## Strip mode



Information on up to 3 hits per column gives data rate 5.12Gb/s

## Pad mode

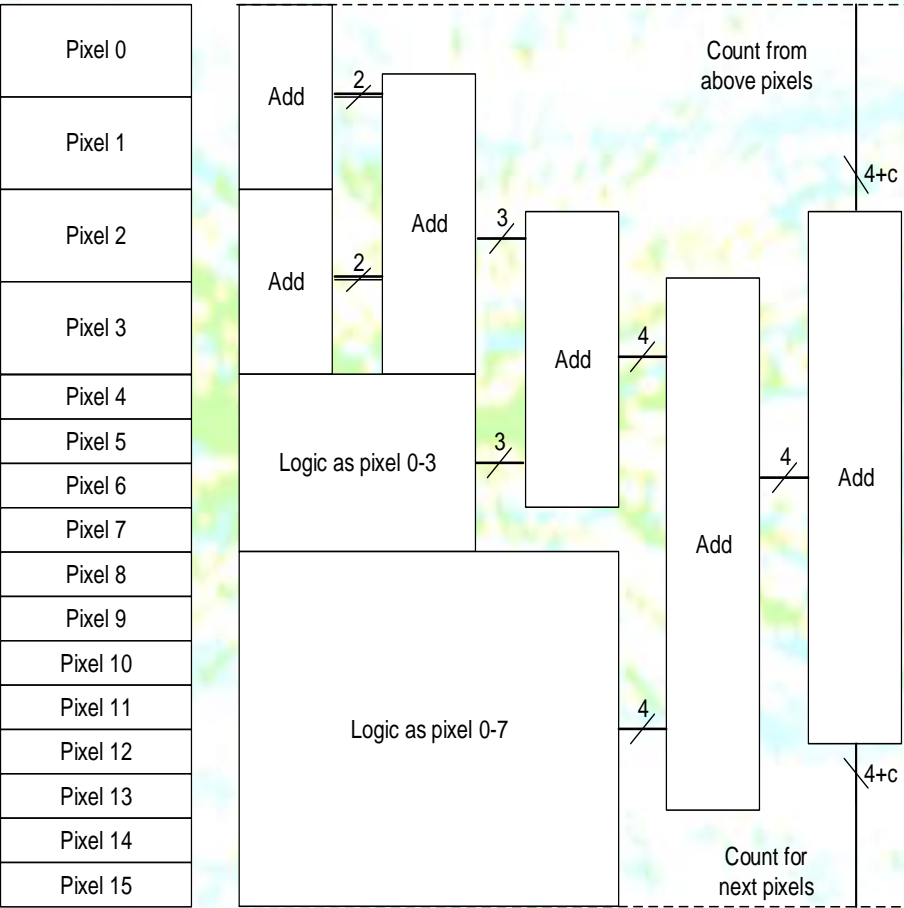
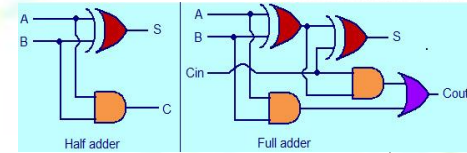


Information on up to 15 hits per column giving 240 hits per pad gives data rate of 2.56Gb/s

Specification	Unit	Value
Pixel Pitch	um	55
Resolution	pix	64 x 64
Frame Rate	MHz	40
Input Referred Noise	e- rms	80
Max hits/col (pad mode)	hits	15
Max hits/col (strip mode)	hits	3

**\*TowerJazz**  
(Small collecting node)

# DECAL- Summing Logic



**16 pixels are grouped together**

**For PAD mode:**

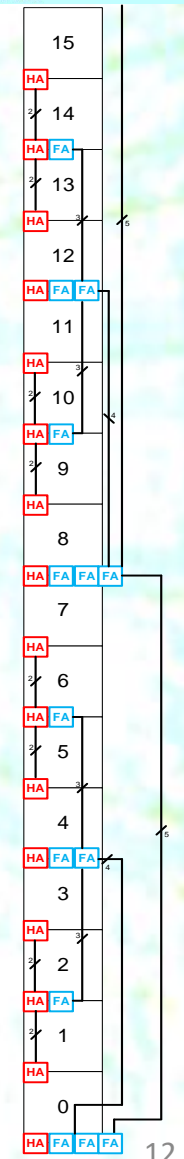
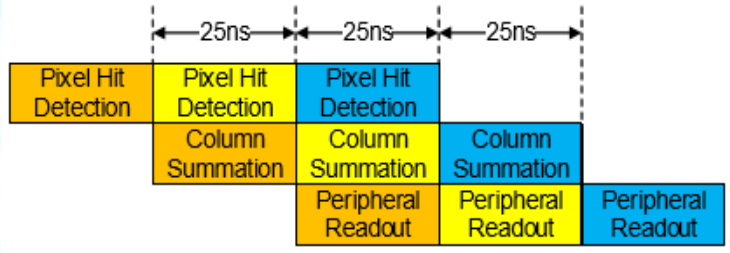
- 4 bits of data + carry (pad mode)

**For STRIP mode:**

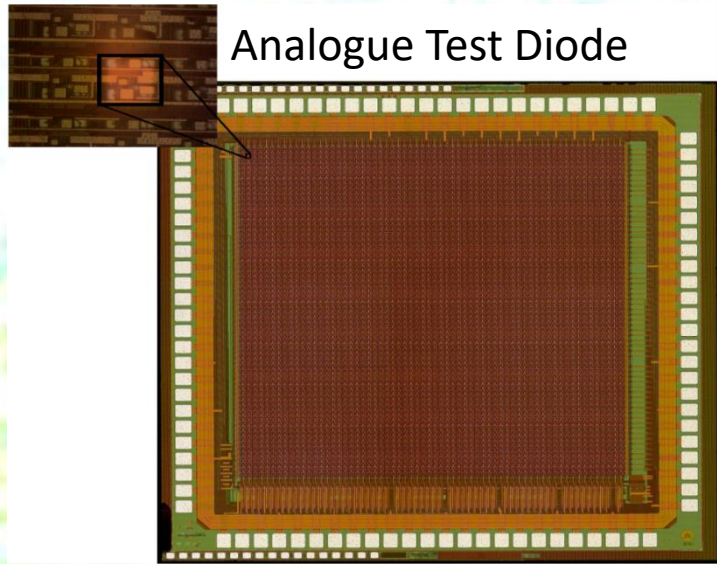
- only the 2 first bits of data used

**To achieve data rate of 40MHz  
column sum has to be complete  
within 25ns using fast logic**

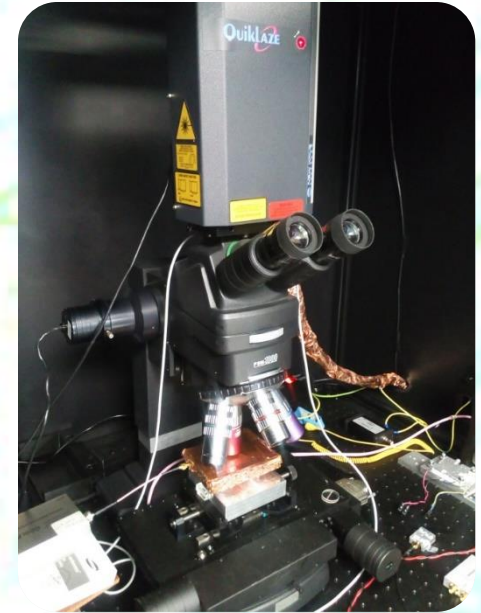
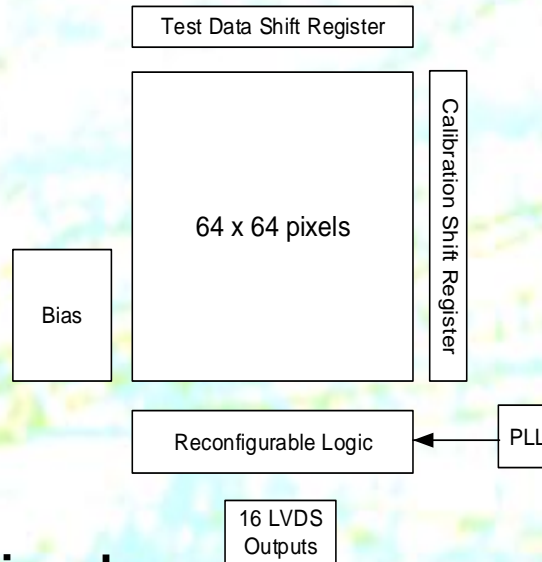
**(Approach should also have  
potential for lower power)**



# DECAL – Analogue Performance



Analogue Test Diode

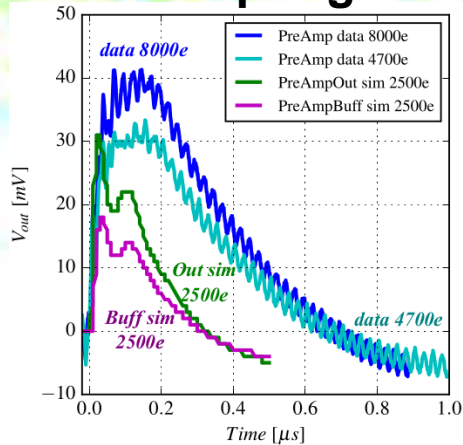


10x10 $\mu\text{m}^2$  TriLite laser (pJ/pulse,  $\lambda=1064$  nm)

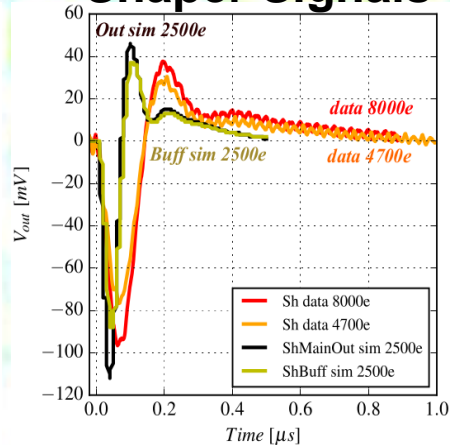
Estimate of injected charge in 18  $\mu\text{m}$  epitaxial layer of DECAL sensor uses measured signal in photodiode

Some delay in measured response time with respect to FE simulation (but expect ~10ns signal collection)

PreAmp Signals



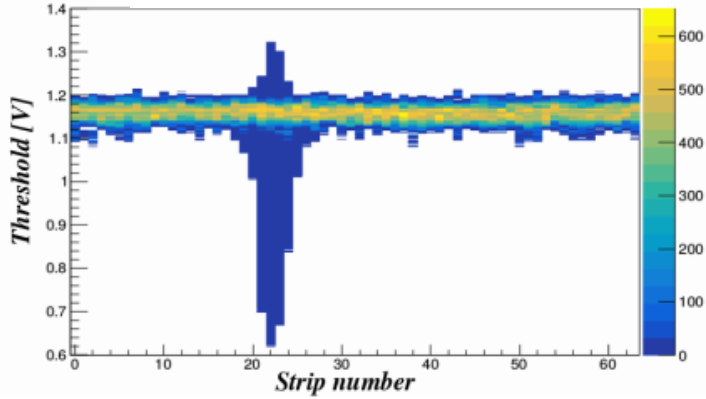
Shaper Signals



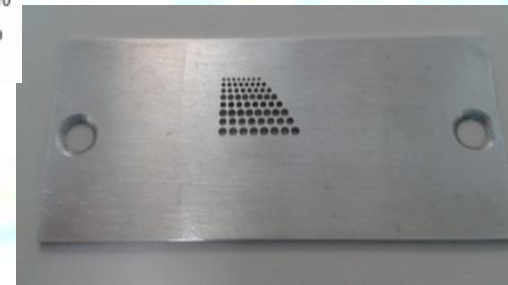
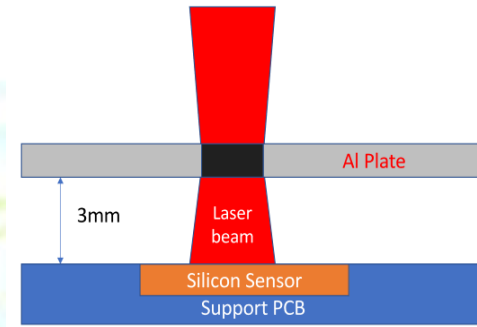
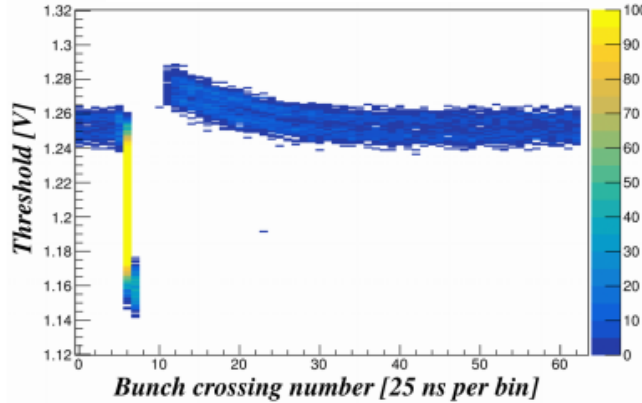
# DECAL Prototype: Laser Testing



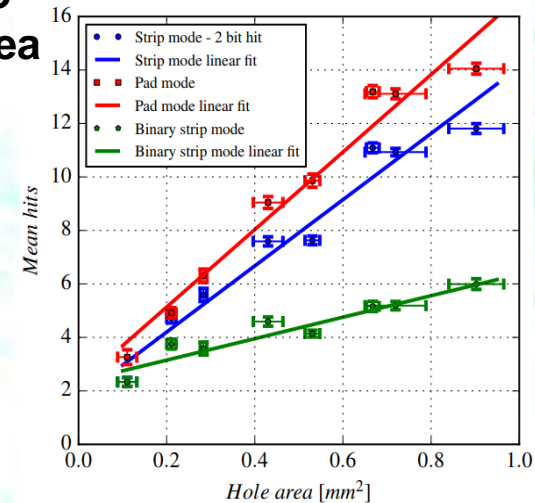
Threshold at which output of comparator first fires vs strip #



Single strip threshold at which comparator first fires vs time

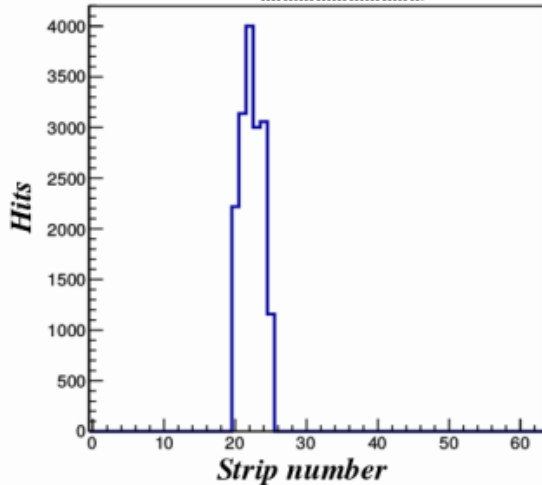


Check pad and strip mode response to different area light spots

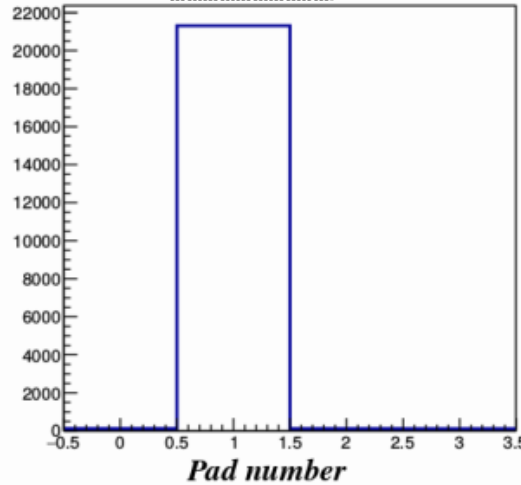


IEEE MIC-NSS (30/10/19) I. Kopsalis

Strip mode



Pad mode



Global threshold value of 1 V

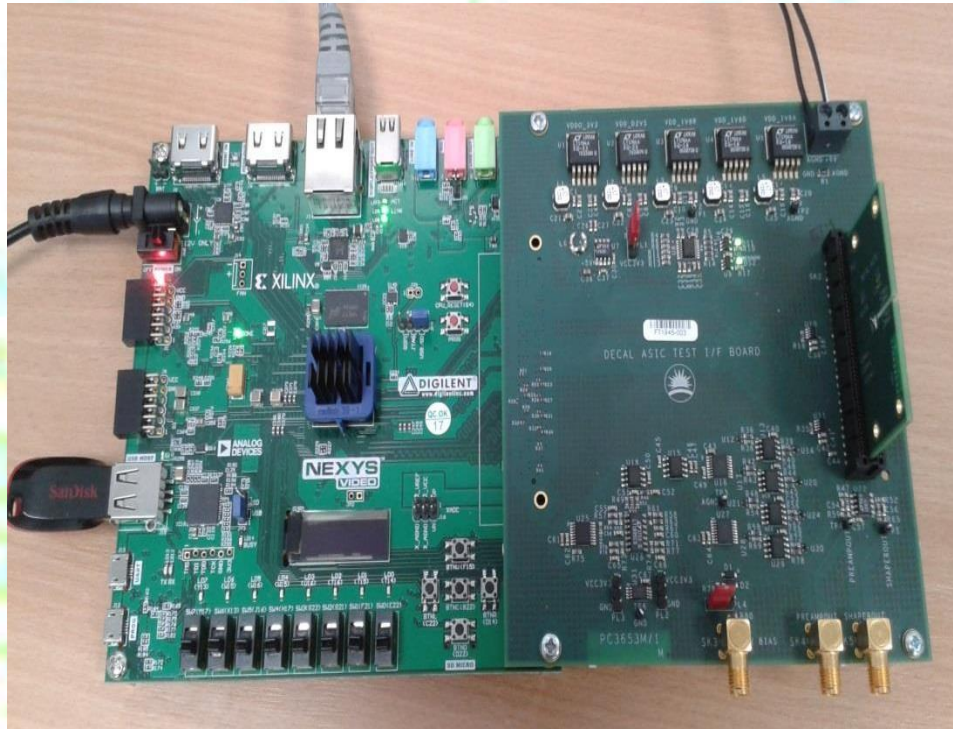
# Conclusions



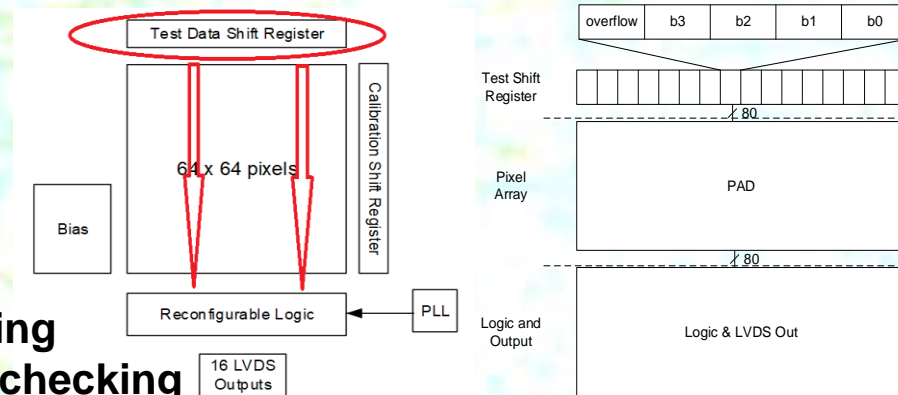
- **Si-W calorimetry should allow excellent PFA performance with a seamless transition from **outer tracking** → **pre-shower** → **ECAL** in potentially the same technology**
  - **For future Si-W (Si-Pb) calorimeters to be affordable, need silicon sensor costs to come down to ~ **CHF/cm<sup>2</sup>** (as **potential silicon areas are » 10<sup>7</sup>cm<sup>2</sup>**)**
  - **It could be that this becomes more achievable in CMOS Imaging Sensor technologies given the very large, fast growing commercial market and the overall system cost impact of integrating the front-end electronics with the sensor substrate**
  - **Power needs study (FCC-ee CMOS estimates range ~**50-100mW/cm<sup>2</sup>** (no pulsing) *Walter Snoeys and Auguste Besson, this meeting on Tuesday*) (cf **CMS HGCAL: ~200kW**)**
  - **A prototype developed which proves concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to > 10<sup>15</sup>n<sub>eq</sub>/cm<sup>2</sup> (Next step is to reprocess DECAL prototype taking advantage of these features)**
  - **Digital EM calorimetry also provides an excellent potential solution for future e<sup>+</sup>e<sup>-</sup> facilities with very fast charge collection which could also be useful for triggering**
  - **Aspects could also be employed with other calorimeter technologies, for example as high granularity pre-shower integrated with outer tracking layers**
  - **RD50 was **publishing** first results on irradiations in the p-type detector technologies currently being implemented for the HL-LHC ATLAS and CMS upgrade trackers in 2004**
- Require ~20 year lead-time for starting R&D targeting largest future systems**

# BACK-UP



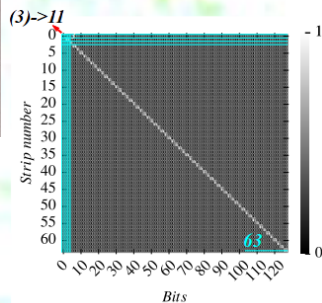


- DIGILENT NEXYS Video Board
- DECAL motherboard allows all the bias voltages and currents to be software controlled.
- Ethernet based readout using ATLAS ITSDAQ software and hardware.
- System allows readout at 40MHz

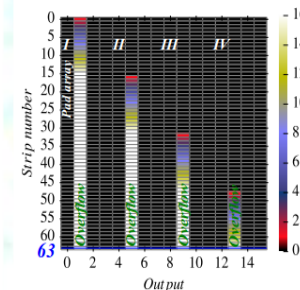
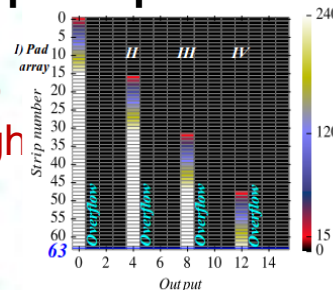


DECAL on Carrier Board

Simulate pixel output by placing data in test shift register and checking output is correct for both strip and pad mode



Pattern of 11'b clocked through in strip mode

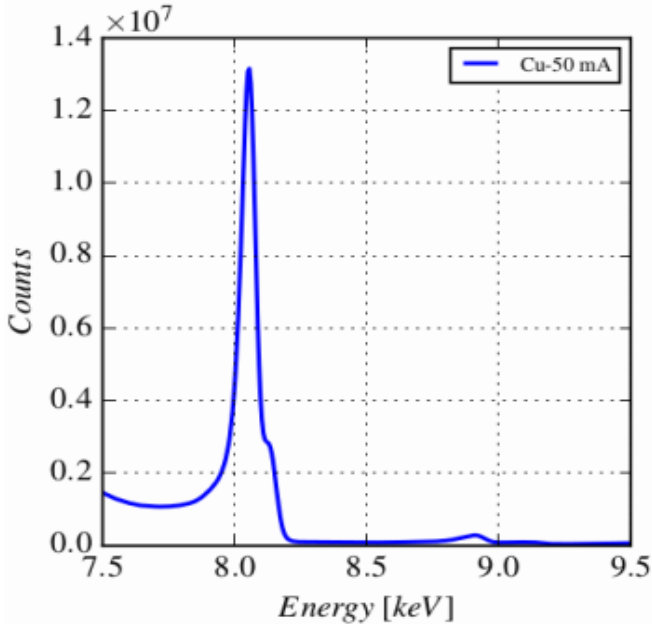


Patterns of 01111'b and 10000'b clocked in pad mode

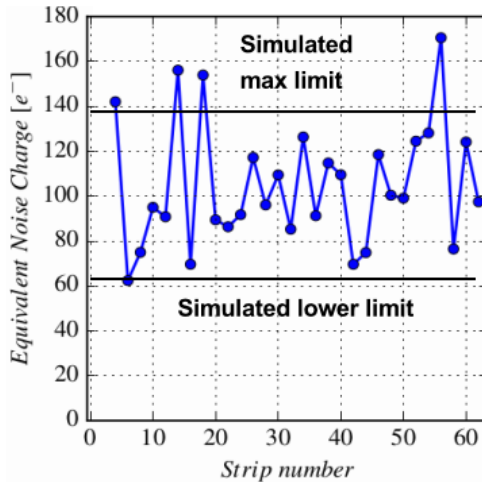
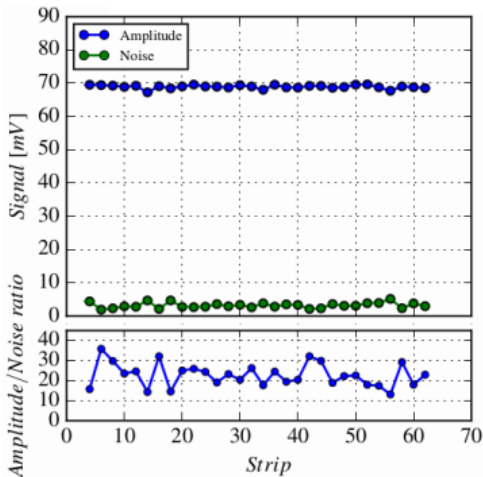
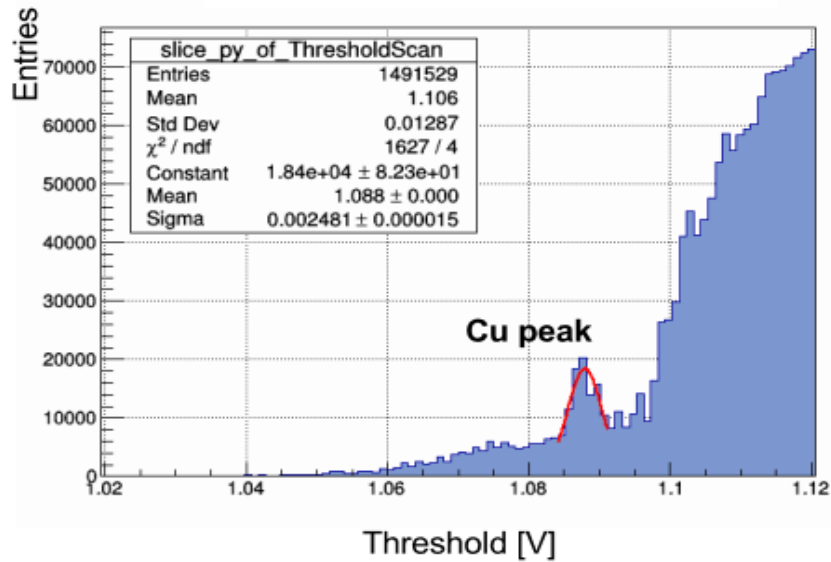
# DECAL Prototype: Cu $K_{\alpha}$ Calibration



Energy spectrum of Cu measured with RAL HEXITEC detector



Scan of single strip threshold at which comparator first fires



Expected signal:  $8050\text{eV} / 3.6\text{eV} = 2236e$

Taking width of fitted peak as estimator of noise gives  
Signal/Noise  $\approx 22$

**Noise  $\approx 100e$**

# Historical Development of Silicon Sensor Arrays



The highest channel count arrays are based on pixelated detectors. For **hybrid pixel sensors** connection to the electronics requires flip-chip technologies.

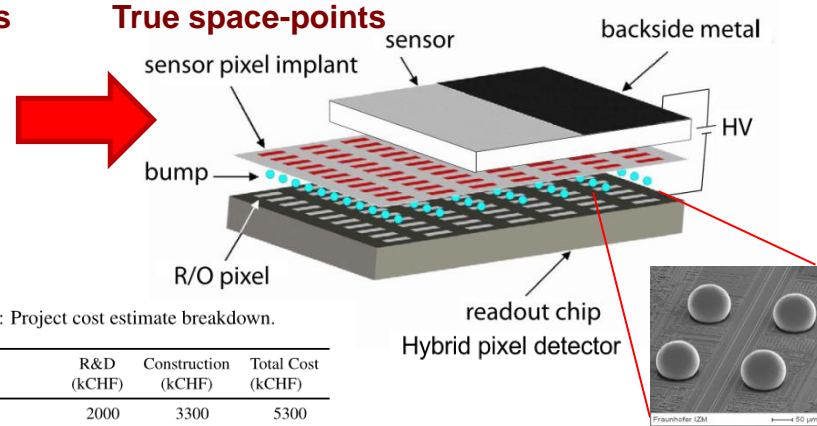
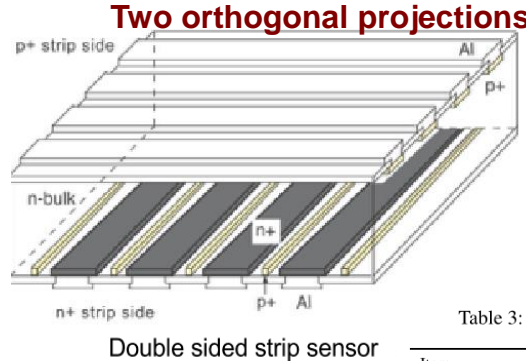
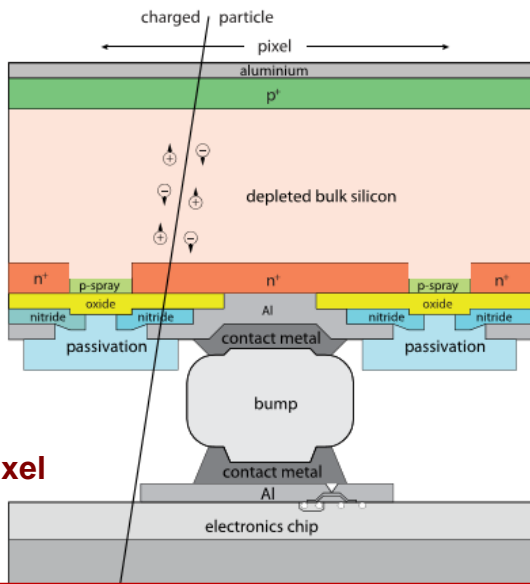
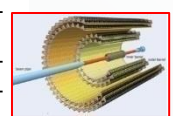


Table 3: Project cost estimate breakdown.

Item	R&D (kCHF)	Construction (kCHF)	Total Cost (kCHF)
Total	2000	3300	5300
Beampipe	600	900	1500
Pixel CMOS Sensors	700	700	1400
Sensor test	100	150	250
Thinning & dicing	200	300	500
Hybrid printed circuit	100	100	200
Mechanics	150	350	500
Assembly & test	50	200	250
Installation tooling	0	200	200
Air cooling	100	150	250
Services	0	100	100
Patch panels	0	150	150



**Monolithic Active Pixel Detectors**

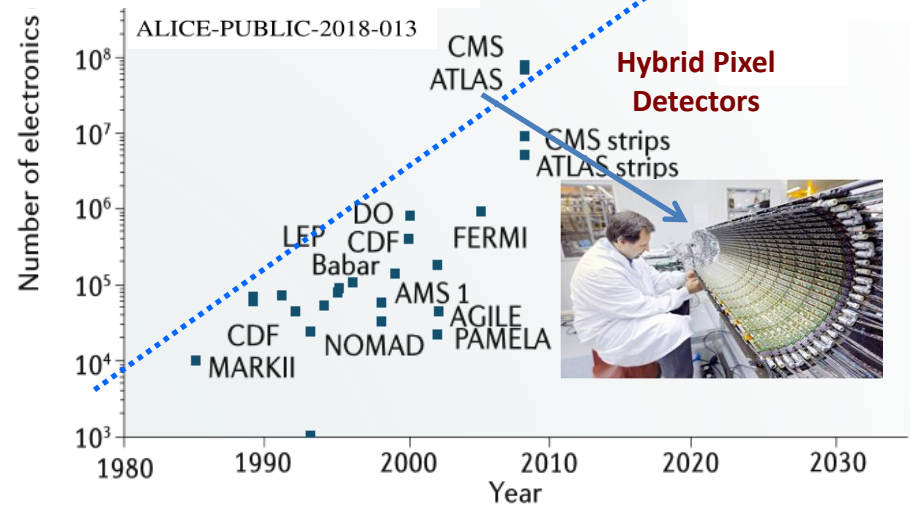


CALICE/FCC (Tpixel) ■  
MAPS EM-calorimeter

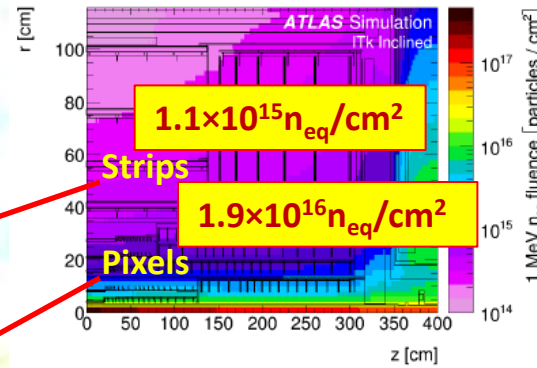
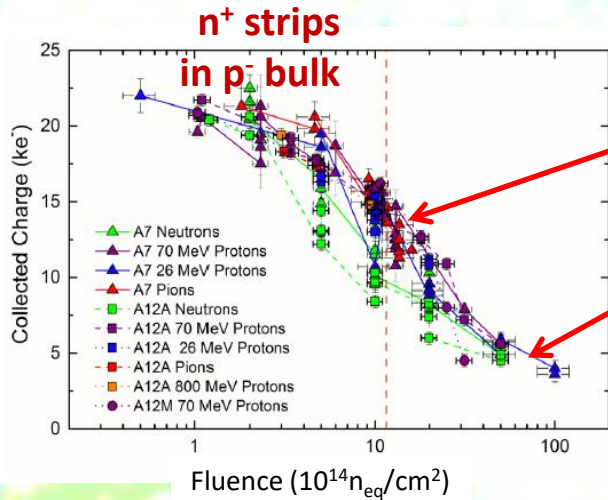
ALICE ITS ■  
10m<sup>2</sup> MAPS

Upgrades:  
ATLAS  
CMS

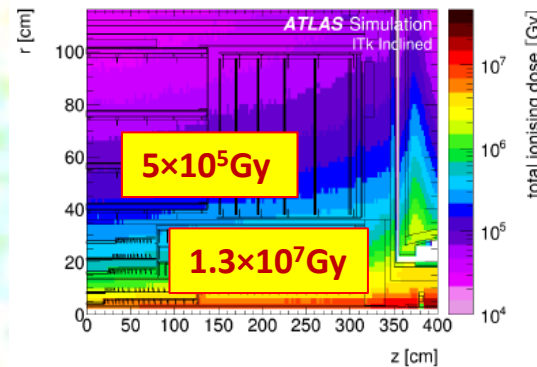
Minimum feature size	250nm	130nm	65nm
Example Read-out Hybrid Pixel Chips	ATLAS FE-13 CMS Medipix	NA62 TDCPix ATLAS IBL FE-14 LHCb VeloPix Medipix3RX TimePix3	CLICpix RD53A TimePix4
Typical hit data storage density capabilities	<1Gb/s/cm <sup>2</sup>	~5Gbp/s/cm <sup>2</sup>	40Gb/s/cm <sup>2</sup>
Output Bandwidth	40-160 Mb/s	0.3-1.2 Gb/s	2-20 Gb/s



- Hybrid silicon detectors (pixels/strips) **signal** output drops with irradiation to very high doses



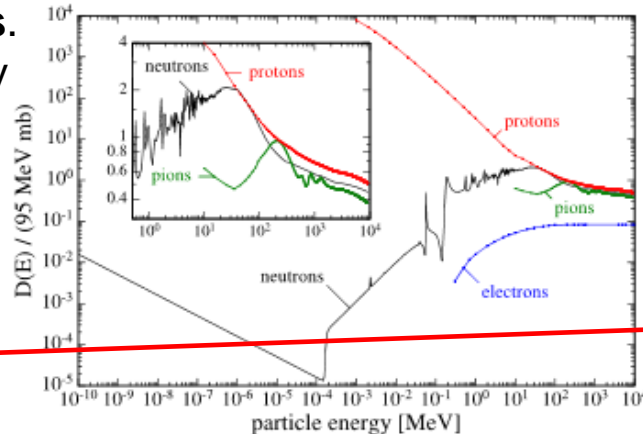
Example of radiation expected at High Luminosity LHC (HL-LHC) (Typically apply 1.5 safety factor)



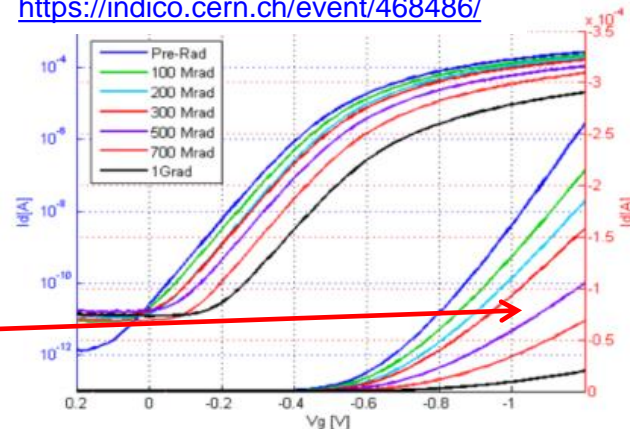
For Monolithic CMOS sensors initially target ~10<sup>15</sup>n<sub>eq</sub>/cm<sup>2</sup>

- Bulk damage** (measured in units of 1MeV equivalent neutrons/cm<sup>2</sup> (assuming scaling with **non-ionising energy loss**) drives the deterioration of **sensors**.
- For **microelectronics** worry about **total ionising dose**.
- (65nm CMOS - **RD53**) can start to see significant deterioration above **500Mrad (5MGy)**
- ◇Many different effects◇

niel



Federico Faccio: PMOS turn-on V<sub>g</sub>  
<https://indico.cern.ch/event/468486/>

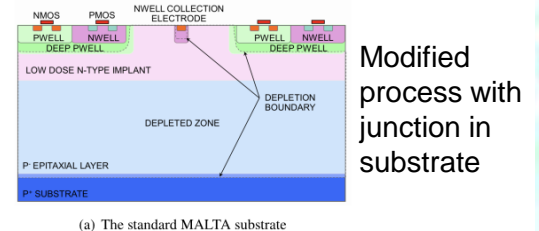
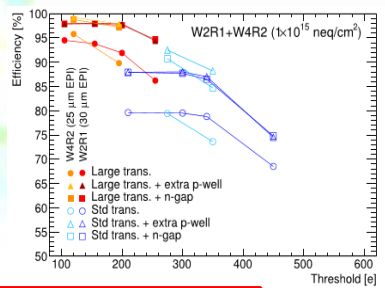
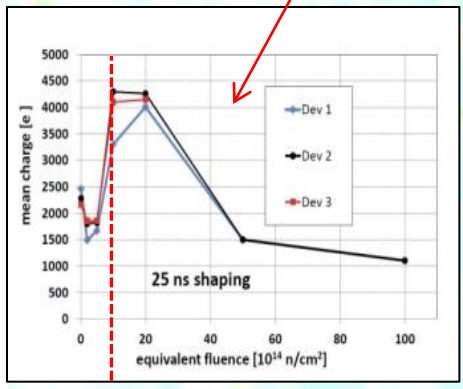
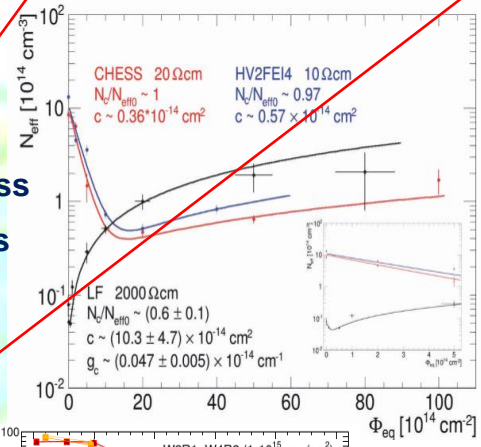
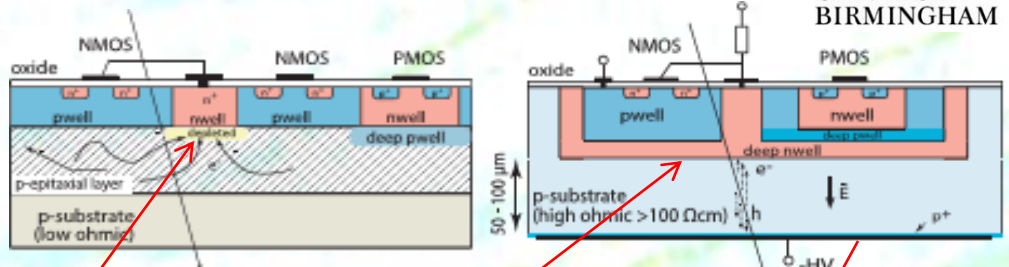


- Commercial CMOS Image Sensors offer possible dramatic decrease in costs (Monolithic Active Pixel Sensors)
- MAPS can deliver very low power consumption at low R/O speeds, possibly  $<100\text{mW}/\text{cm}^2$  i.e. simple water cooling

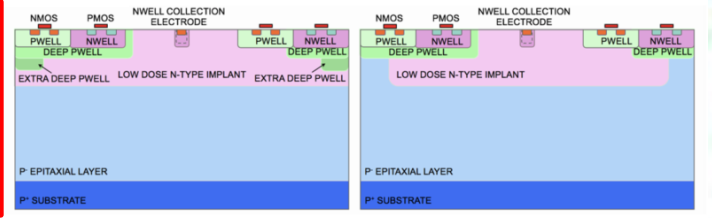
- Ultra low material budget (cf ALICE ITS upgrade:  $<0.5\%$  for inner layers,  $<1\%$  for outer layers)
- But these devices limited in speed and radiation hardness
- Current and near future MAPS for heavy ion experiments
  - integration time up to  $4\mu\text{s}$  (noise, electron diffusion)
  - radiation resistance up to few  $10^{13} n_{\text{eq}}/\text{cm}^2$

- Major developments in HV/HR-CMOS
  - deep depletion region with charge collection by drift not diffusion → huge improvements in collection speed and radiation hardness

- Can usually either have **small collecting node** (and therefore **faster and low noise**) but shallow charge collection or deplete from the **deep n-well** with larger signal produced in up to  $100\mu\text{m}$  of silicon but higher capacitance (→ more noise & slower)



See presentation  
<https://indico.cern.ch/event/803258/contributions/3582758/>  
 by Heinz Pernegger



Modified process with junction in substrate