SiW ECAL Studies for FCC-hh and Their Implications for FCC-ee

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• Introduction
  – Historical Perspective
  – Silicon - Tungsten\Lead Calorimetry
  – Performance Simulation
  – CMOS Monolithic Active Pixel Sensors
  – ALICE FOCAL Beam Tests
• Prototype CMOS Sensor Design
  – Reconfigurable MAPS Concept
  – Layout and Design
  – Device Performance
• Conclusions and Observations
Introduction

- The concept of SiW (or SiPb) calorimetry has long been under consideration as a possible option within the CALICE collaboration as offering unprecedented granularity for PFA and has been the focus of extensive prototyping and test beam activities

  ➢ See other presentations in this session

- For high radiation environments, CMS has developed the High Granularity Calorimeter (HGCAL) as the upgrade path for their forward calorimetry at HL-LHC
- The HGCAL will have ~600m² of silicon sensors (~500m² of scintillators) with 6M Si channels, 0.5 or 1.1 cm² cell size and overall ~27000 silicon modules
- The ECAL has 28 layers with Si + Cu/CuW/Pb absorbers giving 26 $X_0$ and ~1.7$\lambda$

<table>
<thead>
<tr>
<th>1.3, 1.4</th>
<th>Silicon sensors and modules</th>
</tr>
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<table>
<thead>
<tr>
<th>CMS</th>
<th>The Phase-2 Upgrade of the CMS Endcap Calorimeter Technical Design Report</th>
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<tbody>
<tr>
<td>26 514</td>
<td>67 153</td>
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- Silicon module costs ~4CHF/cm²

D. Barney, https://indico.cern.ch/event/718124/
A Reconfigurable CMOS Sensor for Tracking, Pre-Shower and Digital Electromagnetic Calorimetry

Historical Development of Silicon Sensor Arrays

- **1960s**: First Si strips
- **1970s**: Silicon sensor arrays
- **1980s**:
  - CDF
  - DELPHI
  - L3
  - OPAL
- **1990s**:
  - NA11
  - MARKII
  - AMS 1
- **2000s**:
  - ALICE
  - CMS
  - FERMILAB
  - CMS HGCAL
  - CALICE/FCC SW EM-calorimeter
  - CMS EGCal
- **2010s**:
  - Upgrade of CMS
  - Upgrade of ATLAS
  - Upgrade of ALICE
- **2020s**: CALICE/FCC Tpixel and MAPS EM-calorimeter

**Silicon Surface (m²)**

- **10⁻¹ m²**
- **10⁻² m²**
- **10⁻¹ m²**
- **10⁰ m² = 1 hectare**

**Number of Electronics Channels**

- **10⁴**
- **10⁵**
- **10⁶**
- **10⁷**
- **10⁸**
- **10⁹**
- **10¹⁰**
- **10¹¹**

**Year**

- **1980**
- **1990**
- **2000**
- **2010**
- **2020**
- **2030**
Many different silicon detector technologies for particle tracking have been developed over the last four decades.

What is remarkable is that every decade the instrumented areas have increased by a factor of 10 while the numbers of channels in the largest arrays have increased by a factor of 100. This despite other specifications for readout speed, spatial resolution, reduced multiple scattering (minimal total material including cooling and services) and radiation hardness also becoming much more demanding.
Commercial Microelectronics Evolution

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

Data Storage

Historically showed doubling times of < 2 years but now slowing.

However, particle physics lags significantly behind commercial state-of-the-art because of additional constraints

F Faccio: https://indico.cern.ch/event/468486
Particle Flow Calorimetry (PFA)

- Concept of a high granularity calorimeter with PFA capabilities widely studied as an option for calorimetry both for $e^+e^-$ (see other presentations in this session) and hadron colliders (see for example EP Seminar https://indico.cern.ch/event/718124/)

- In the HL-LHC/FCC-hh context, improving calorimetry targets multi-jet final states, missing energy and separation of heavy bosons in hadronic decays

"Typical" jet:
- ~62% charged particles (mainly hadrons)
- ~27% photons
- ~10% neutral hadrons
- ~1% neutrinos

- Idea of PFA is to measure each individual particle in a jet using the detector system that provides best energy/momentum determination for that particle type.
SiW ECAL CMOS MAPS Motivation

- CMS HGCAL silicon costs ~4CHF/cm² would still need to come down even more for many thousand m² (» 10⁷cm²) array to become affordable

  - NB partially mitigated by cost savings from reducing ECAL thickness for FCC-hh to < 20cm and removing need for cryostat with respect to LAr. (Reduces total cost of HCAL, magnet system and muon spectrometer)

- Excellent PFA capabilities but difficult to match LAr for radiation-hardness and EM energy resolution

- For a hybrid silicon system (such as the HGCAL), at some stage the price of polished high- \( \rho \) wafers could set a lower limit to what overall costs might be possible with separate thick depleted silicon substrate (but other options may exist)

- Alternatively, CMOS Imaging Sensors represent a ~20B$ business internationally (https://www.marketsandmarkets.com/Market-Reports/cmos-image-sensor-market-252212367.html) and market expected to continue growing rapidly driving down prices for such detectors

- Although current CMOS sensor array (such as for ALICE ITS Monolithic Active Pixel Sensor) cost estimates can currently be ~ten times* those for CMS HGCAL, expect prices will be much lower for larger orders and as a function of time, while integration of electronics within the sensor also reduces cost of full system

- Prototypes (see below) demonstrate concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to > 10¹⁵nₑq/cm²

  - * A. Andreazza this morning
The Digital EM Calorimeter Concept

- Count pixels above threshold within each 5mm×5mm pad
- 5.1 Silicon Tungsten Calorimeter

Idea initially in context of CALICE but then adapted to FCC-hh environment.

Simulated 4 different geometries:
- 30 Layers, 3.5mm W (30 × 1.0 X₀)  5.6mm Pb
- 50 Layers, 2.1mm W (50 × 0.6 X₀)  3.4mm Pb

Absorber (W or Pb), varying thickness
- Substrate (Si), 450μm
- Epitaxial (Si), 18μm

• For single electrons, similar performance of Digital ECAL (with realistic channel threshold per pixel of $480e^*$) and Analogue ECAL (with perfect performance and full substrate signal per pad) up to around 300GeV (4T field without pile-up)

• Above this energy, saturation (more than one hit per $50\mu m \times 50\mu m$ pixel) starts to impact performance of digital compared with analogue ECAL

$*6 \times \sigma$ assuming noise of $\sigma = 80e$
ALICE Fo-Cal MAPS R&D

T. Peitzmann: International Workshop on Forward Physics and Forward Calorimeter Upgrade in ALICE (Tsukuba, 08.03.2019)

24 layer MIMOSA CMOS sensor calorimeter Si-W stack

1.5mm W

244 GeV electron: very high single particle hit rate in shower core

Good energy resolution but lower than simulations, particularly at higher energies

New ALPIDE CMOS sensor based 3cm×3cm area 24 layer stack

Looking forward to results from test-beams with this system

\[
\frac{\sigma_E}{E} = a \pm \frac{b}{\sqrt{E/\text{GeV}}} \pm \frac{c}{E/\text{GeV}}
\]

\[
a = (2.95 \pm 1.65)\%
\]

\[
b = (28.5 \pm 3.8)\%
\]

\[
c = 6.3\%
\]
**DECAL (4mm×4mm Array) Prototype Chip**

Concept in FCC-hh context of a common silicon development for:
- Outer tracking
- Pre-shower
- EM calorimeter

Reconfigurable sensor as:
- 5mm×50µm strips
- 5mm×5mm pad

Prototype as proof of concept (180nm CMOS*)

### Strip mode

<table>
<thead>
<tr>
<th>64 strip array</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 x 64 pixels</td>
</tr>
</tbody>
</table>

Information on up to 3 hits per column gives data rate 5.12Gb/s

### Pad mode

<table>
<thead>
<tr>
<th>4 pad array</th>
</tr>
</thead>
<tbody>
<tr>
<td>each 16 columns wide</td>
</tr>
</tbody>
</table>

Information on up to 15 hits per column giving 240 hits per pad gives data rate of 2.56Gb/s

<table>
<thead>
<tr>
<th>Specification</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Pitch</td>
<td>µm</td>
<td>55</td>
</tr>
<tr>
<td>Resolution</td>
<td>pix</td>
<td>64 x 64</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>MHz</td>
<td>40</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>e- rms</td>
<td>80</td>
</tr>
<tr>
<td>Max hits/col (pad mode)</td>
<td>hits</td>
<td>15</td>
</tr>
<tr>
<td>Max hits/col (strip mode)</td>
<td>hits</td>
<td>3</td>
</tr>
</tbody>
</table>

*TowerJazz (Small collecting node)
16 pixels are grouped together

For PAD mode:
- 4 bits of data + carry (pad mode)

For STRIP mode:
- only the 2 first bits of data used

To achieve data rate of 40MHz
column sum has to be complete
within 25ns using fast logic

(Approach should also have
potential for lower power)
DECAL – Analogue Performance

Analogue Test Diode

PreAmp Signals

Shaper Signals

Some delay in measured response time with respect to FE simulation (but expect ~10ns signal collection)

10x10µm² TriLite laser (pJ/pulse, λ=1064 nm)

Estimate of injected charge in 18 µm epitaxial layer of DECAL sensor uses measured signal in photodiode
DECAL Prototype: Laser Testing

Threshold at which output of comparator first fires vs strip #

Single strip threshold at which comparator first fires vs time

IEEE MIC-NSS (30/10/19) I. Kopsalis

Check pad and strip mode response to different area light spots

Global threshold value of 1 V
Conclusions

- Si-W calorimetry should allow excellent PFA performance with a seamless transition from outer tracking → pre-shower → ECAL in potentially the same technology.

- For future Si-W (Si-Pb) calorimeters to be affordable, need silicon sensor costs to come down to ~ CHF/cm² (as potential silicon areas are » 10⁷ cm²).

- It could be that this becomes more achievable in CMOS Imaging Sensor technologies given the very large, fast growing commercial market and the overall system cost impact of integrating the front-end electronics with the sensor substrate.

- Power needs study (FCC-ee CMOS estimates range ~50-100 mW/cm² (no pulsing). Walter Snoeys and Auguste Besson, this meeting on Tuesday) (cf CMS HGCAL: ~200 kW).

- A prototype developed which proves concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to > 10¹⁵ n eq/cm². (Next step is to reprocess DECAL prototype taking advantage of these features).

- Digital EM calorimetry also provides an excellent potential solution for future e⁺e⁻ facilities with very fast charge collection which could also be useful for triggering.

- Aspects could also be employed with other calorimeter technologies, for example as high granularity pre-shower integrated with outer tracking layers.

- RD50 was publishing first results on irradiations in the p-type detector technologies currently being implemented for the HL-LHC ATLAS and CMS upgrade trackers in 2004.

→ Require ~20 year lead-time for starting R&D targeting largest future systems.
DECAL Prototype: Data Acquisition System

- DIGILENT NEXYS Video Board
- DECAL motherboard allows all the bias voltages and currents to be software controlled.
- Ethernet based readout using ATLAS ITSDAQ software and hardware.
- System allows readout at 40MHz

Simulate pixel output by placing data in test shift register and checking output is correct for both strip and pad mode.

Pattern of 11'b clocked through in strip mode

Patterns of 01111'b and 10000'b clocked in pad mode
Energy spectrum of Cu measured with RAL HEXITEC detector

Scan of single strip threshold at which comparator first fires

Expected signal: $8050\text{eV} / 3.6\text{eV} = 2236\text{e}$

Taking width of fitted peak as estimator of noise gives

Signal/Noise $\approx 22$

Noise $\approx 100\text{e}$
The highest channel count arrays are based on pixelated detectors. For **hybrid pixel sensors** connection to the electronics requires flip-chip technologies.

**Historical Development of Silicon Sensor Arrays**

<table>
<thead>
<tr>
<th>Item</th>
<th>R&amp;D (kCHF)</th>
<th>Construction (kCHF)</th>
<th>Total Cost (kCHF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>2000</td>
<td>3300</td>
<td>5300</td>
</tr>
<tr>
<td>Beampipe</td>
<td>600</td>
<td>900</td>
<td>1500</td>
</tr>
<tr>
<td>Pixel CMOS Sensors</td>
<td>700</td>
<td>700</td>
<td>1400</td>
</tr>
<tr>
<td>Sensor test</td>
<td>100</td>
<td>150</td>
<td>250</td>
</tr>
<tr>
<td>Thinning &amp; dicing</td>
<td>200</td>
<td>300</td>
<td>500</td>
</tr>
<tr>
<td>Hybrid printed circuit</td>
<td>100</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>Mechanics</td>
<td>150</td>
<td>350</td>
<td>500</td>
</tr>
<tr>
<td>Assembly &amp; test</td>
<td>50</td>
<td>200</td>
<td>250</td>
</tr>
<tr>
<td>Installation tooling</td>
<td>0</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Air cooling</td>
<td>100</td>
<td>150</td>
<td>250</td>
</tr>
<tr>
<td>Services</td>
<td>0</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Patch panels</td>
<td>0</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

**Monolithic Active Pixel Detectors**

**Hybrid Pixel Readout ASICs**

- **Minimum feature size**: 250nm, 130nm, 65nm
- **Example Read-out Hybrid Pixel Chips**: ATLAS FE-I3, CMS Medipix, NA62 TDCPix, ATLAS IBL FE-I4, LHCb VeloPix, Medipix3RX, TimePix3, CLICpix, RDS3A, TimePix4
- **Typical hit data storage density capabilities**: <1Gb/s/cm², ~5Gb/s/cm², 40Gb/s/cm²
- **Output Bandwidth**: 40-160 Mb/s, 0.3-1.2 Gb/s, 2-20 Gb/s
Hybrid silicon detectors (pixels/strips) **signal** output drops with irradiation to very high doses.

- **Bulk damage** (measured in units of 1MeV equivalent neutrons/cm² (assuming scaling with non-ionising energy loss) drives the deterioration of sensors.
- For **microelectronics** worry about total ionising dose.
- (65nm CMOS - RD53) can start to see significant deterioration above **500Mrad (5MGy)**
- Many different effects

For Monolithic CMOS sensors initially target ~$10^{15}$n$_{eq}$/cm$^2$

Example of radiation expected at High Luminosity LHC (HL-LHC) (Typically apply 1.5 safety factor)

Federico Faccio: PMOS turn-on $V_g$

https://indico.cern.ch/event/468486/
Commercial CMOS Image Sensors offer possible dramatic decrease in costs (Monolithic Active Pixel Sensors)

MAPS can deliver very low power consumption at low R/O speeds, possibly <100mW/cm² i.e. simple water cooling
- Ultra low material budget (cf ALICE ITS upgrade: <0.5% for inner layers, <1% for outer layers)
- But these devices limited in speed and radiation hardness
- Current and near future MAPS for heavy ion experiments
  - integration time up to 4μs (noise, electron diffusion)
  - radiation resistance up to few $10^{13}$ n$_{eq}$cm$^{-2}$

Major developments in HV/HR-CMOS → deep depletion region with charge collection by drift not diffusion → huge improvements in collection speed and radiation hardness

Can usually either have small collecting node (and therefore faster and low noise) but shallow charge collection or deplete from the deep n-well with larger signal produced in up to 100μm of silicon but higher capacitance (→more noise & slower)

Modified process with junction in substrate

See presentation https://indico.cern.ch/event/803258/contributions/3582758/ by Heinz Pernegger