

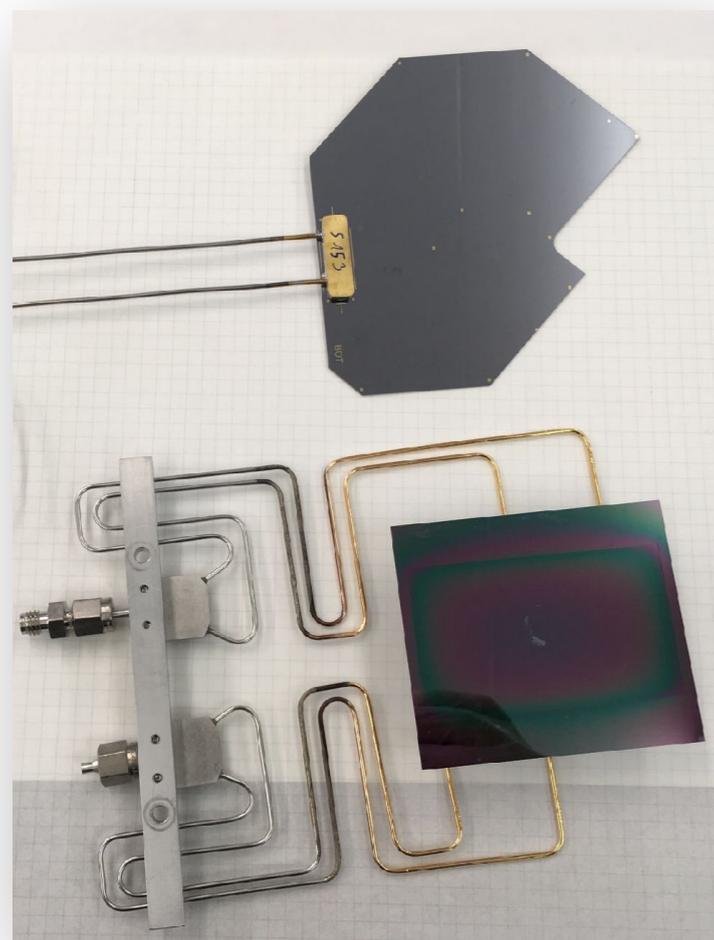
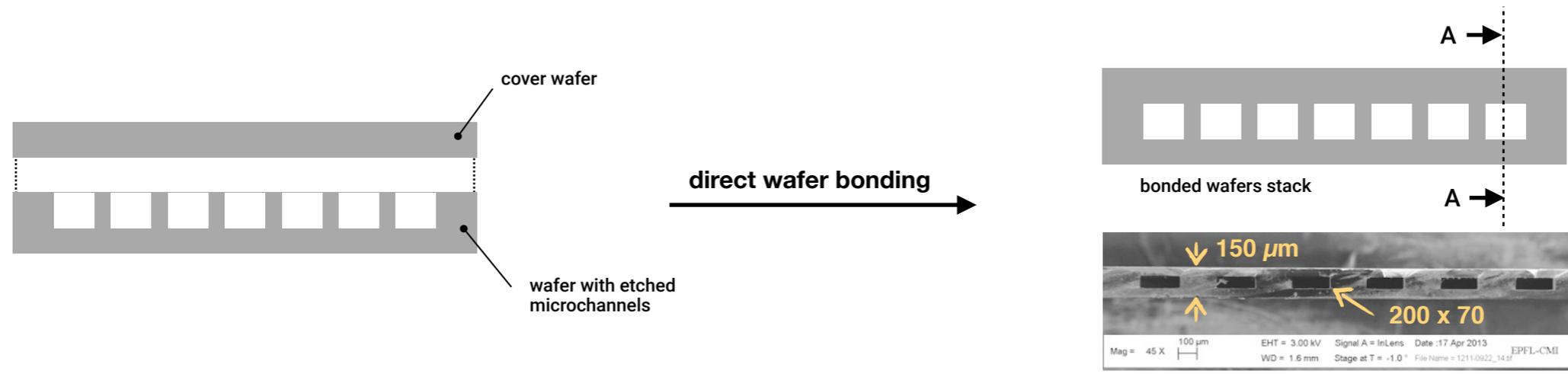
# Cooling solutions for the pixel detectors of NA62 and LHCb

Alessandro MAPELLI

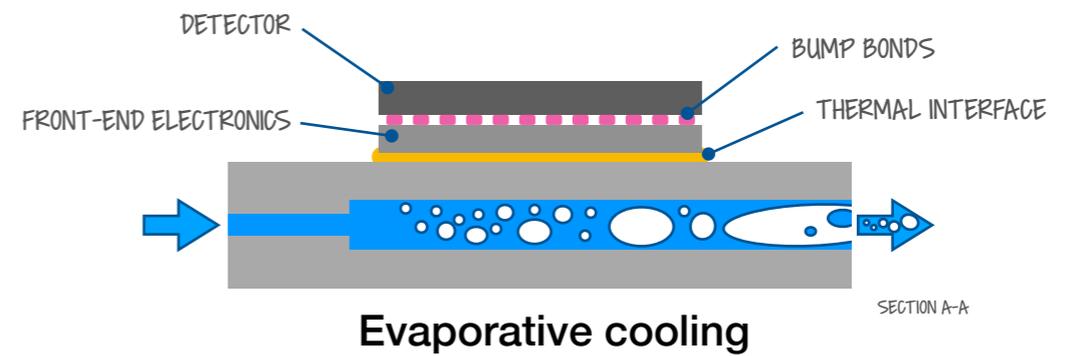
**3rd FCC Physics and Experiments Workshop  
13-17 January 2020**

[indico.cern.ch/event/838435](https://indico.cern.ch/event/838435)

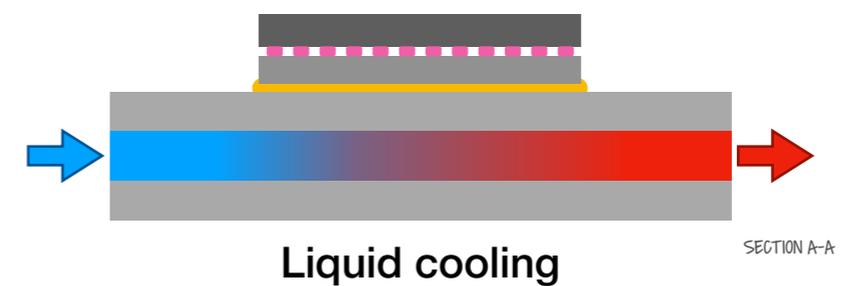
# silicon microchannel cooling plates



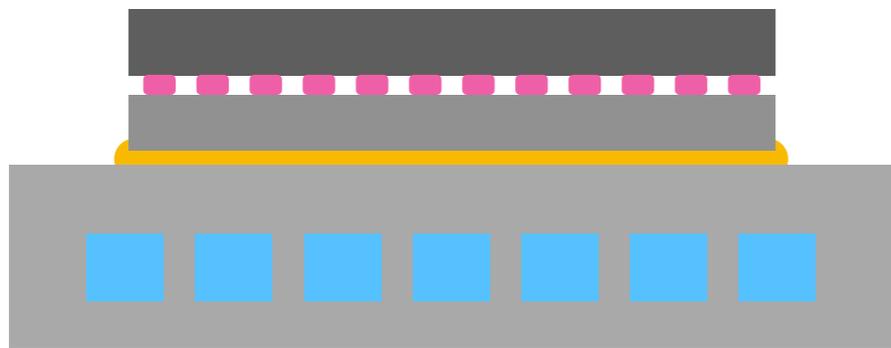
LHCb



NA62

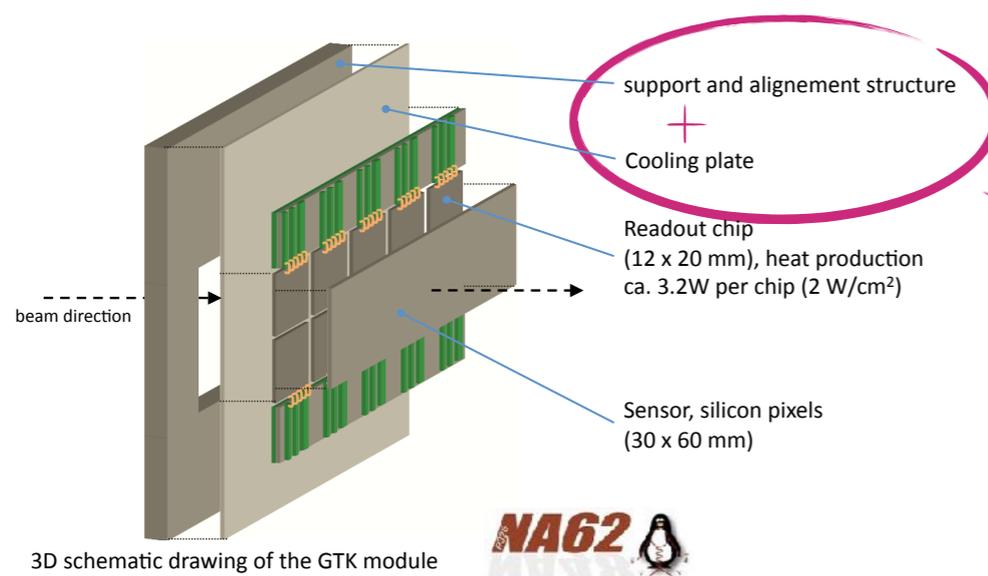


# Silicon microchannel cooling plates

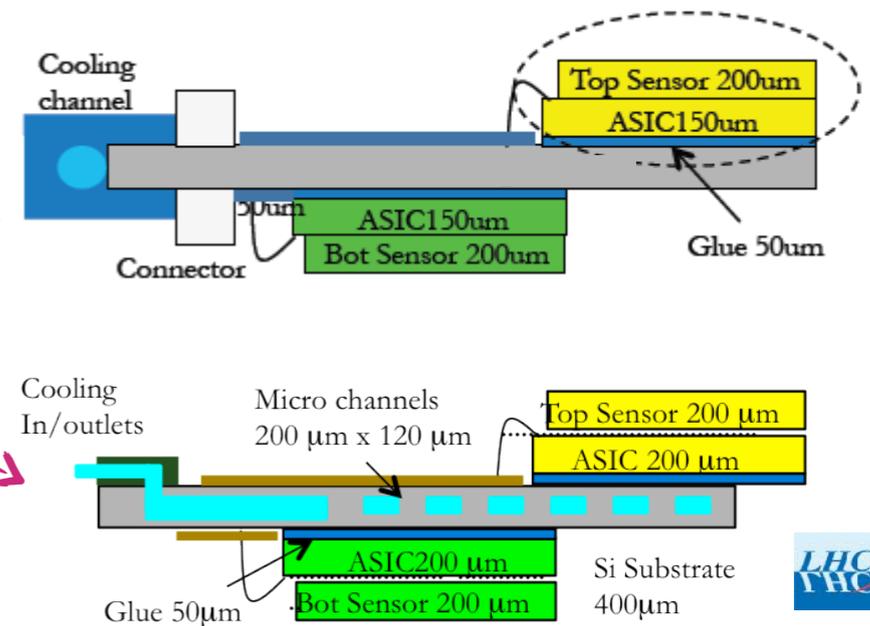


- No CTE mismatch
- Standard microfabrication processes
  - Microfluidics uses the same processes as microelectronics
- Active and distributed cooling
  - Better temperature uniformity across sensor
- Low and uniform material budget
- Radiation resistance
- Great potential for integration
  - Same microfabrication techniques as sensors and microelectronics.
- Thermal Figure of Merit

# NA62 GTK and LHCb VELO Upgrade

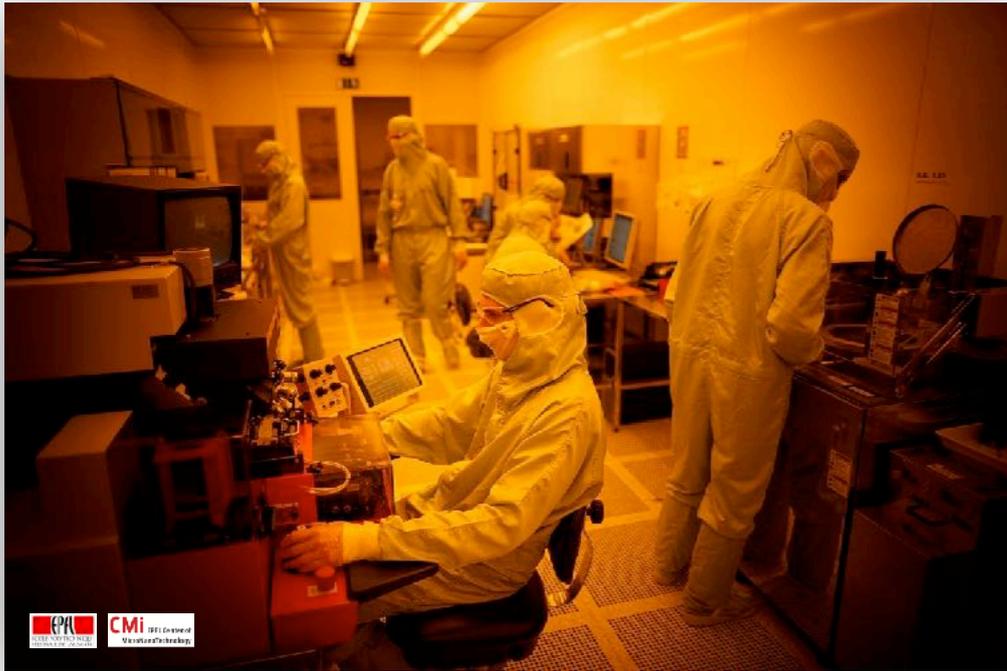


Silicon microchannel cooling plate

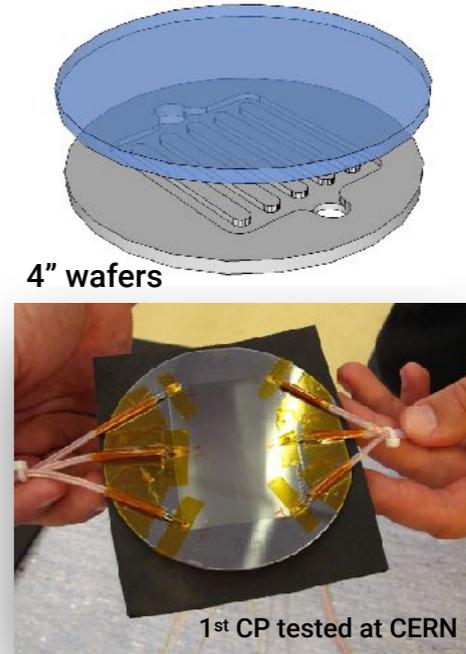
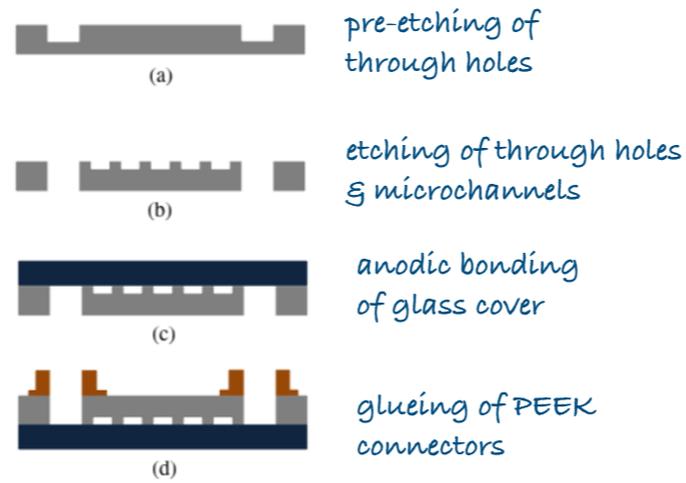


	NA62	LHCb
# of modules	3	52 (2x 26)
distance between modules	~10 m	2.5 cm
sensors	hybrid pixel	hybrid pixel
sensor size	60 x 38 mm	43 x 15 mm
sensors/module	1	4 (2 on each side of plate)
power dissipation (average)	~2 W/cm <sup>2</sup>	~2 W/cm <sup>2</sup>
coolant	liquid C <sub>6</sub> F <sub>14</sub>	evap. CO <sub>2</sub>
cooling plate thickness	~200 µm	~500 µm
operating temp. on sensor	-10°C	> -20°C
max. operating pressure	~10 bars	~60 bars
safety pressure	~20 bars	~200 bars
operation in vacuum	primary vacuum of NA62	secondary vacuum of LHC
distance to beam	in the beam axis	5.1 mm

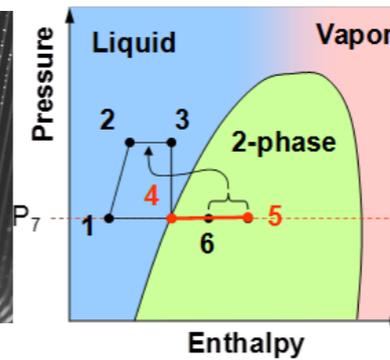
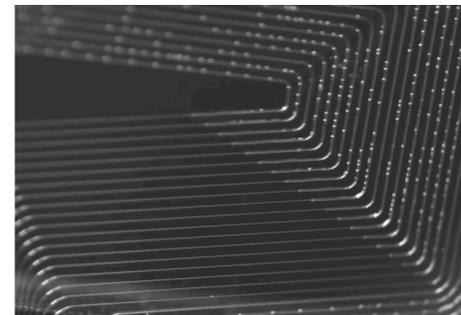
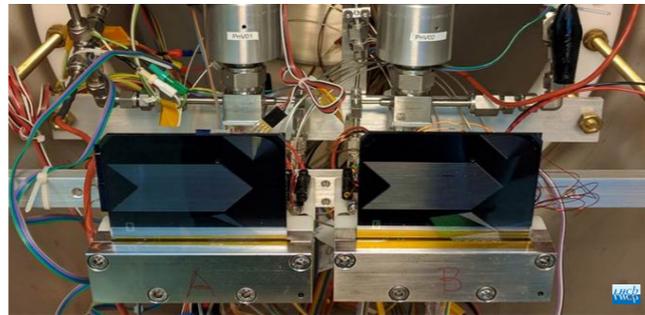
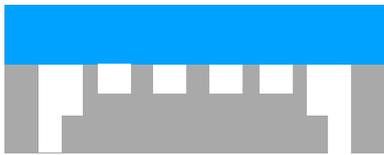
# “in-house” microfabrication processes



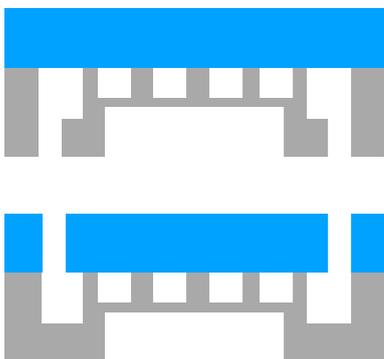
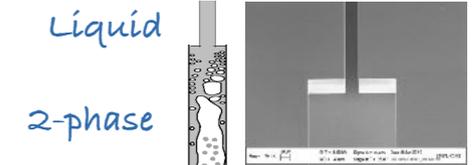
Process-flow developed at CERN for the first microchannel cooling plates



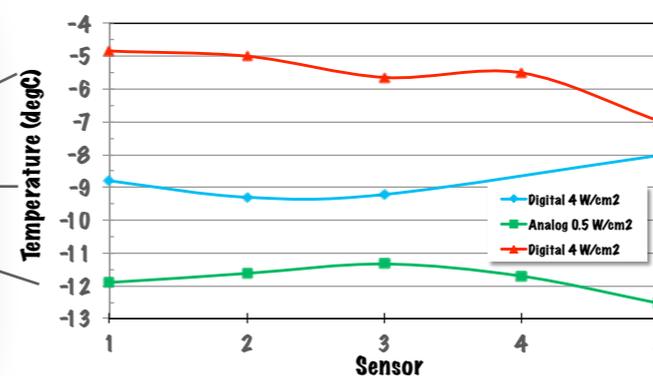
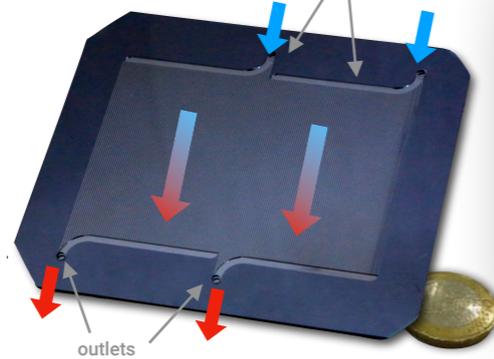
A. Mapelli et al. / Nuclear Physics B (Proc. Suppl.) 215 (2011) 349–352



First demonstration of 2-phase CO<sub>2</sub> circulation in silicon microchannels.

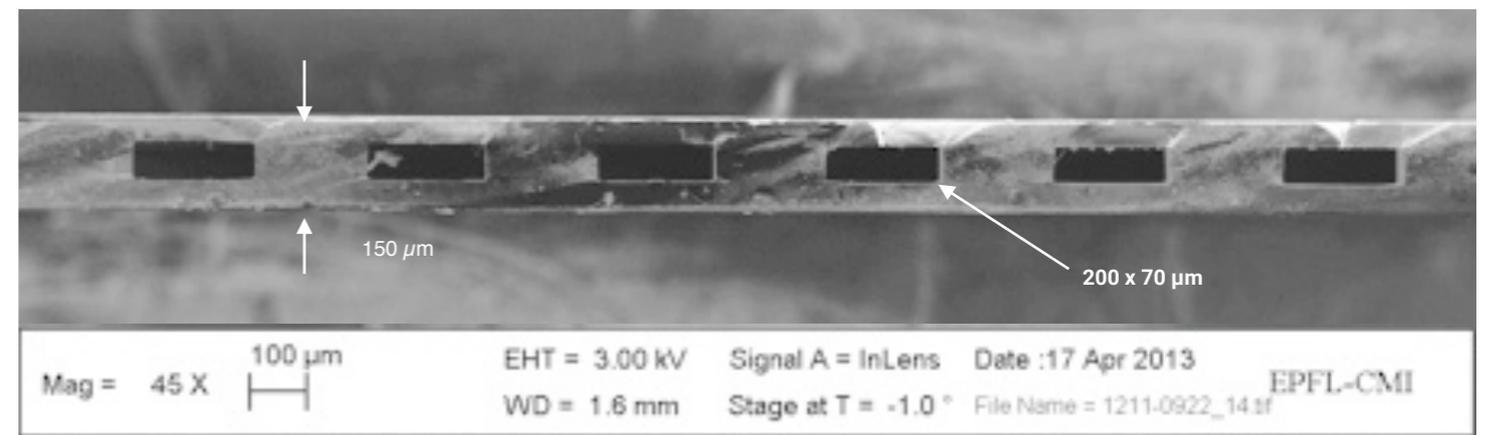
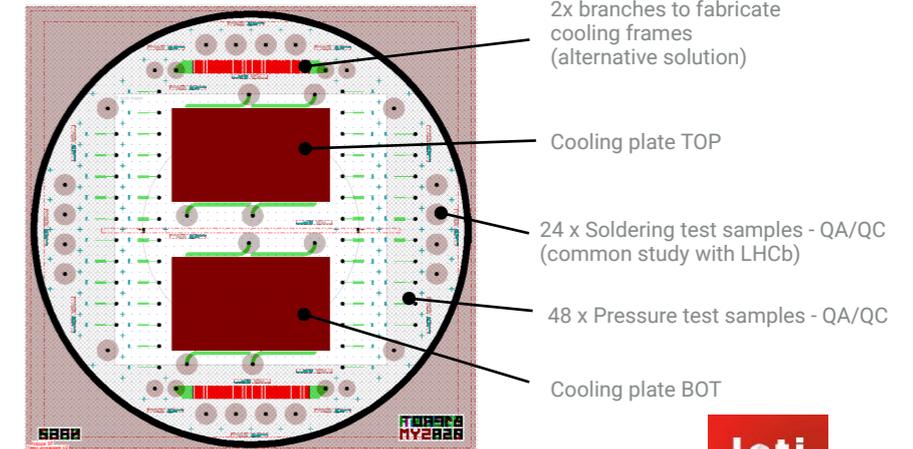
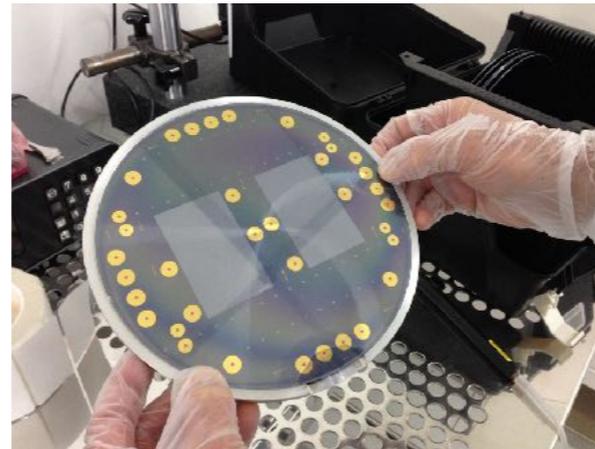


inlets and distribution manifolds (1.6 x 0.28 mm)



- Power dissipation
  - Digital Power 38 W
  - Analog Power 10 W
- Liquid C<sub>6</sub>F<sub>14</sub>
  - 7g/s
  - -19°C at inlet

# microfabrication of the GTK cooling plates

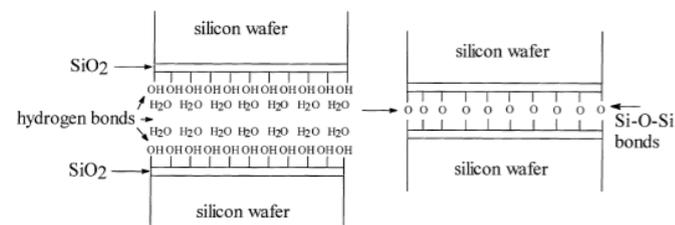


- Collaborative effort between CERN (ALICE, LHCb, NA62 and EP-DT) and external partners (CSEM, EPFL).
- Design by CERN EP-DT
- Prototypes fabricated by CERN EP-DT at EPFL-CMi on 4" wafers
- Pre-production series by IceMOS on 6" wafers
- Three batches fabricated at CEA-Leti on 8" wafers
- Fourth batch is under fabrication for the post-LS2 GTK modules.

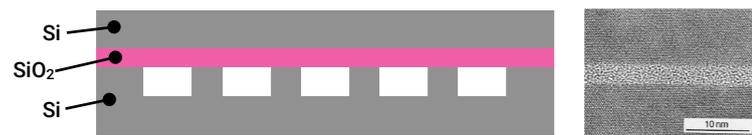
# Silicon direct wafer bonding

*No intermediate layer such as eutectic metals or adhesives between the wafers*

## Hydrophilic bonding



A. Plöbl, G. Kräuter/Materials Science and Engineering R25 (1999) 1-88

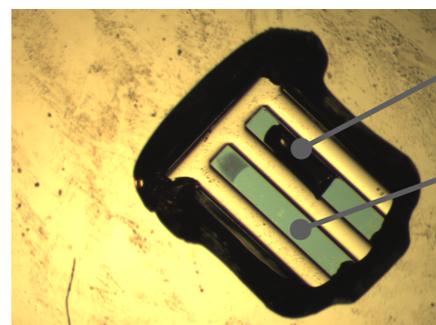


$T_{\text{anneal}} = 1050^{\circ}\text{C}$

$P_{\text{max}} \sim 400$  bars

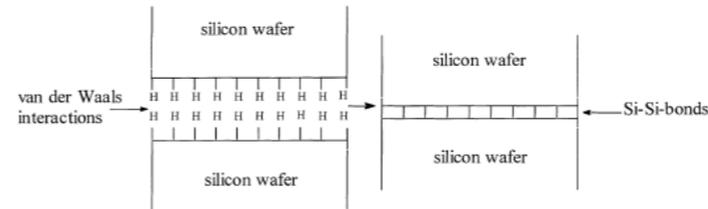
delamination + rupture

Delaminated SiO<sub>2</sub>      Fractured Si



Fractured Si  
Delaminated SiO<sub>2</sub>

## Hydrophobic bonding



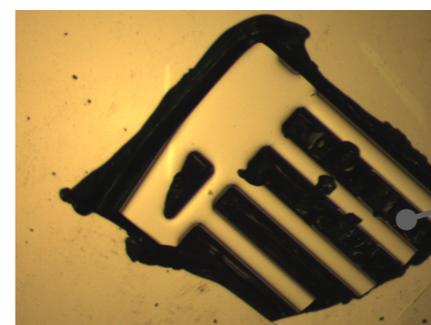
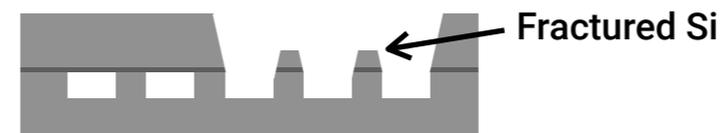
A. Plöbl, G. Kräuter/Materials Science and Engineering R25 (1999) 1-88



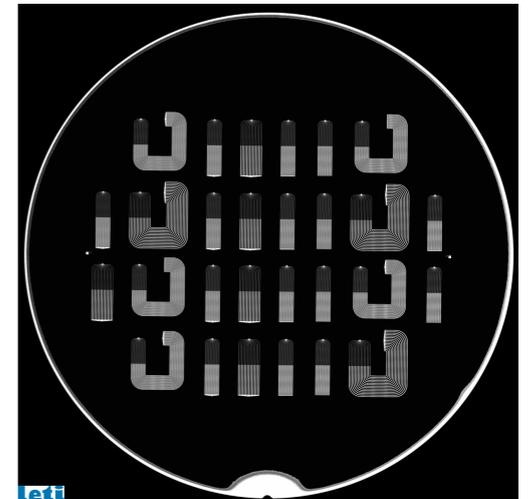
$T_{\text{anneal}} = 1050^{\circ}\text{C}$

$P_{\text{max}} \sim 700$  bars

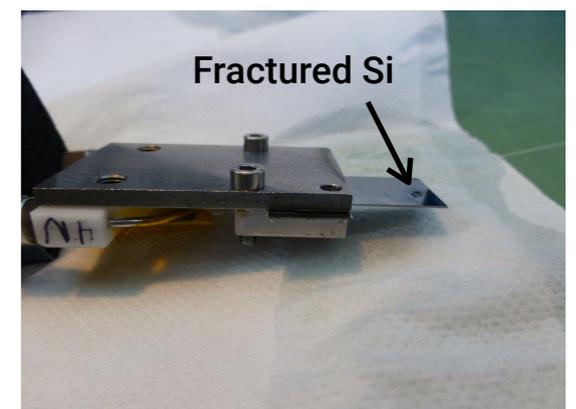
rupture without delamination



Fractured Si

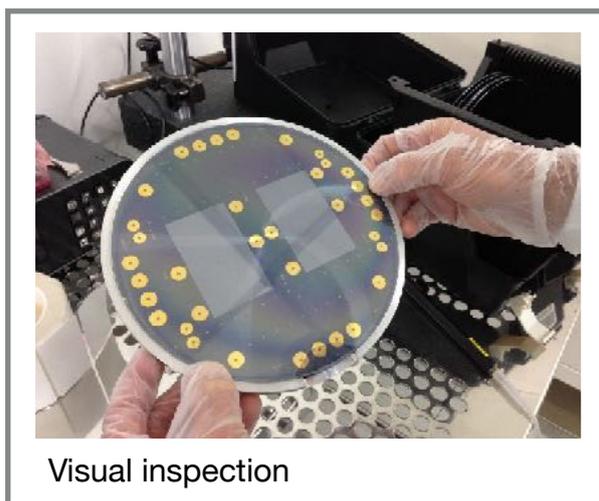
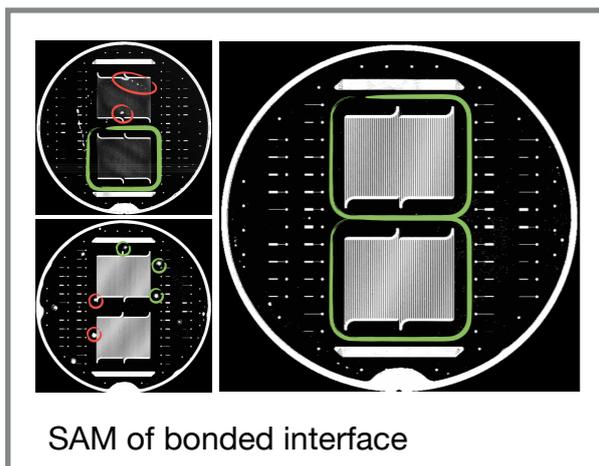
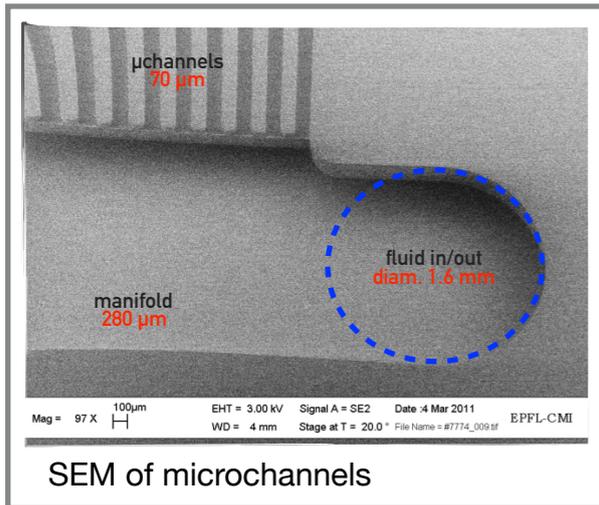


Scanning Acoustic Microscope image of bonded wafers with test structures.

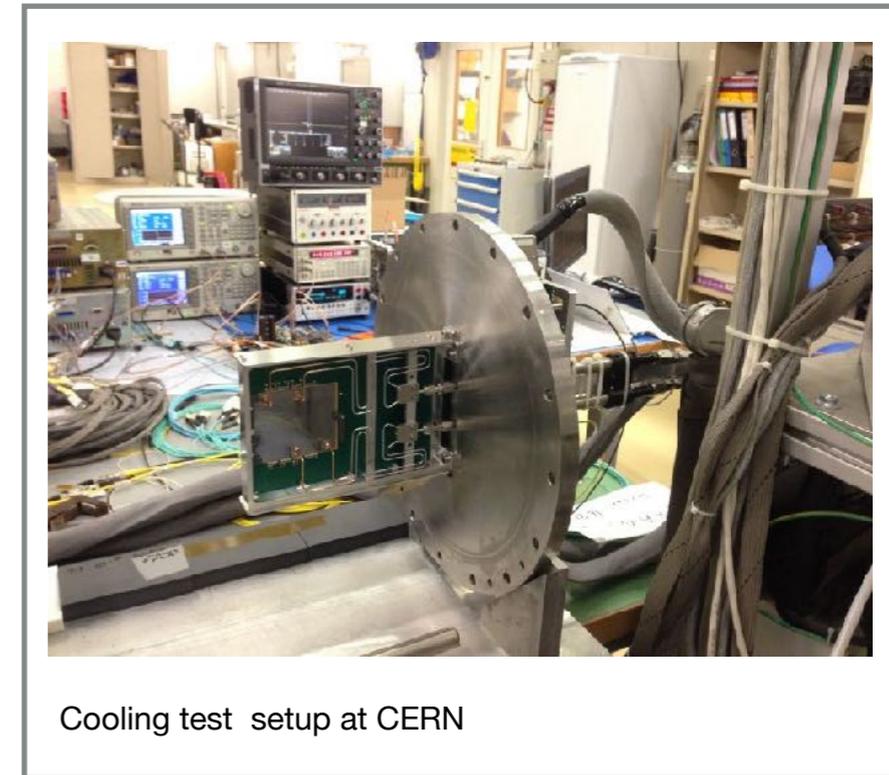
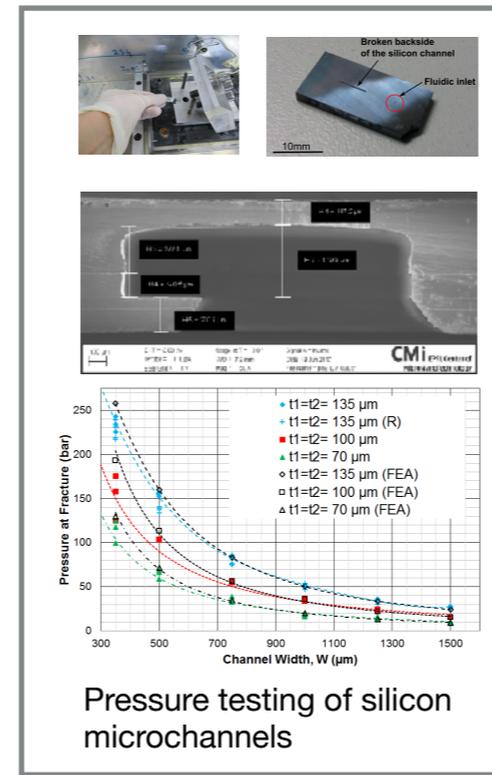
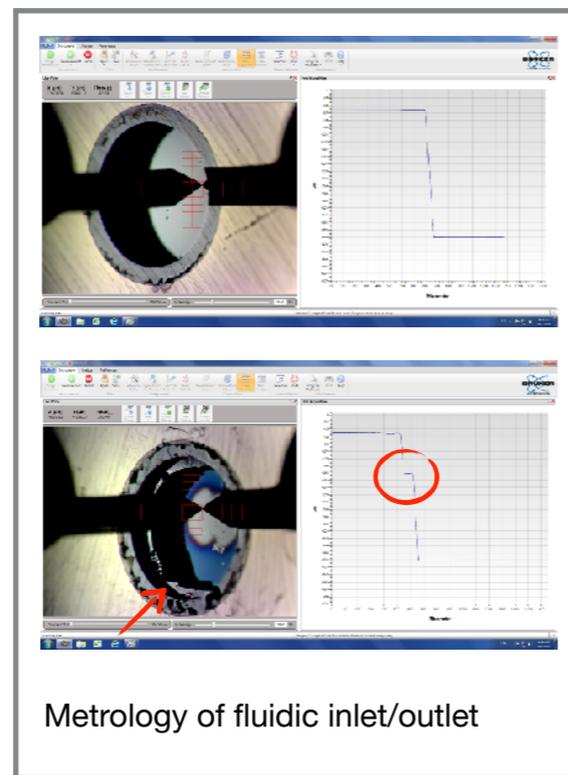


Fractured Si

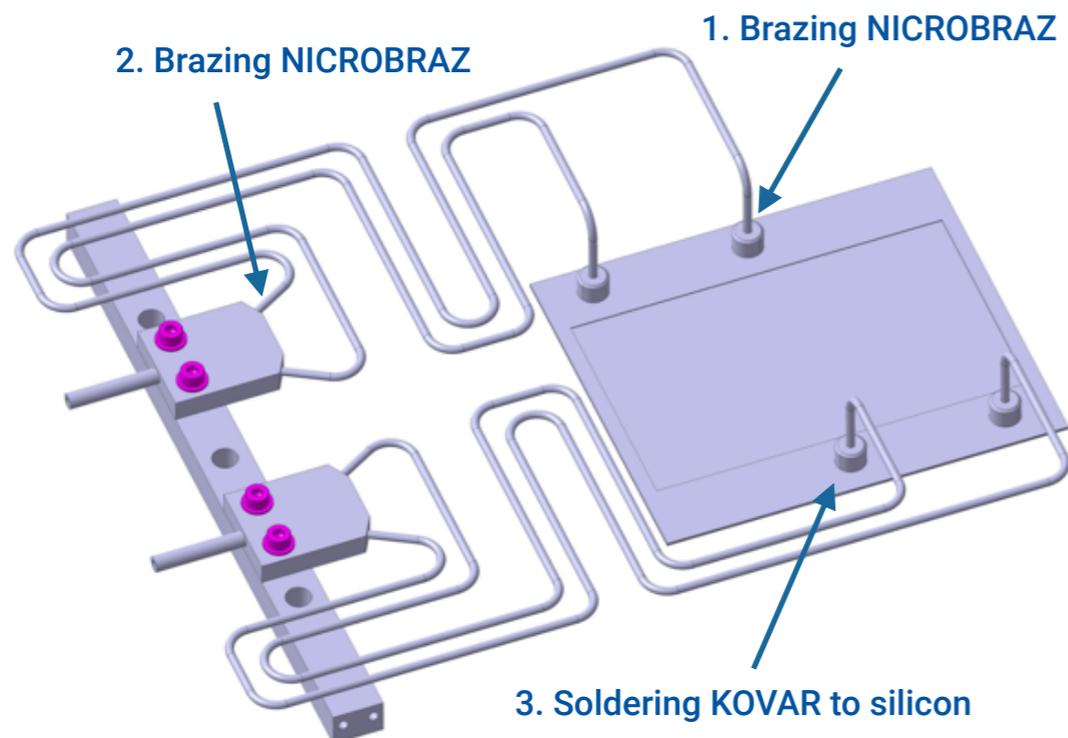
# QA/QC of the cooling plates



- Etching profiles of the microchannels.
- Scanning Acoustic Microscopy of bonded wafers.
- Visual inspection during tape-out.
- Metrology of cooling plates (Inlets and pools).
- Pressure tests on dedicated samples
  - 1500  $\mu\text{m}$  wide cavities (manifolds) > 25 bars
  - 200  $\mu\text{m}$  wide cavities (microchannels) > 200 bars
  - Soldering pads > 200 bars
- Pressure and temperature cycles on soldered cooling plate.



# Microfluidic system integration

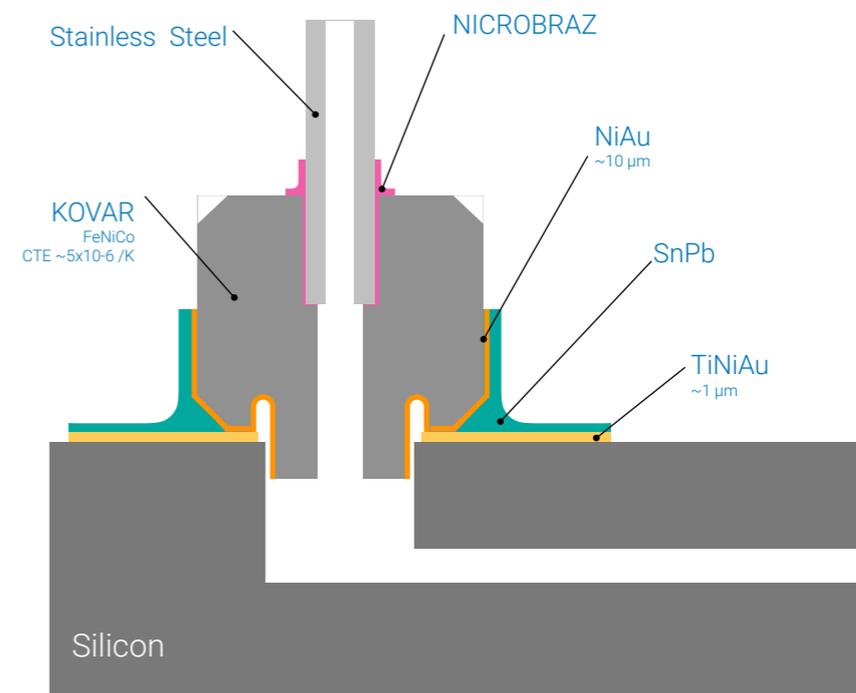
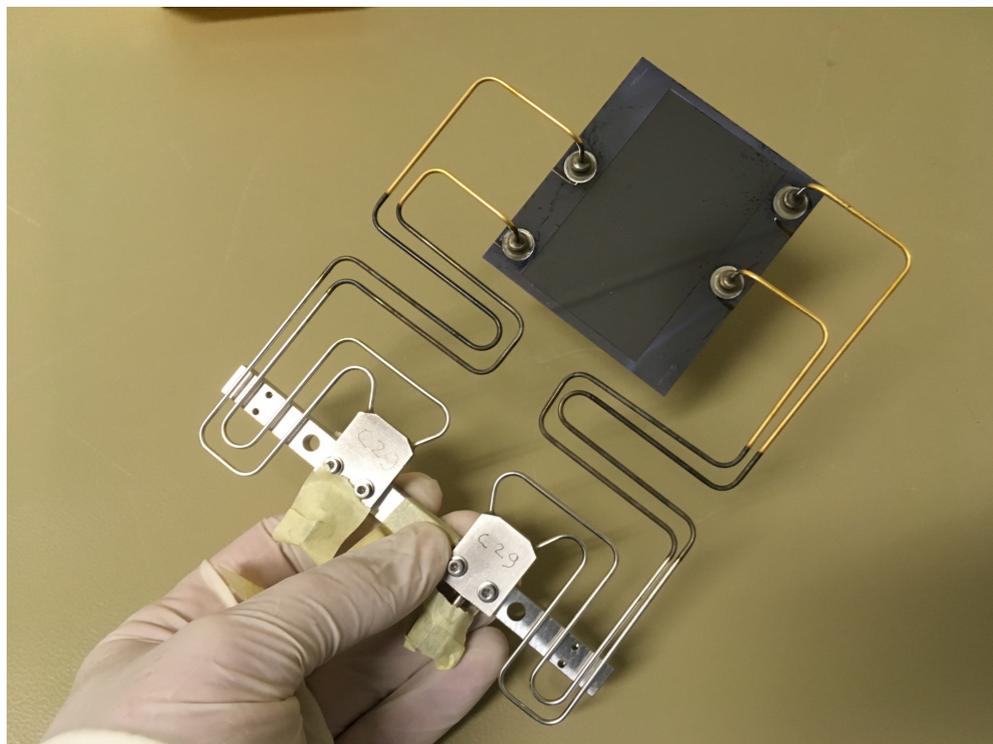


## Assembly steps:

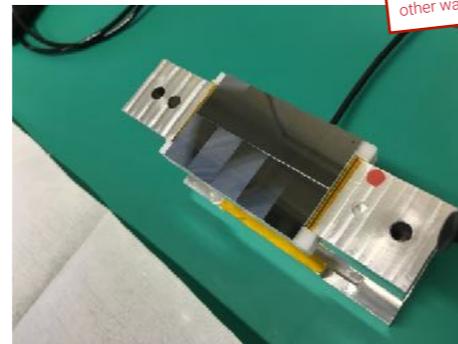
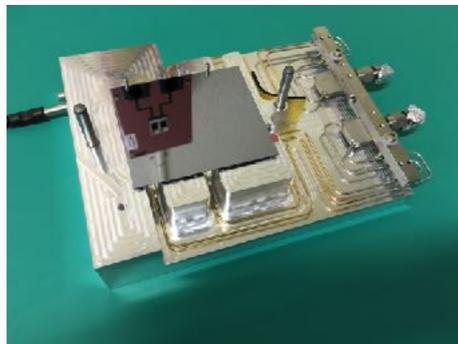
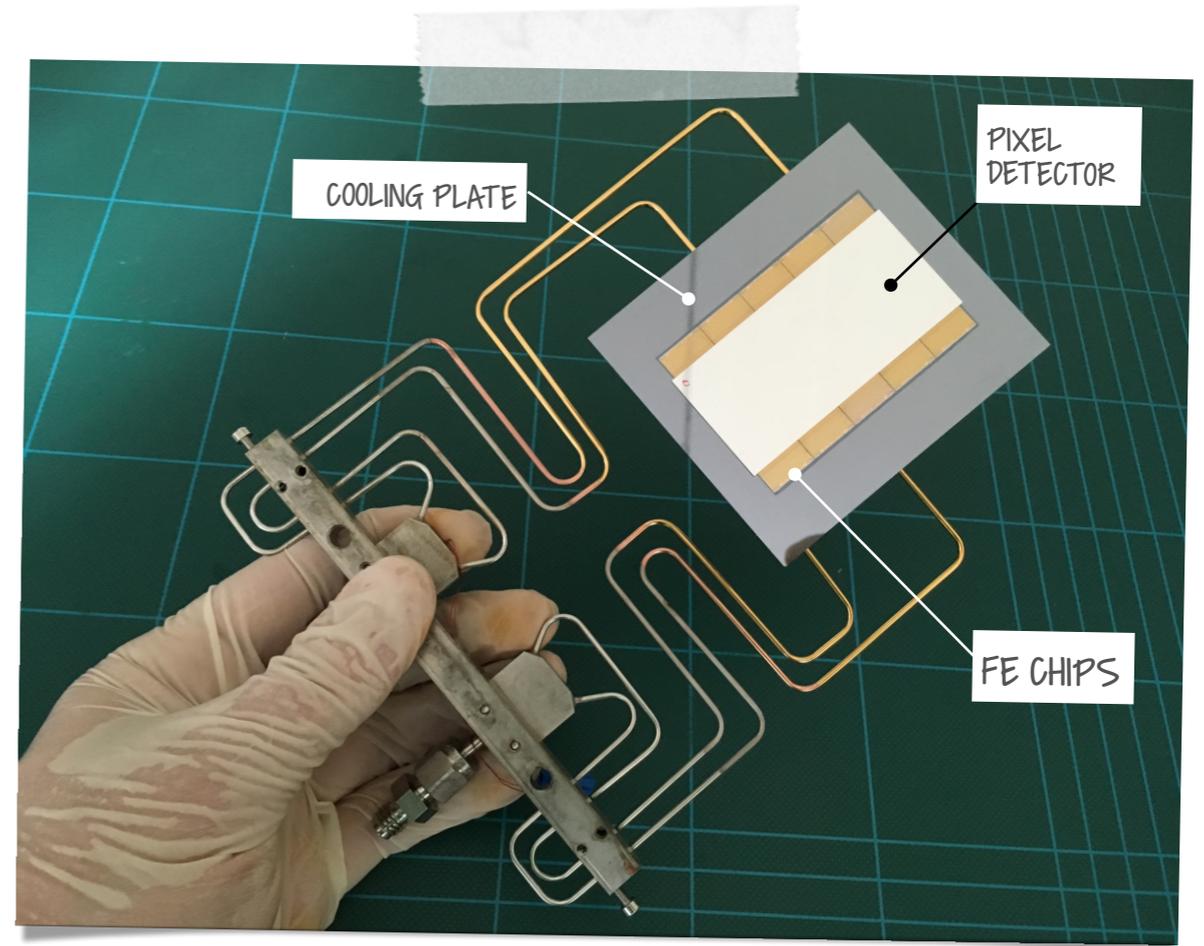
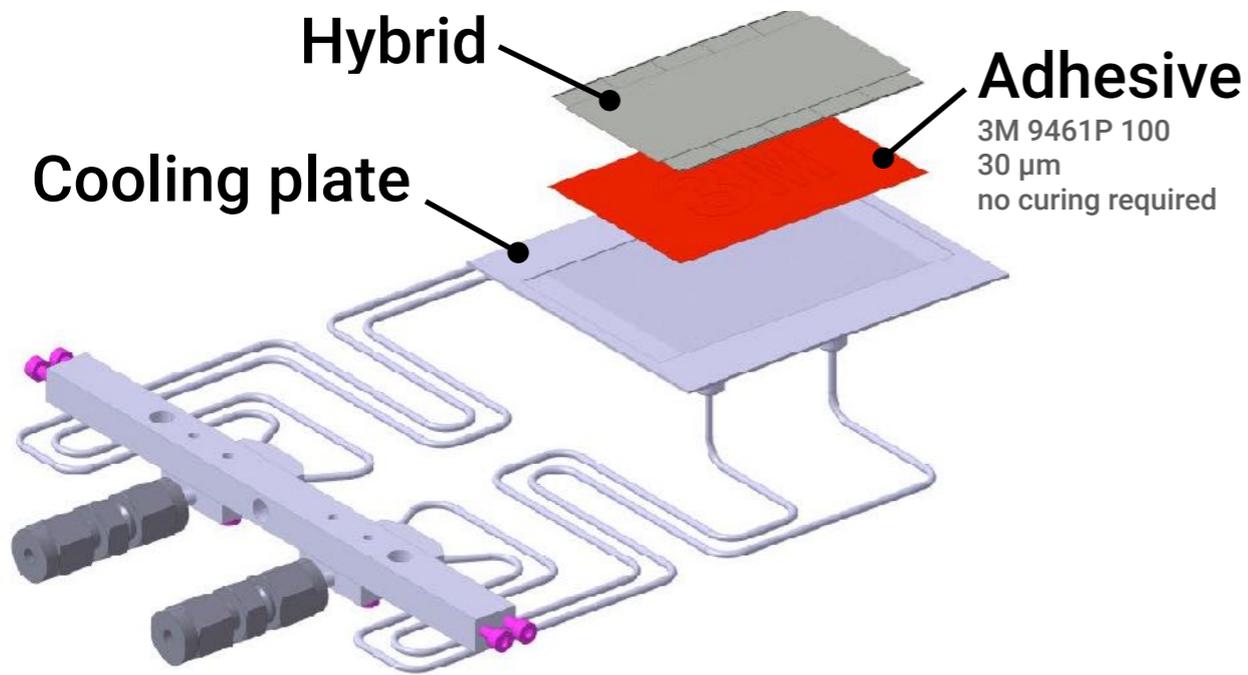
- Machining of KOVAR connectors;
- Brazing of connectors to capillaries (1);
- Bending of the capillaries;
- Brazing the other end of the capillaries to the manifolds (2);
- NiAu plating of the connectors;
- Soldering of the connectors to the silicon cooling plate (3);

## QA/QC:

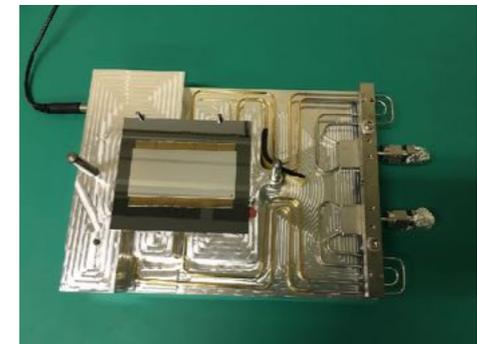
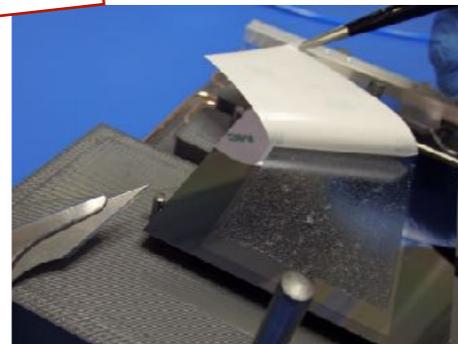
- After each joining step the He leak rate is measured. (Acceptance leak rate:  $10^{-10}$  mbar  $l^{-1}s^{-1}$ ).
- Pressure testing of the cooling plate at  $1.43 \times P_{op}$



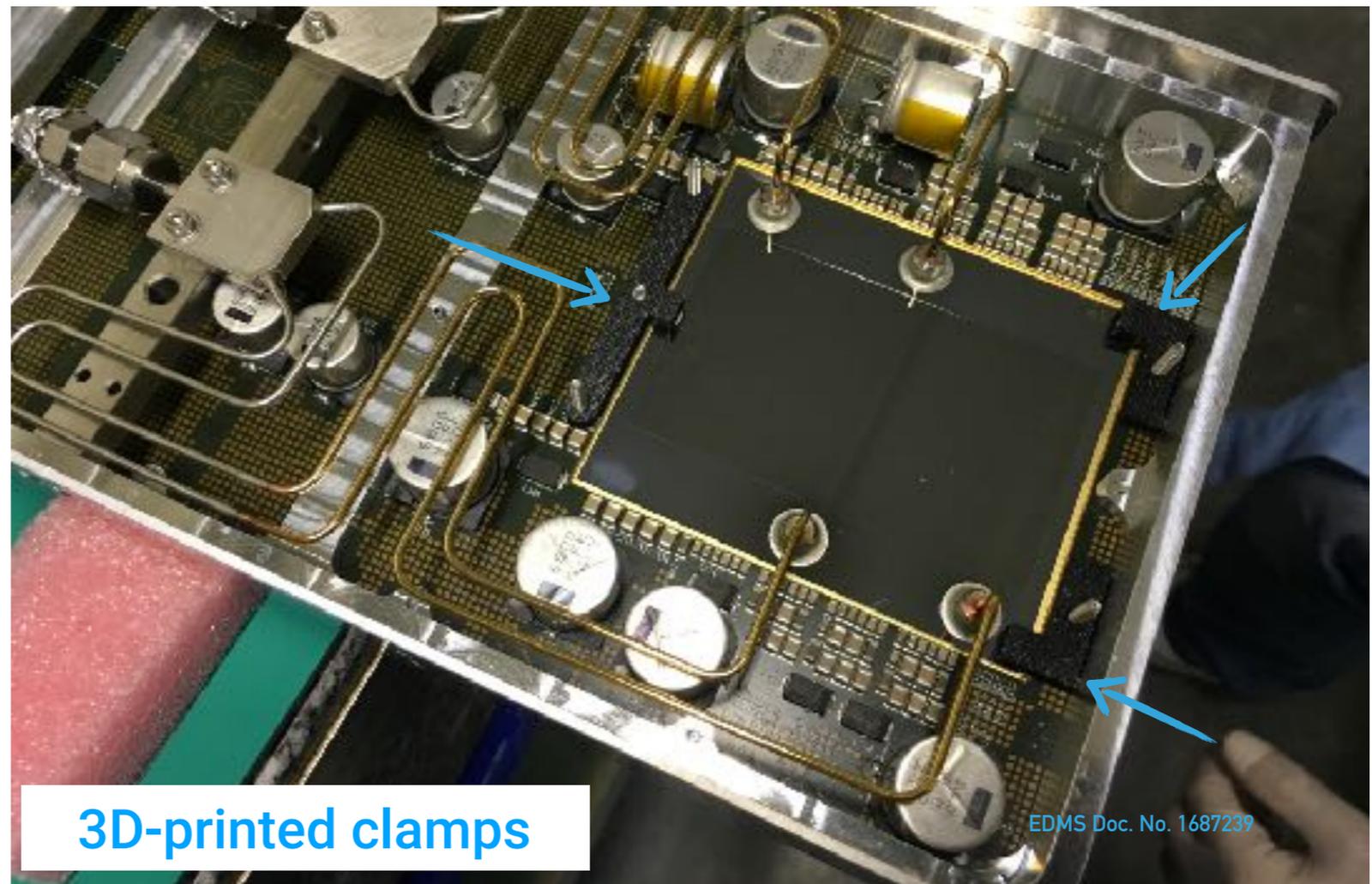
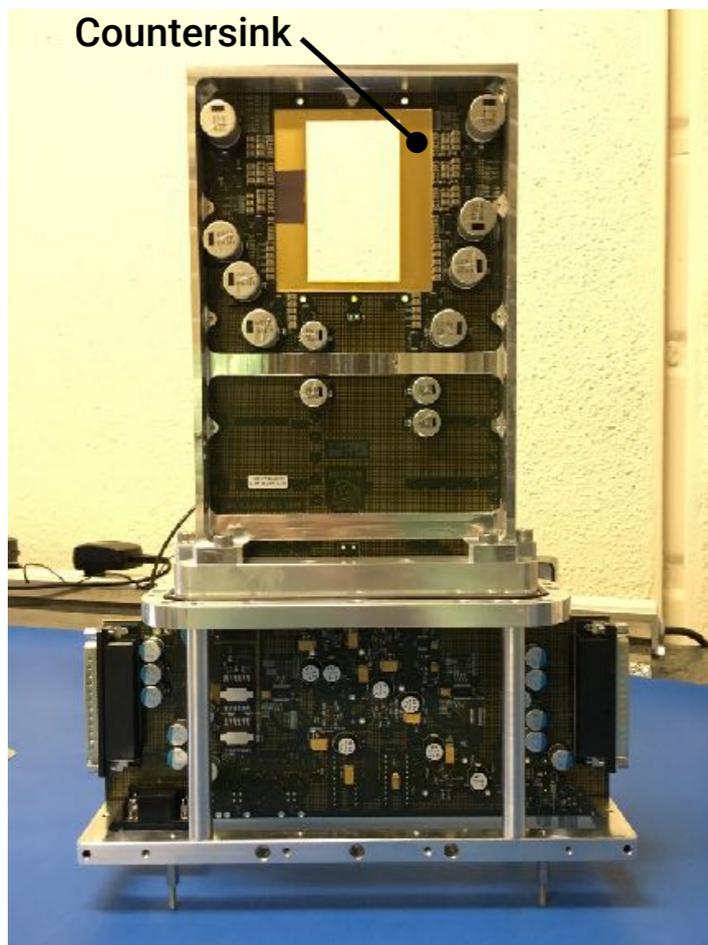
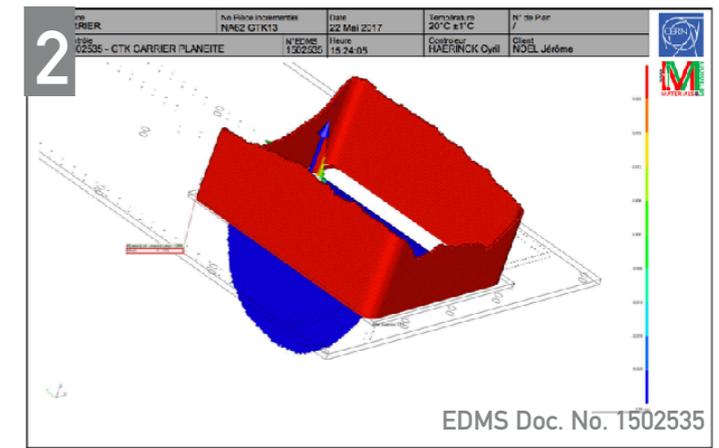
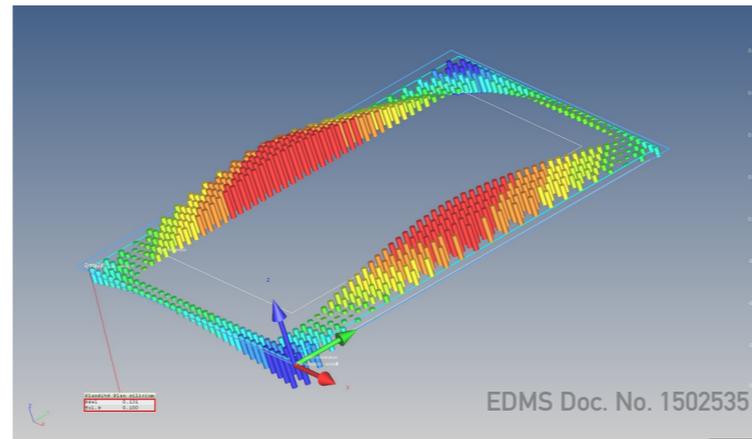
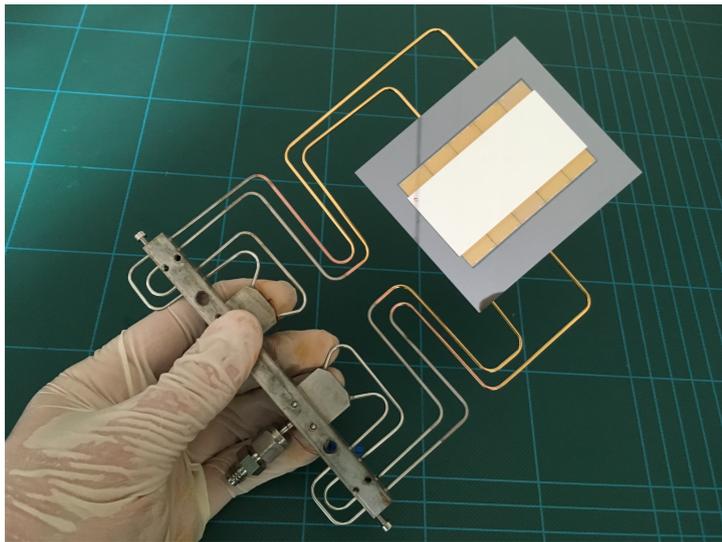
# Glueing the detector on the cooling plate



**REWORKABILITY**  
The detector can be detached from the cooling plate... or the other way around.

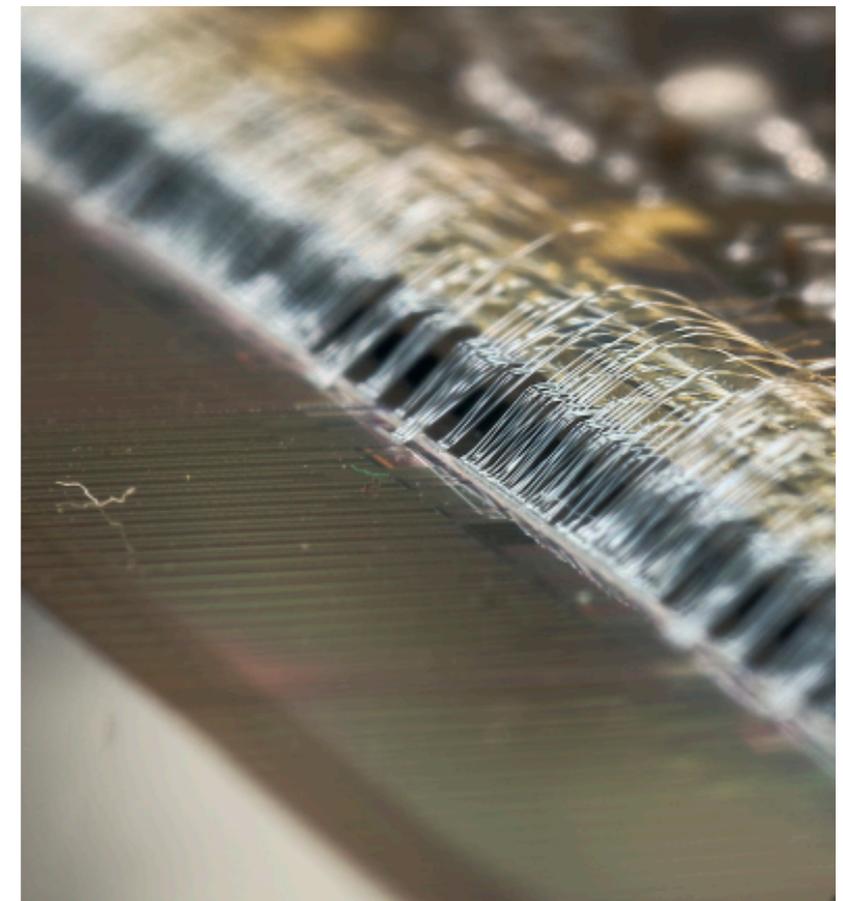
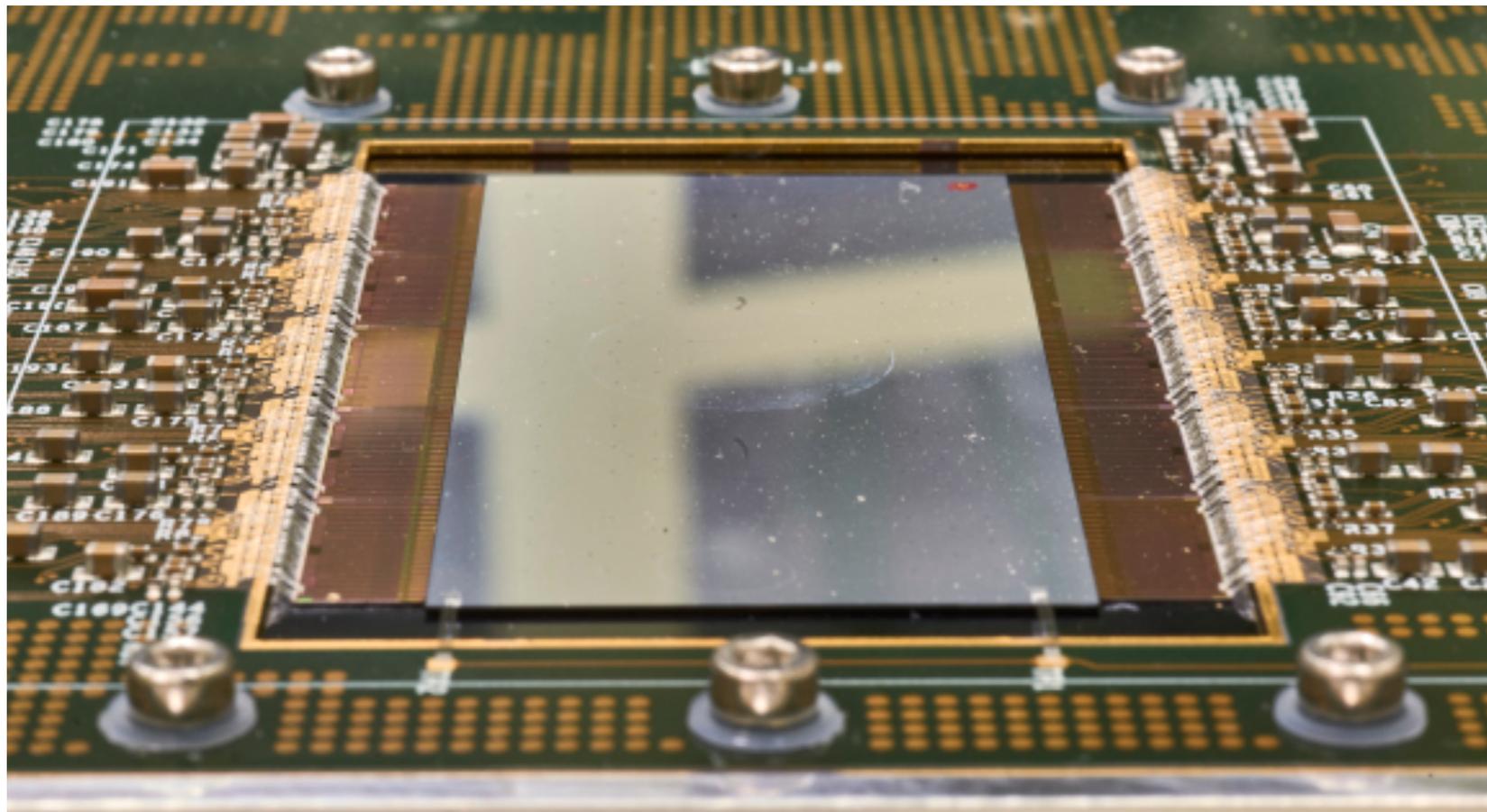
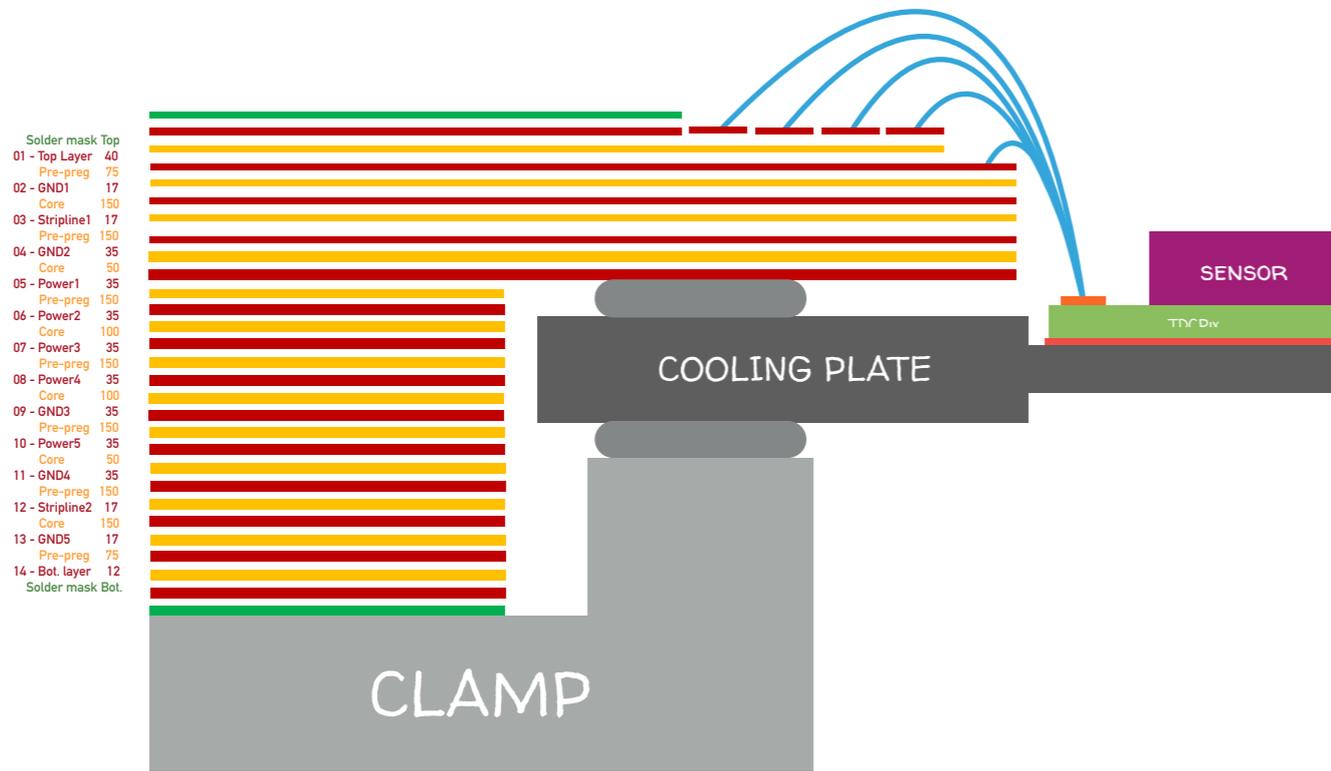


# Clamping the cooling plate to the PCB



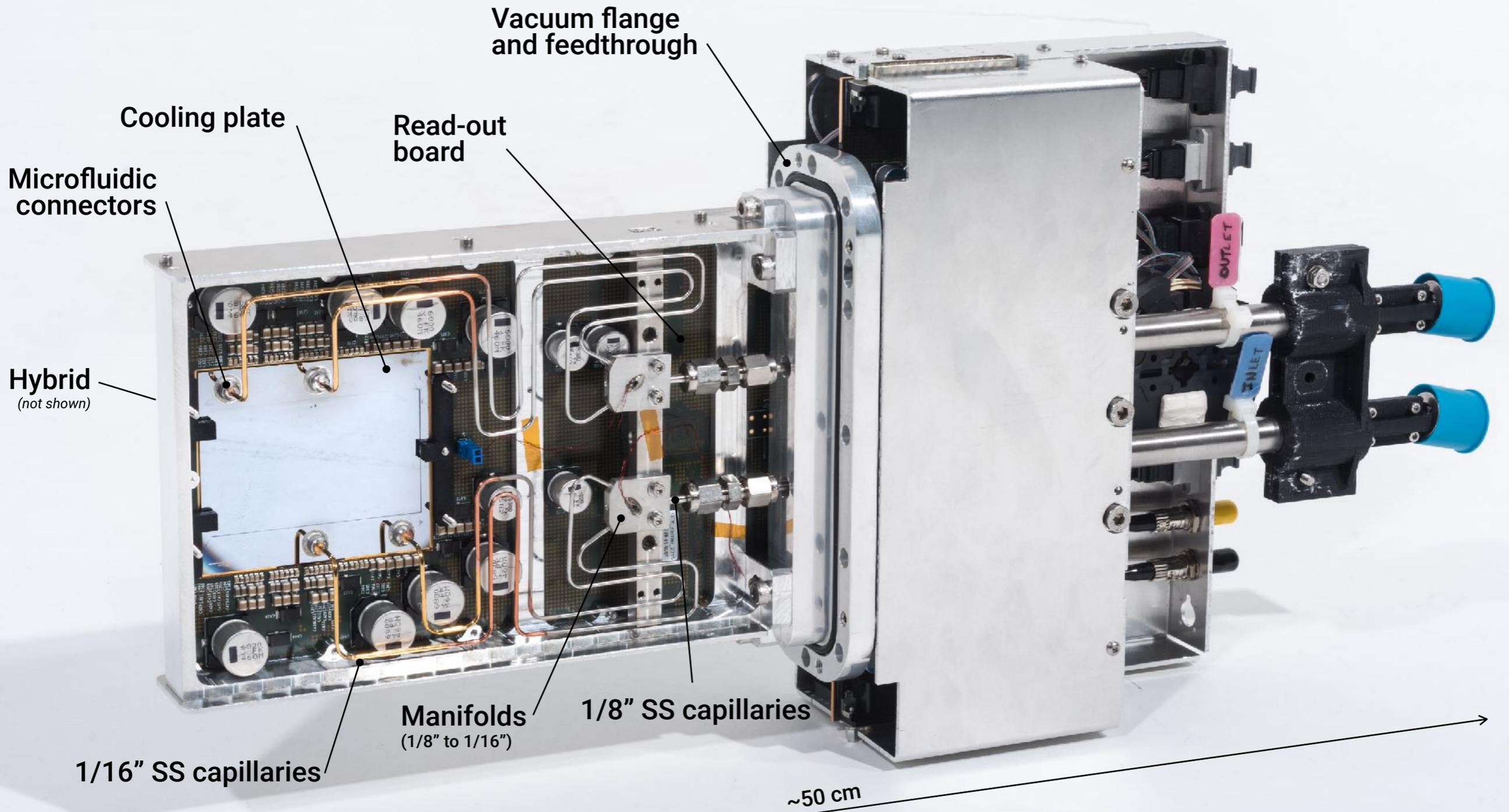
# Wire-bonding

- Performed at CERN (<http://bondlab-ga.web.cern.ch/>)
- 18000 wire bonds per module with a pitch of 73  $\mu\text{m}$
- Height difference between PCB pads and TDCPix pads.



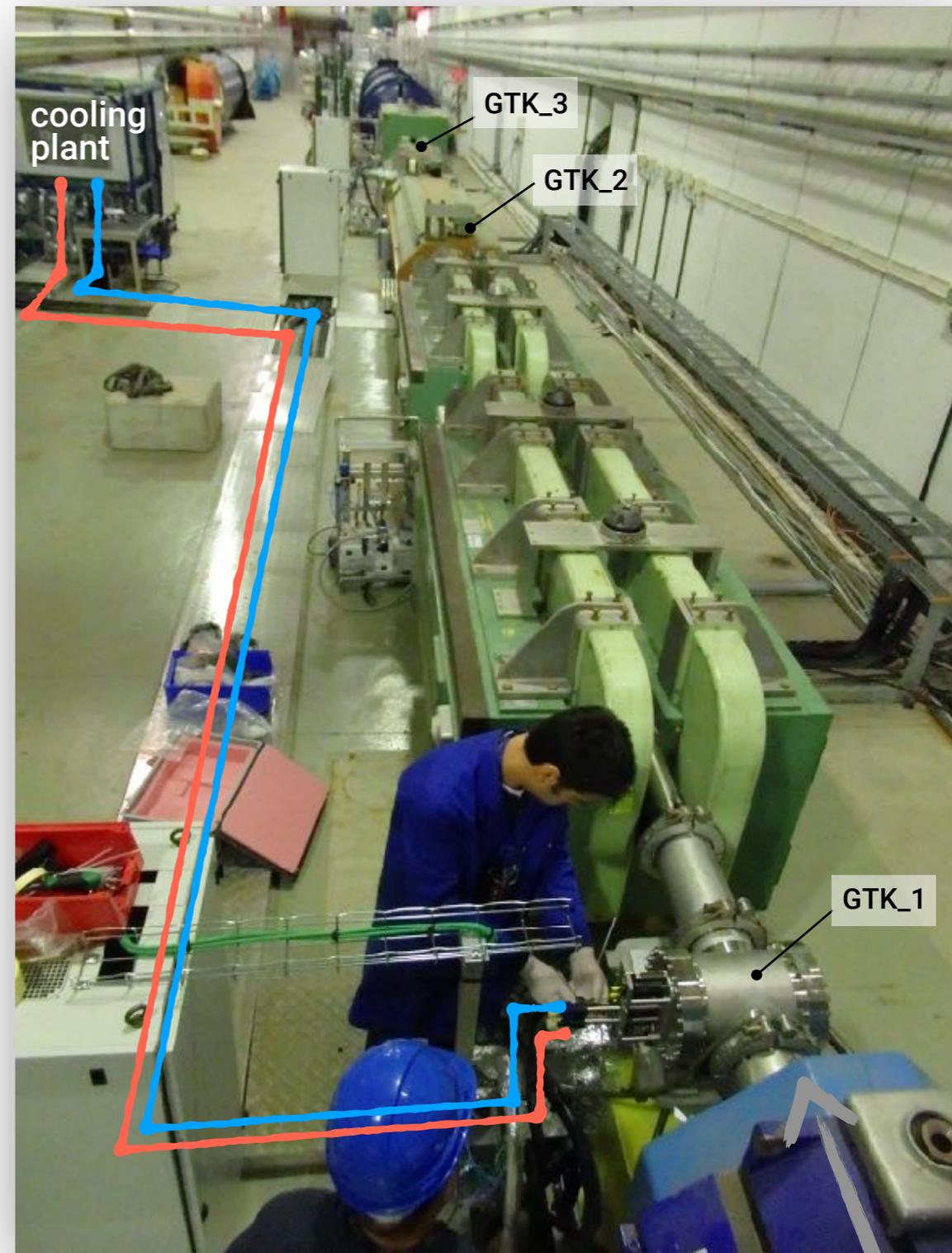
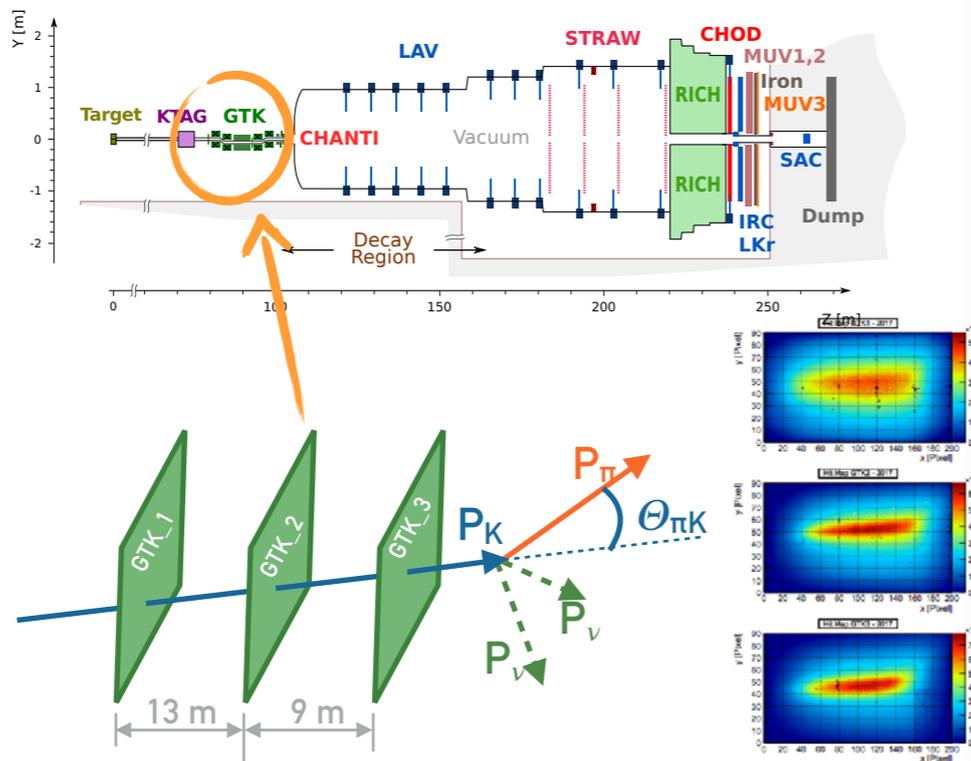


# NA62 GigaTracker

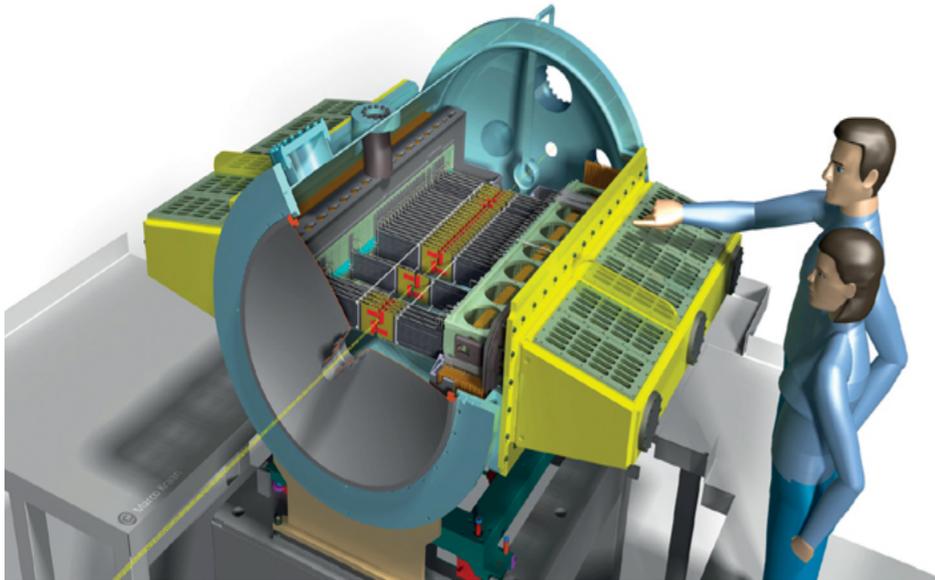


# The GTK in the NA62 experiment

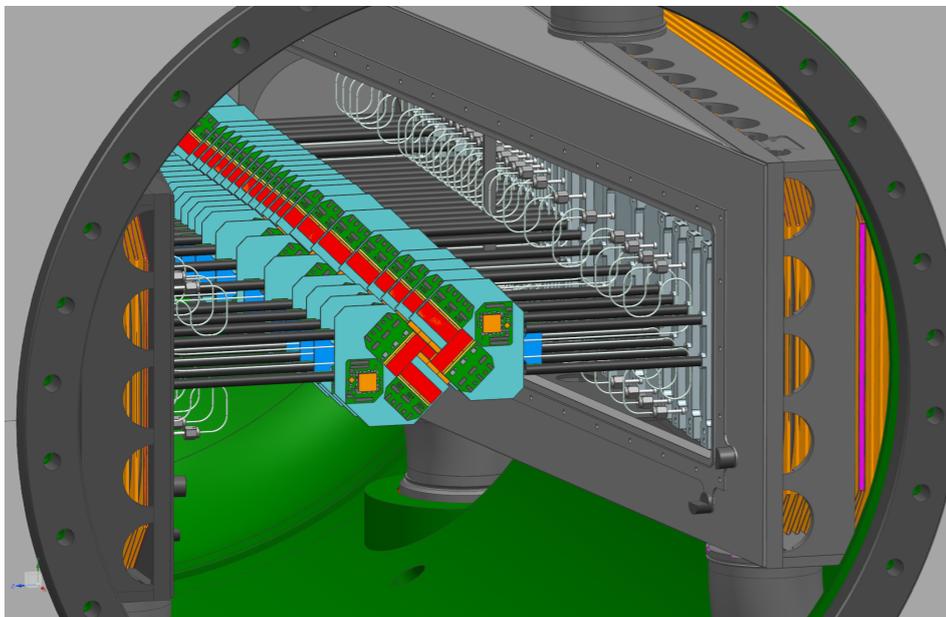
- **2014** - Installation of the first GTK.
- **2016-2018** - Physics runs with 3 GTK detectors.
- **2019-2020** - (LS2) construction of the GTKs for 2021-2022.
- At nominal beam intensity the detectors are exposed to a fluence corresponding to  $4 \times 10^{14}$  neq /cm<sup>2</sup> in one year (200 days) of data taking.
- In order to minimise radiation-induced damages, the detectors are operated at approximately -15°C in vacuum ( $\sim 10^{-6}$  mbar).
- Detectors have to be replaced every 100 days.
- GTK **designed to be replaced rapidly** (<0.5 day intervention).



# LHCb VELO Upgrade

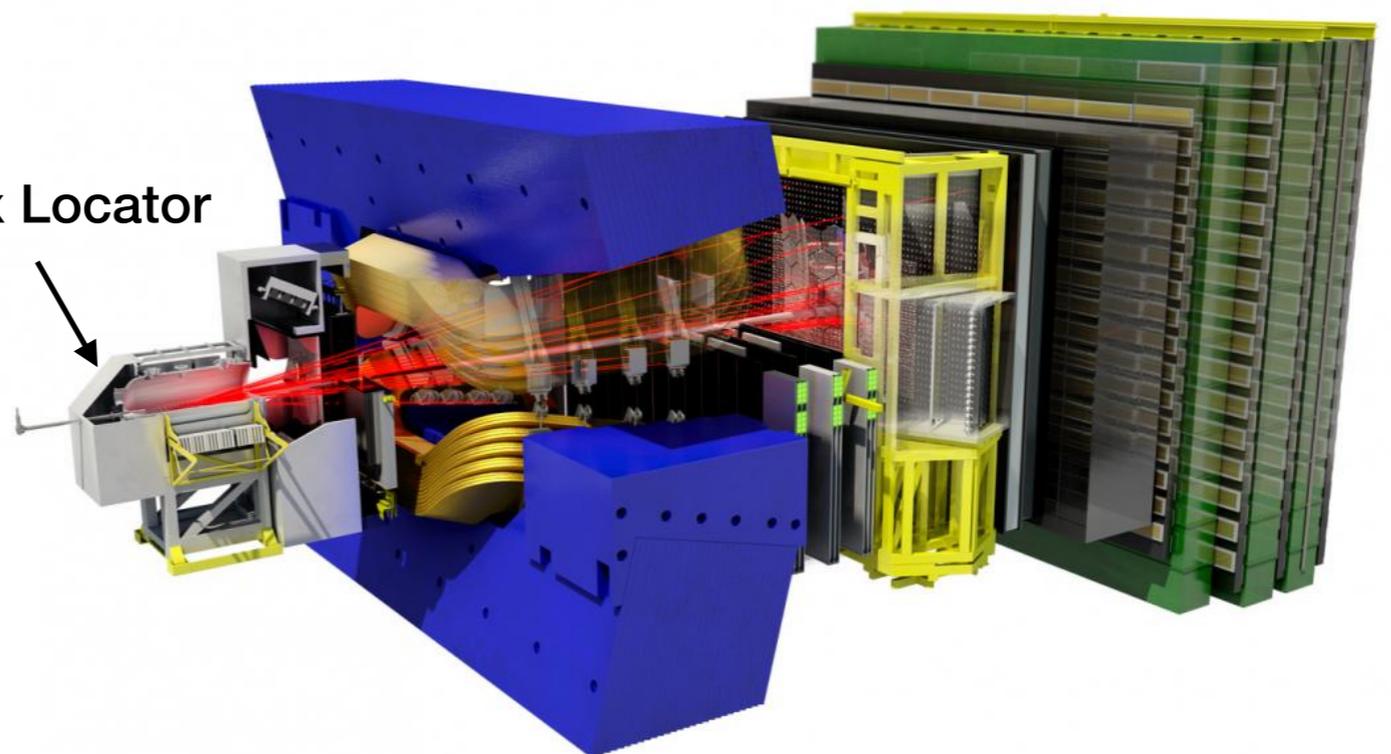


- Distance of closest pixel to LHC beam is 5.1 mm.
- Particle rate up to 600MHz/cm<sup>2</sup>.
- Very high radiation dose
  - $4 \times 10^{14}$  neq /cm<sup>2</sup> for 50 fb<sup>-1</sup>,
  - and non-uniform radiation.
- Very high data rates
  - up to ~15 Gbit/s for central ASICs and 2.9 Tbit/s in total.
- Sensor temperature < -20°C (CO<sub>2</sub> @ -30°C).
- Total maximum power dissipation per module is ~30 W. Nearly 1W/cm<sup>2</sup>.
- Inside vacuum vessel.



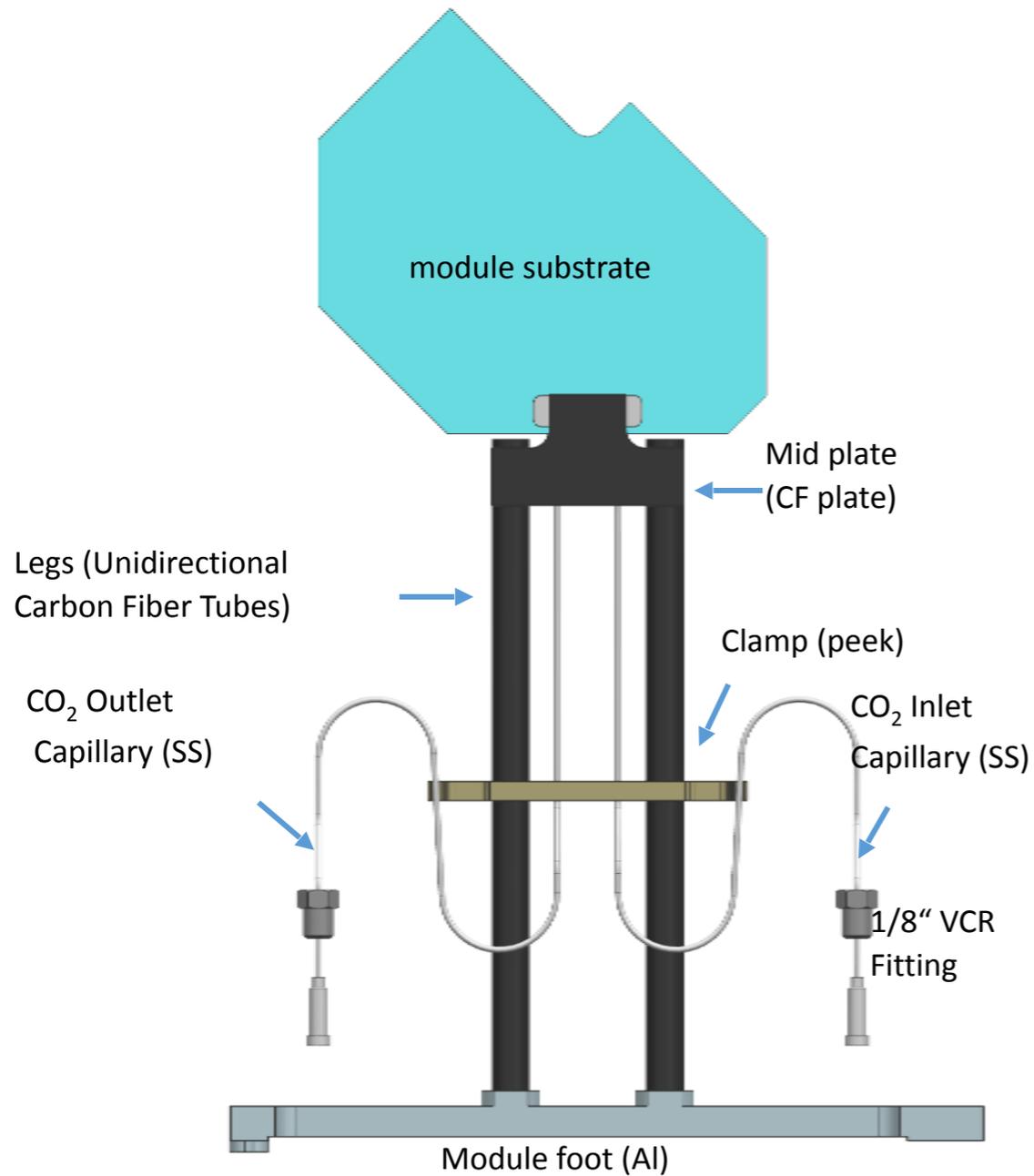
**52 modules (26 per side)**

Vertex Locator

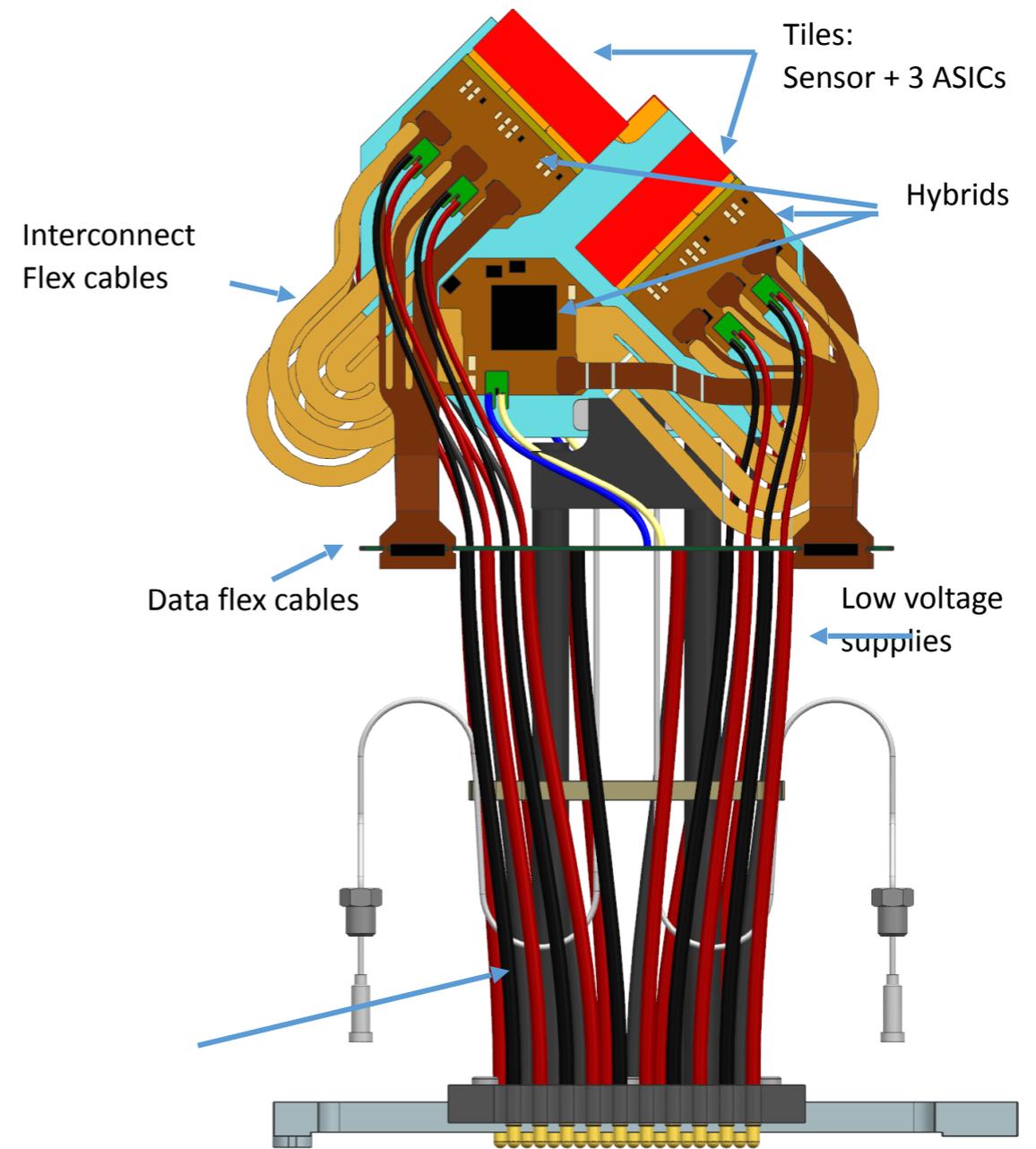


# Module Design

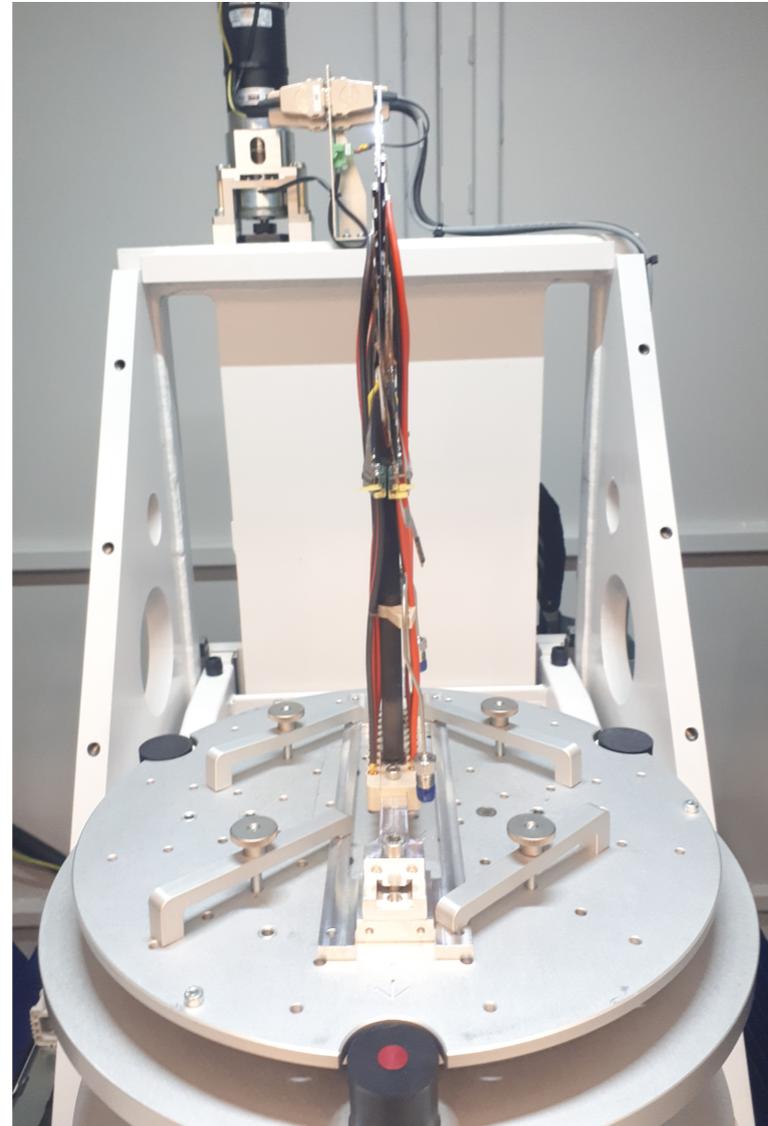
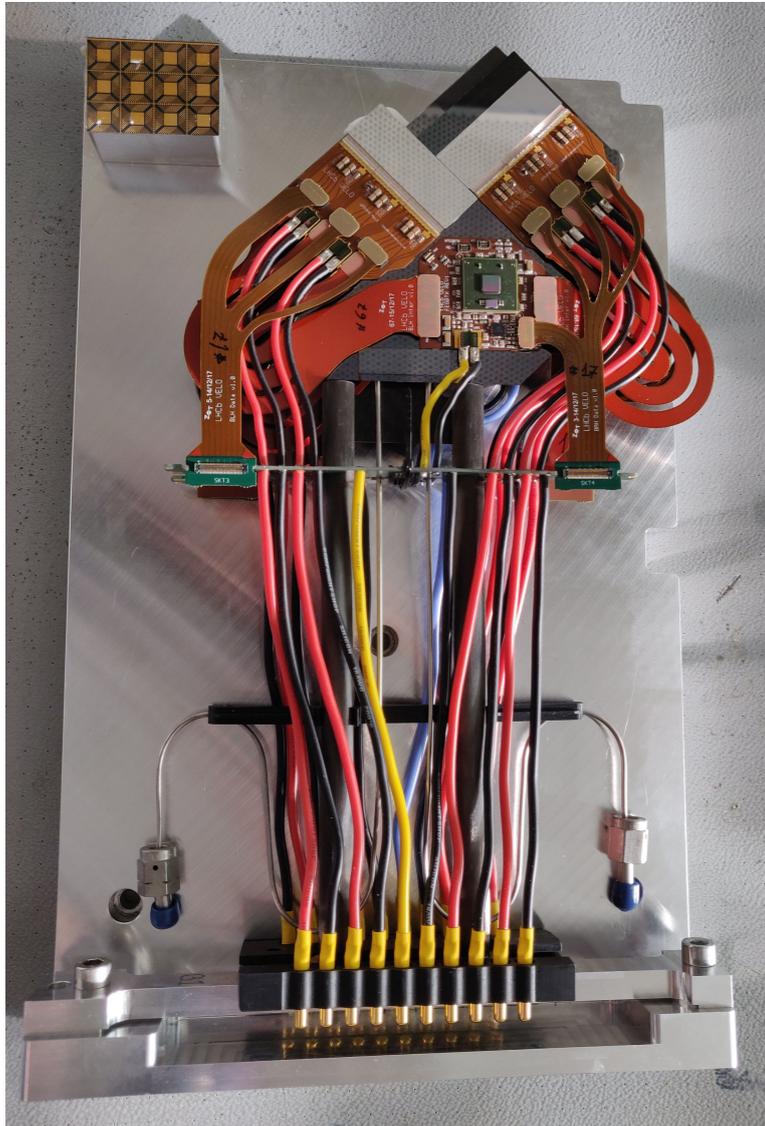
“Bare” Module



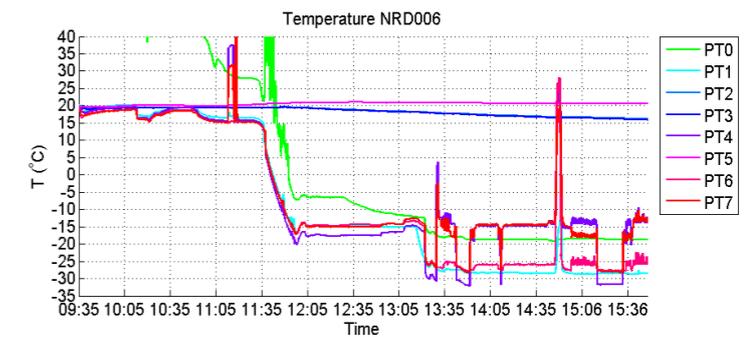
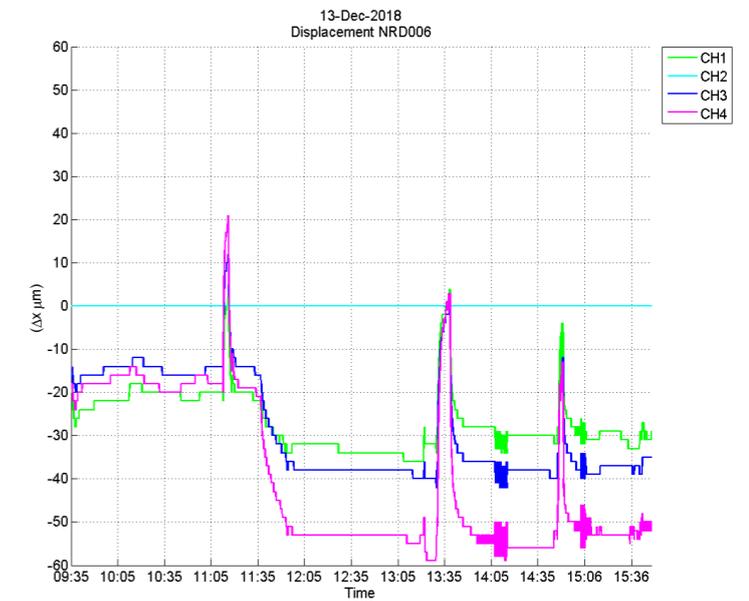
“Full” Module



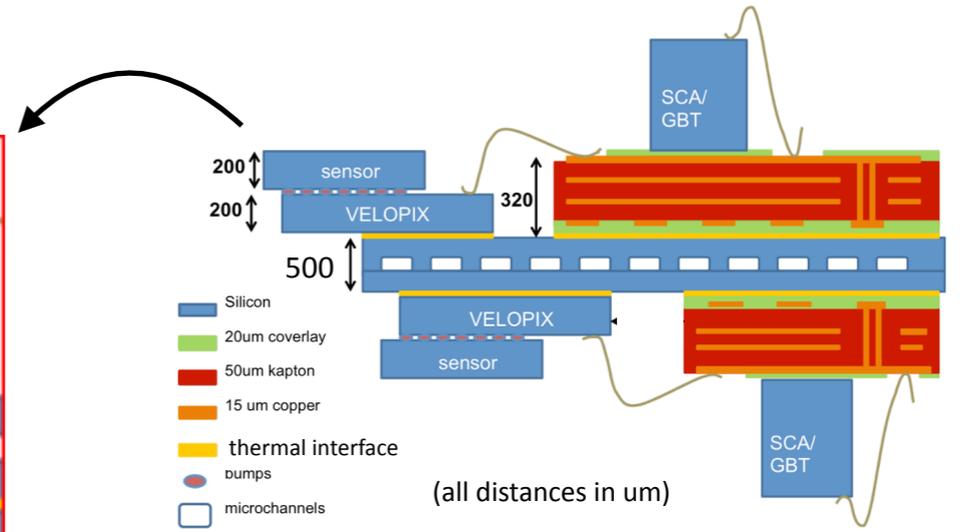
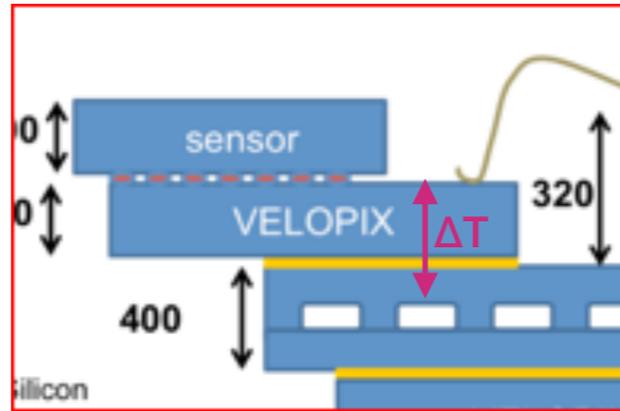
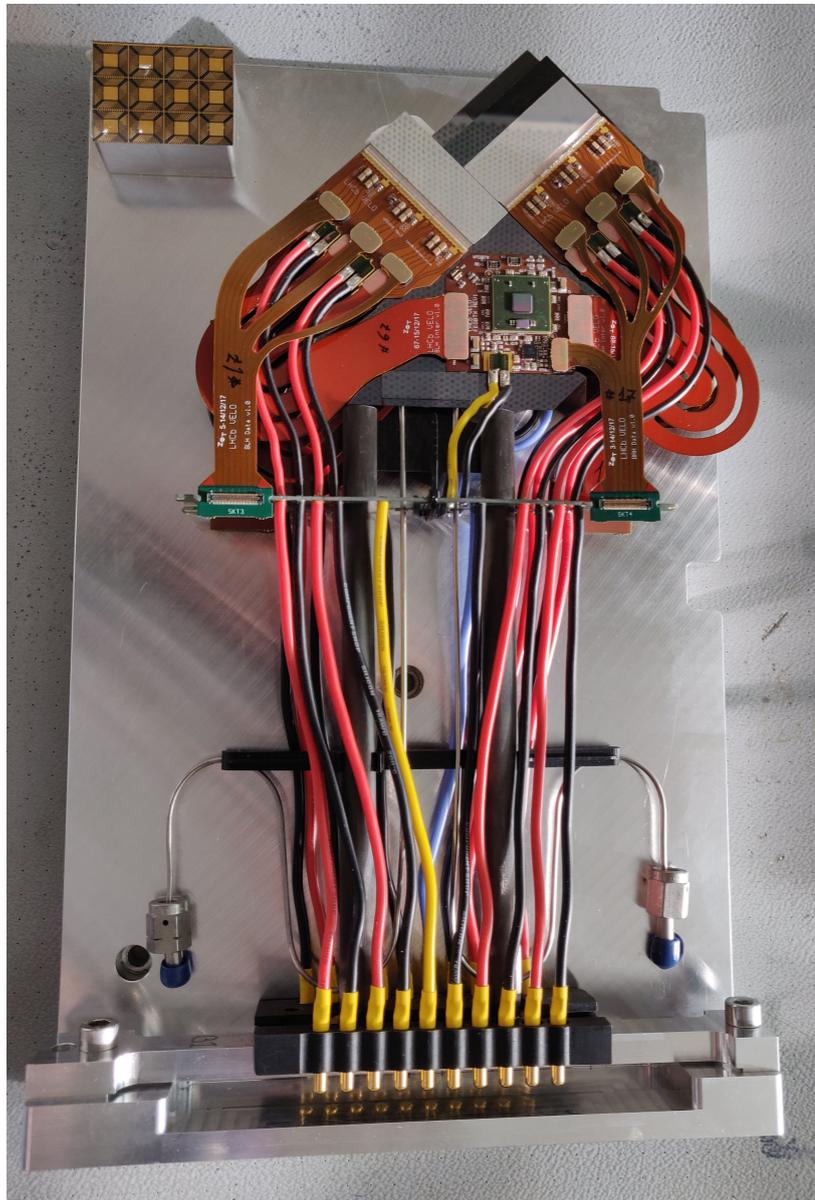
# VELO Module



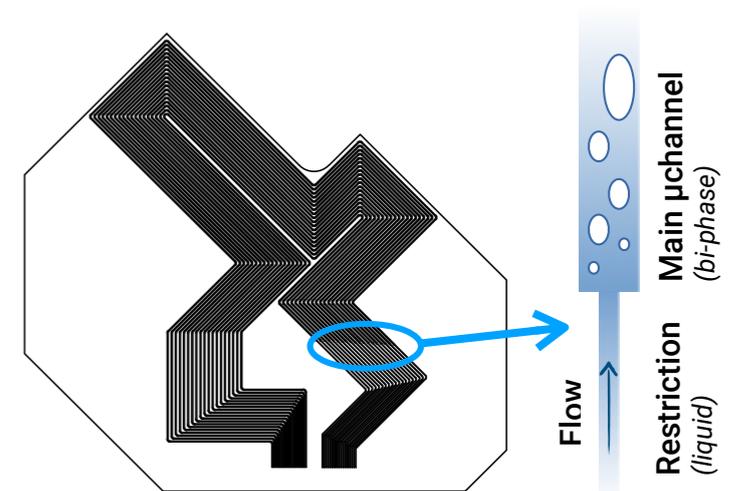
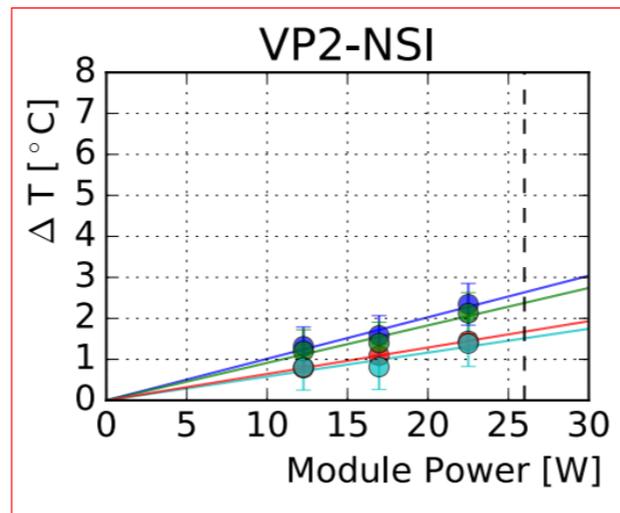
The tip of the module is displaced by less than  $40 \mu\text{m}$  when cooling from room temperature  $+20^\circ\text{C}$  to  $-30^\circ\text{C}$



# VELO Module

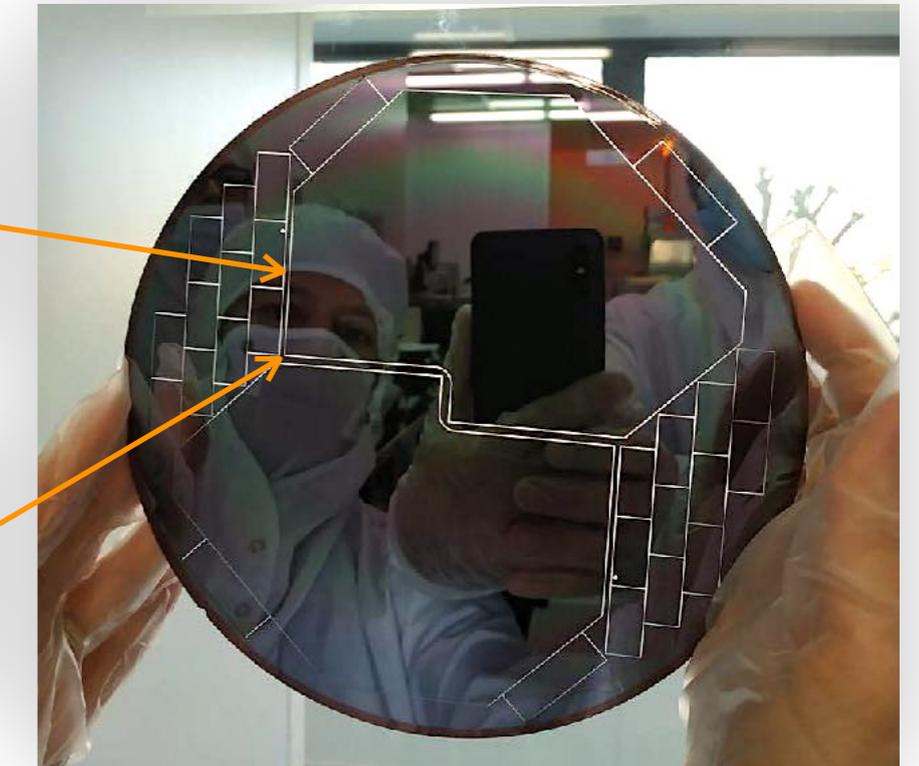
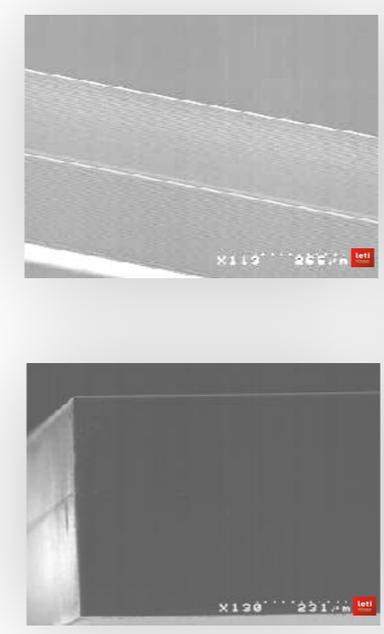
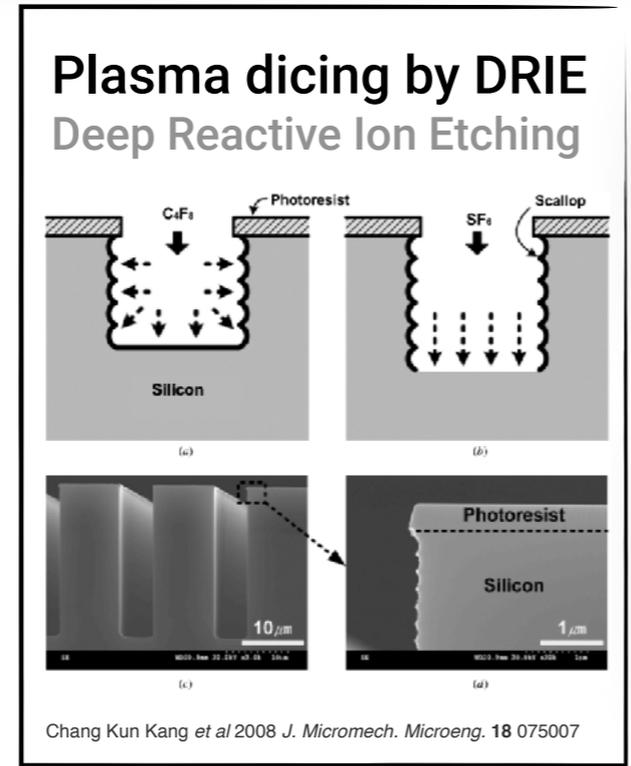
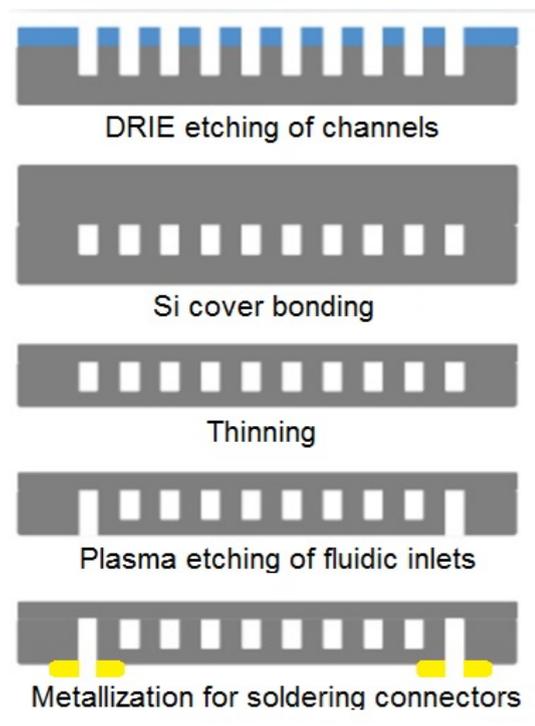
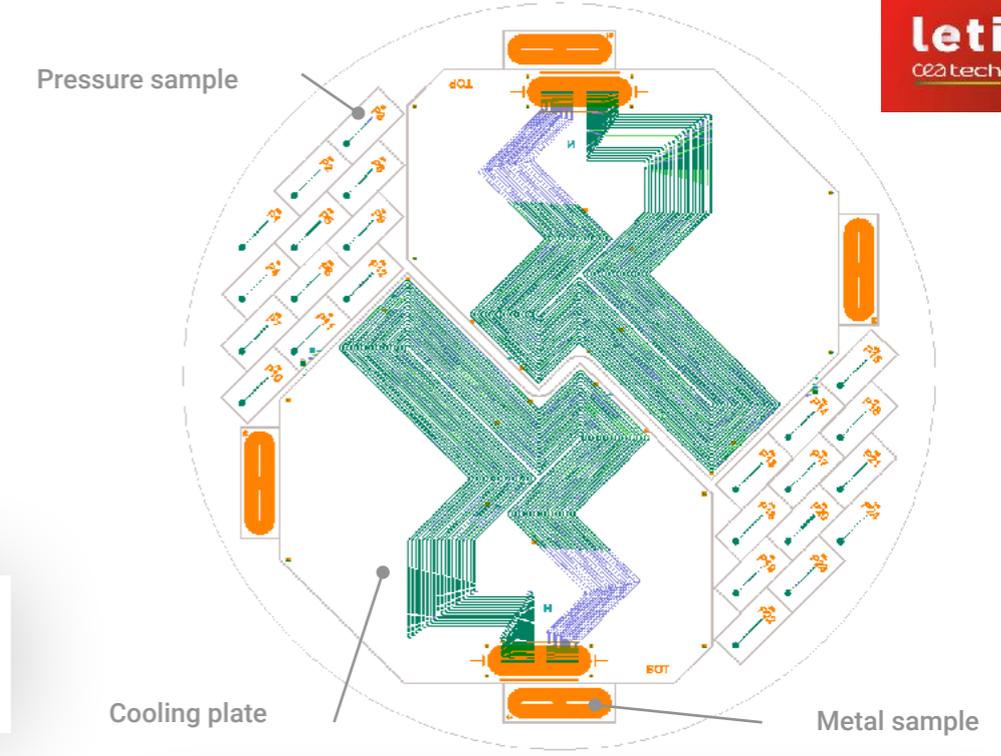
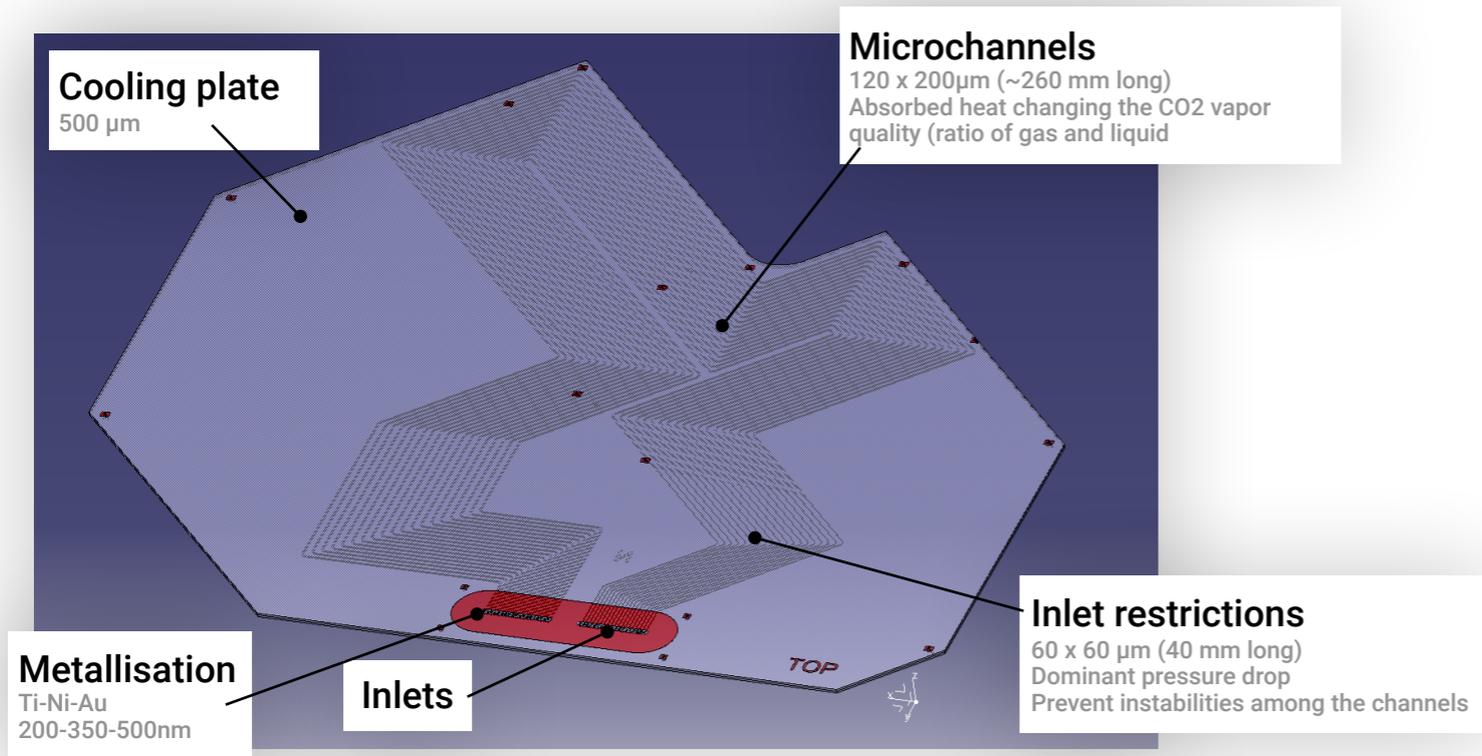


For 22W dissipated in the module the ASIC temperature is < 3C above CO2 cooling liquid temperature. (Stycast glue layer thickness < 100 μm)



Microchannels designed to bring the coolant under the heat sources.

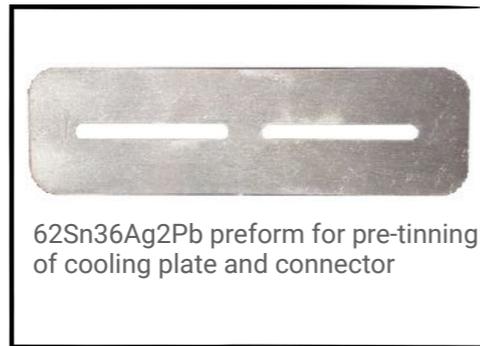
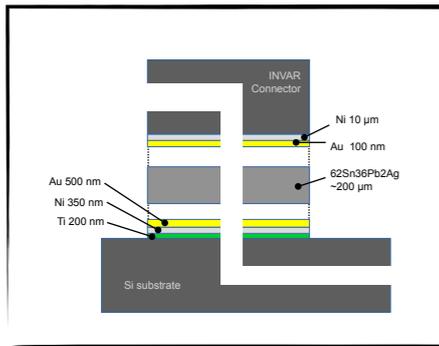
# microfabrication of the VELO cooling plates



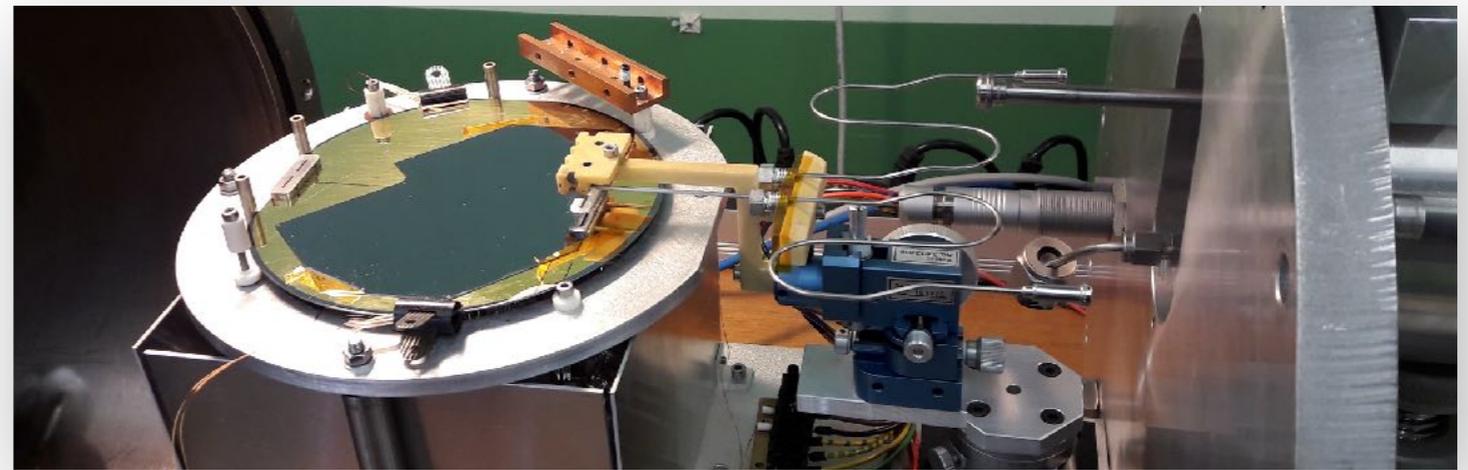
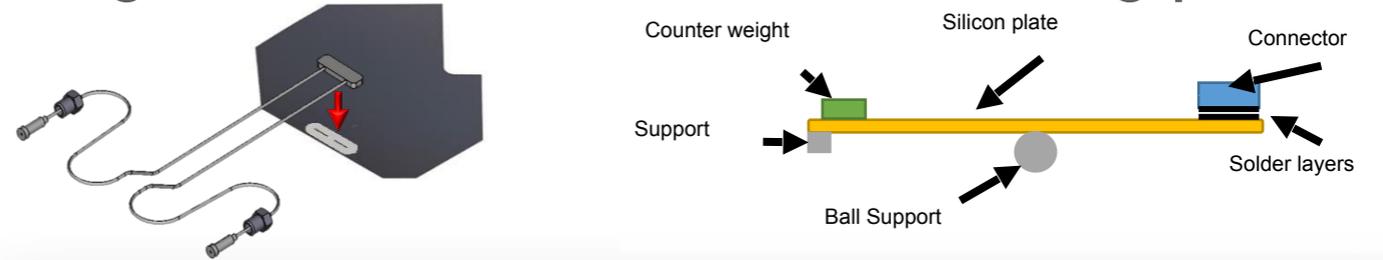
Leti-3S received in December 2019 an LHCb Industry Award to acknowledge their outstanding contribution for the successful manufacturing of the microchannel cooling plates for the LHCb VELO LS2 Upgrade.



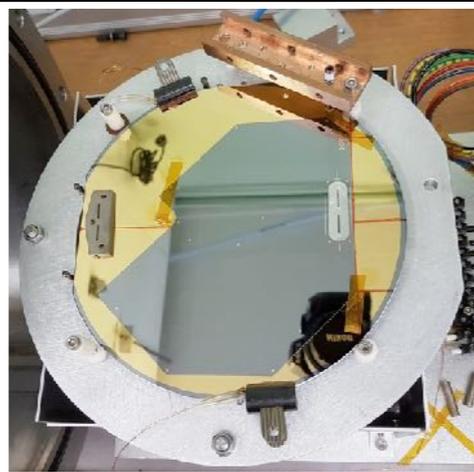
# soldering of metallic connectors



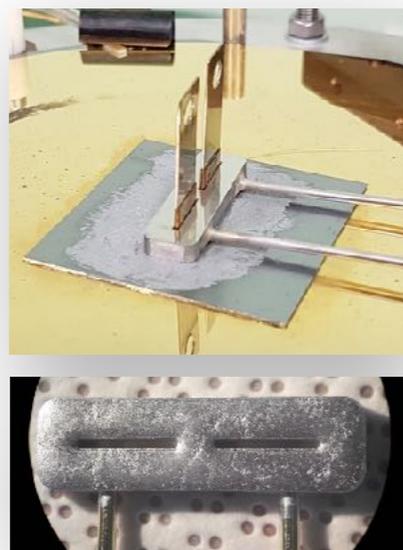
## 3. Alignment of connector to cooling plate



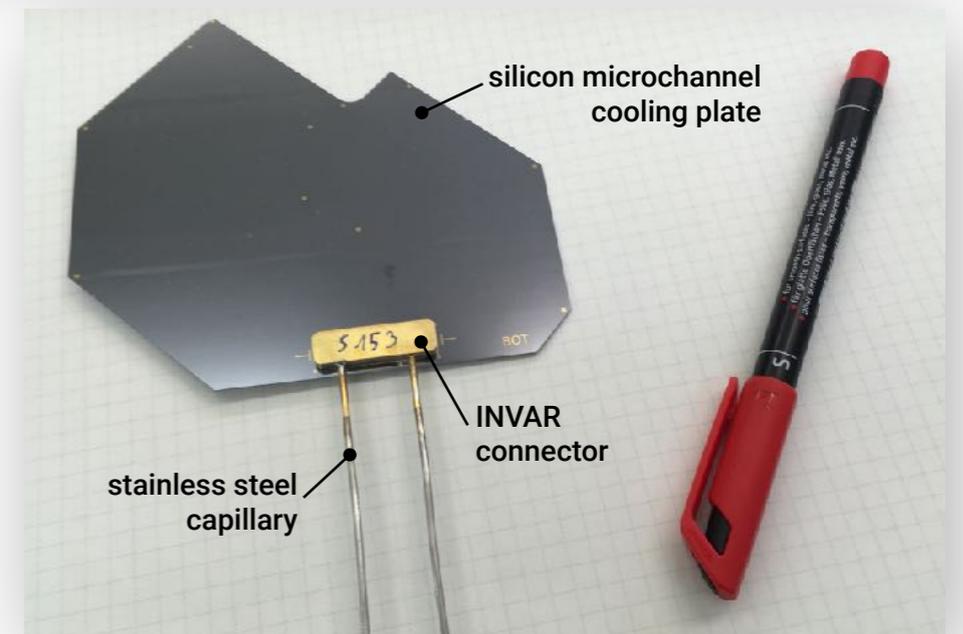
## 1. Pre-tinning of cooling plate



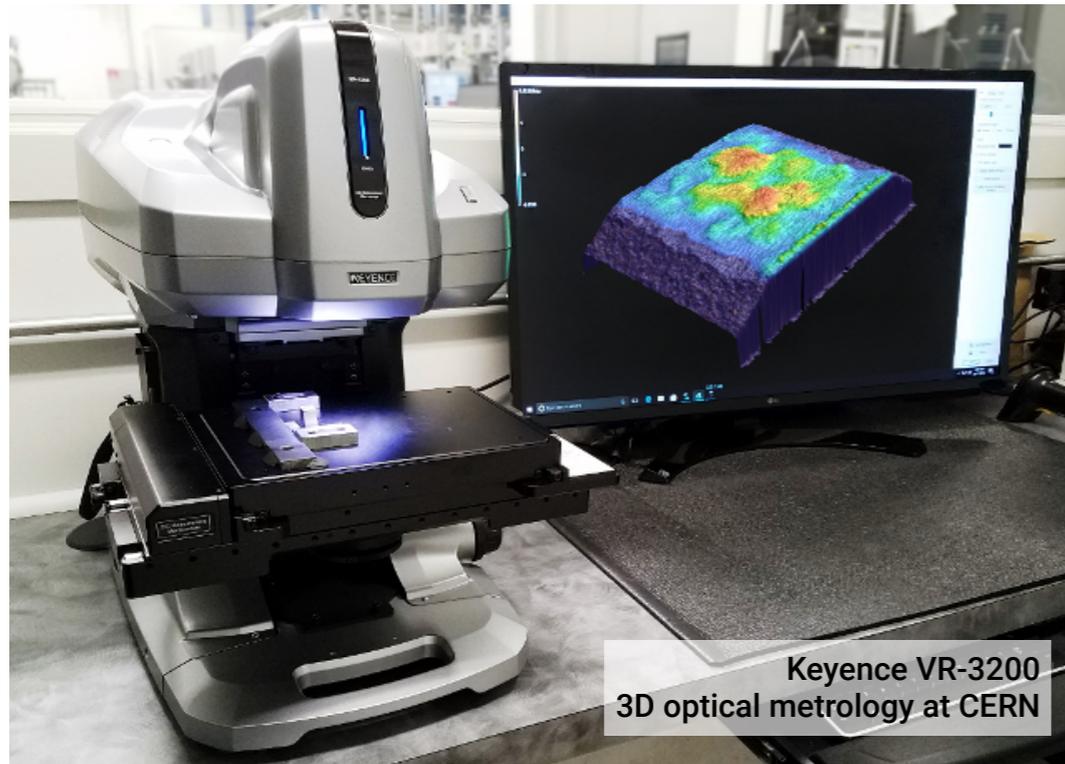
## 2. Pre-tinning of connector



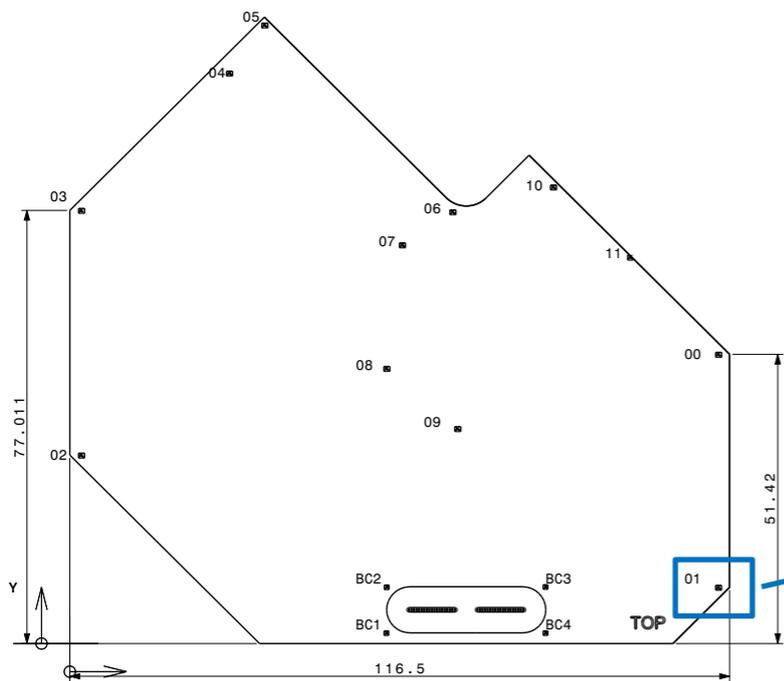
## 4. Soldering



# cooling plates planarity

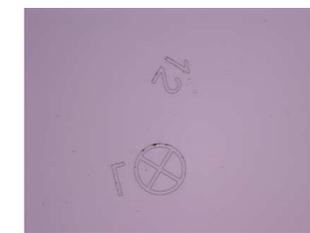
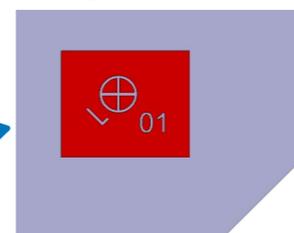


	before soldering	after soldering
planarity measurement		
min.	-60 $\mu\text{m}$	-50 $\mu\text{m}$
max.	+26 $\mu\text{m}$	+25 $\mu\text{m}$
variation	86 $\mu\text{m}$	75 $\mu\text{m}$



- Slight change on the planarity of the cooling plates.
- No significant stress generated by the soldering.
- The cooling plate is the backbone of the mechanical assembly of the VELO module.

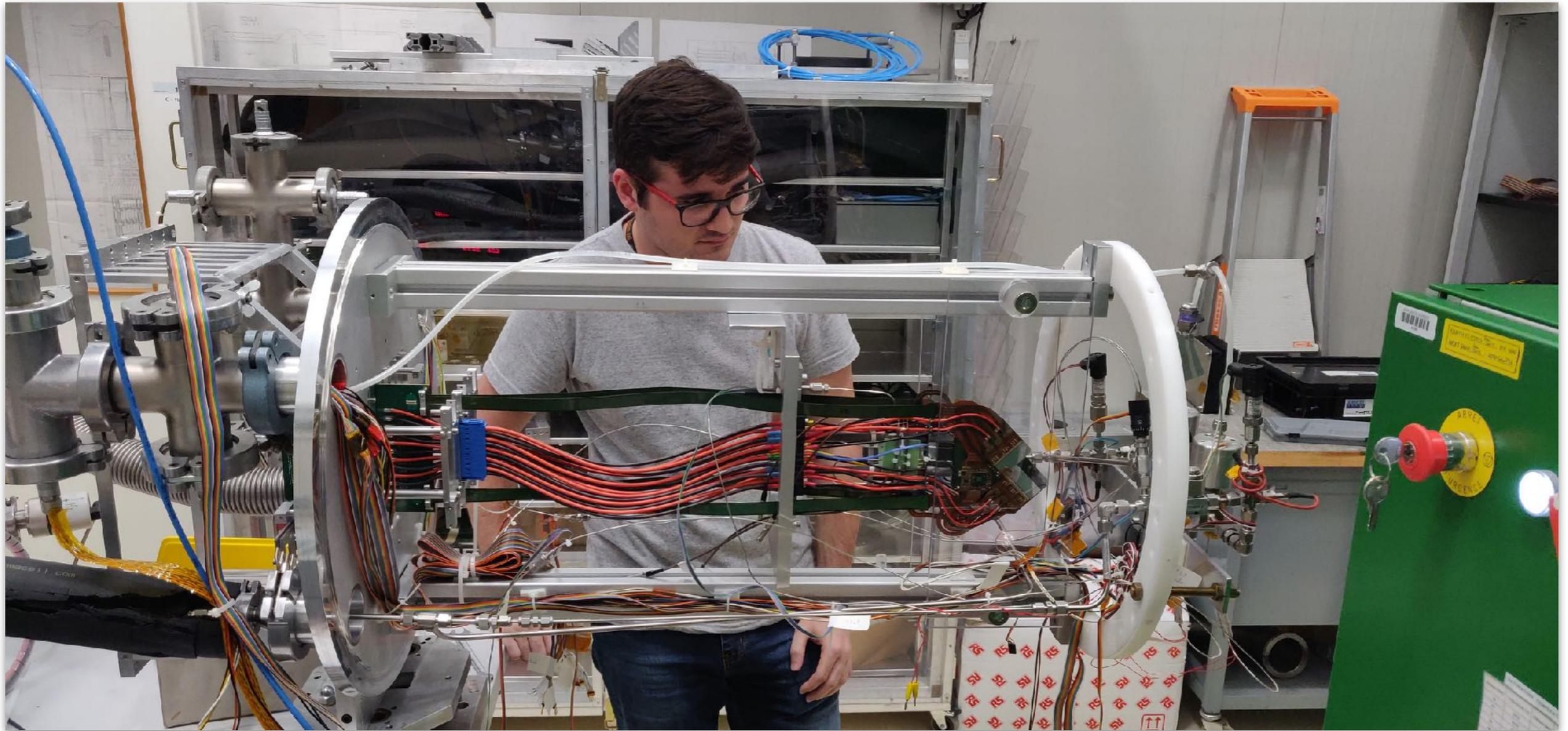
Alignment marks for module assembly



patterned on metal

etched in silicon

# VELO module under test



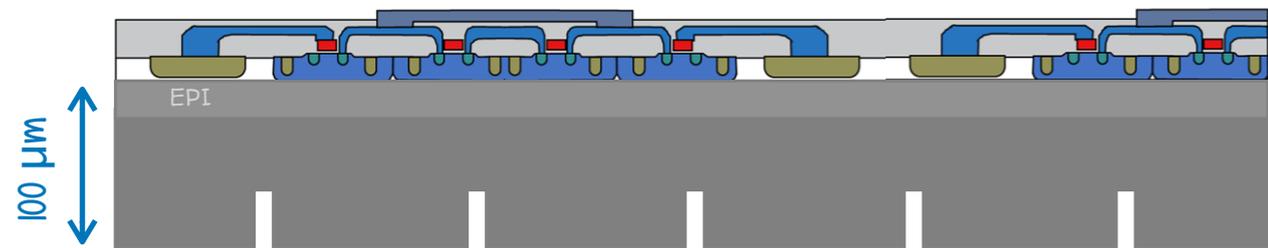
© Oscar Augusto de Aguiar Francisco, CERN, Feb. 2019

# Next steps..

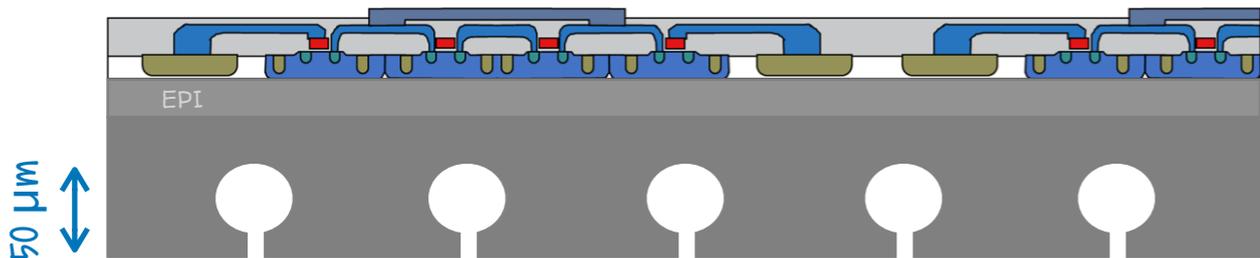
**Embedding channels in detectors**  
**Getting rid of the fluidic connectors**

# BCTs on the backside of monolithic detectors

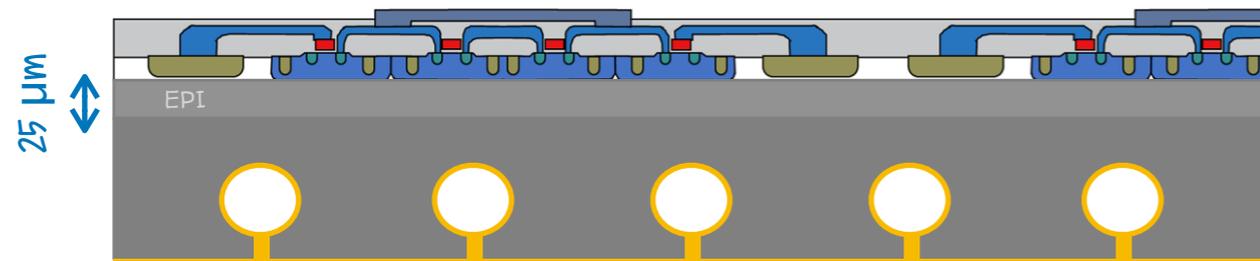
CMOS-compatible post-processing of single dies.



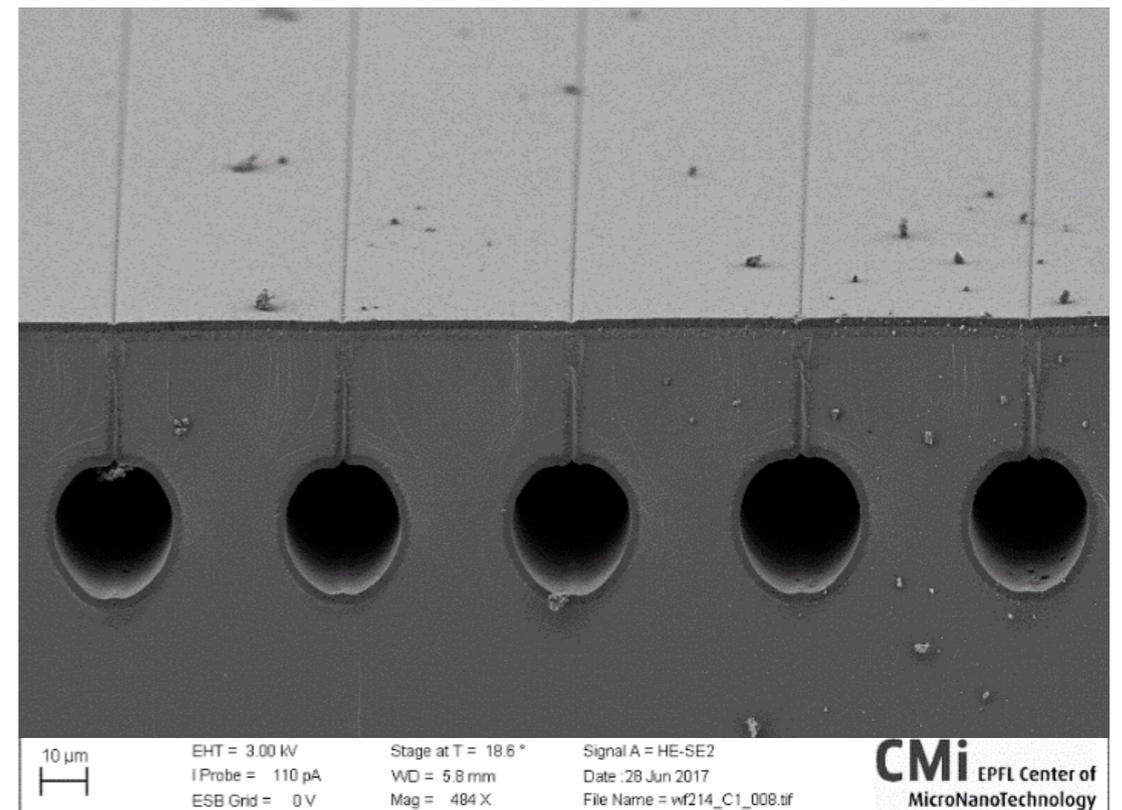
DRIE OF 30 μm DEEP TRENCHES (3 x 10 μm)



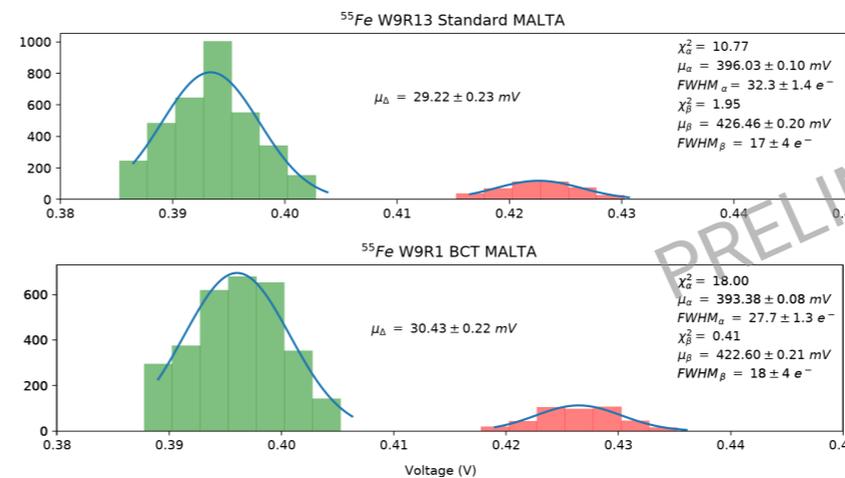
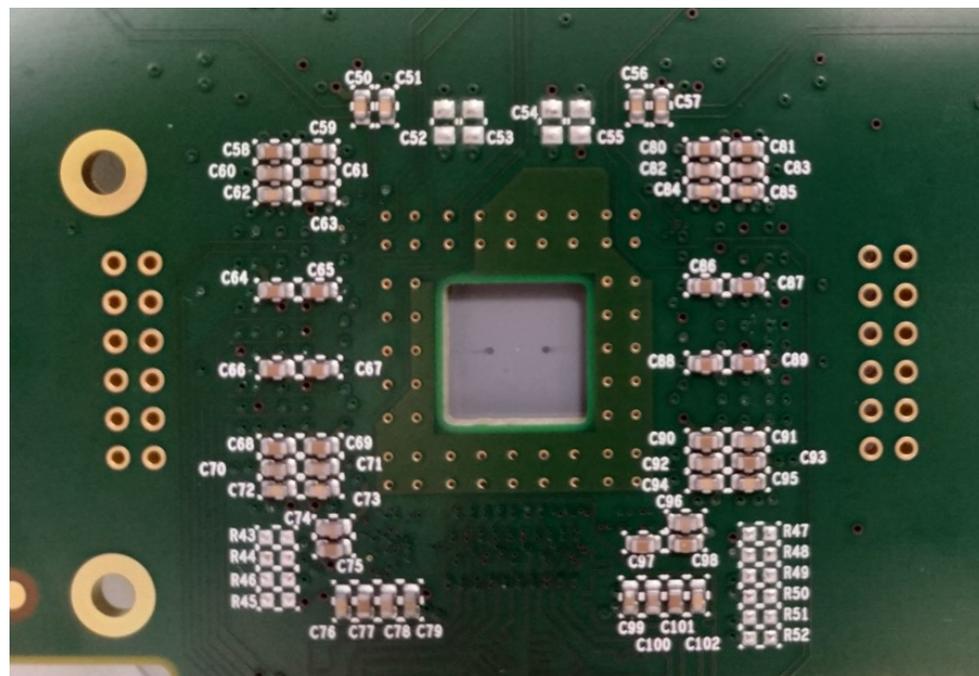
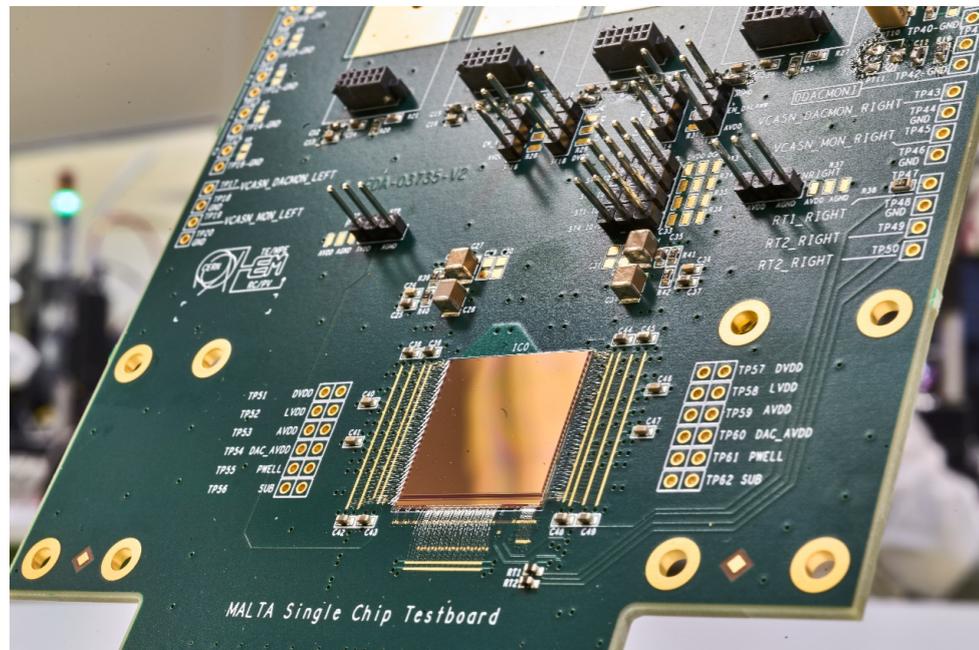
XeF<sub>2</sub> ETCHING OF MICROCHANNELS (diam. 40 μm)



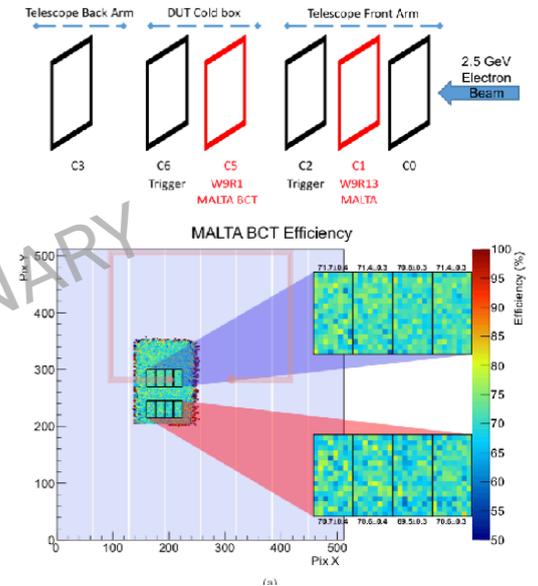
TRENCHES FILLED WITH PARYLENE (5 μm)



# Performance of MALTA with BCTs



$^{55}\text{Fe}$  source scan



test beam

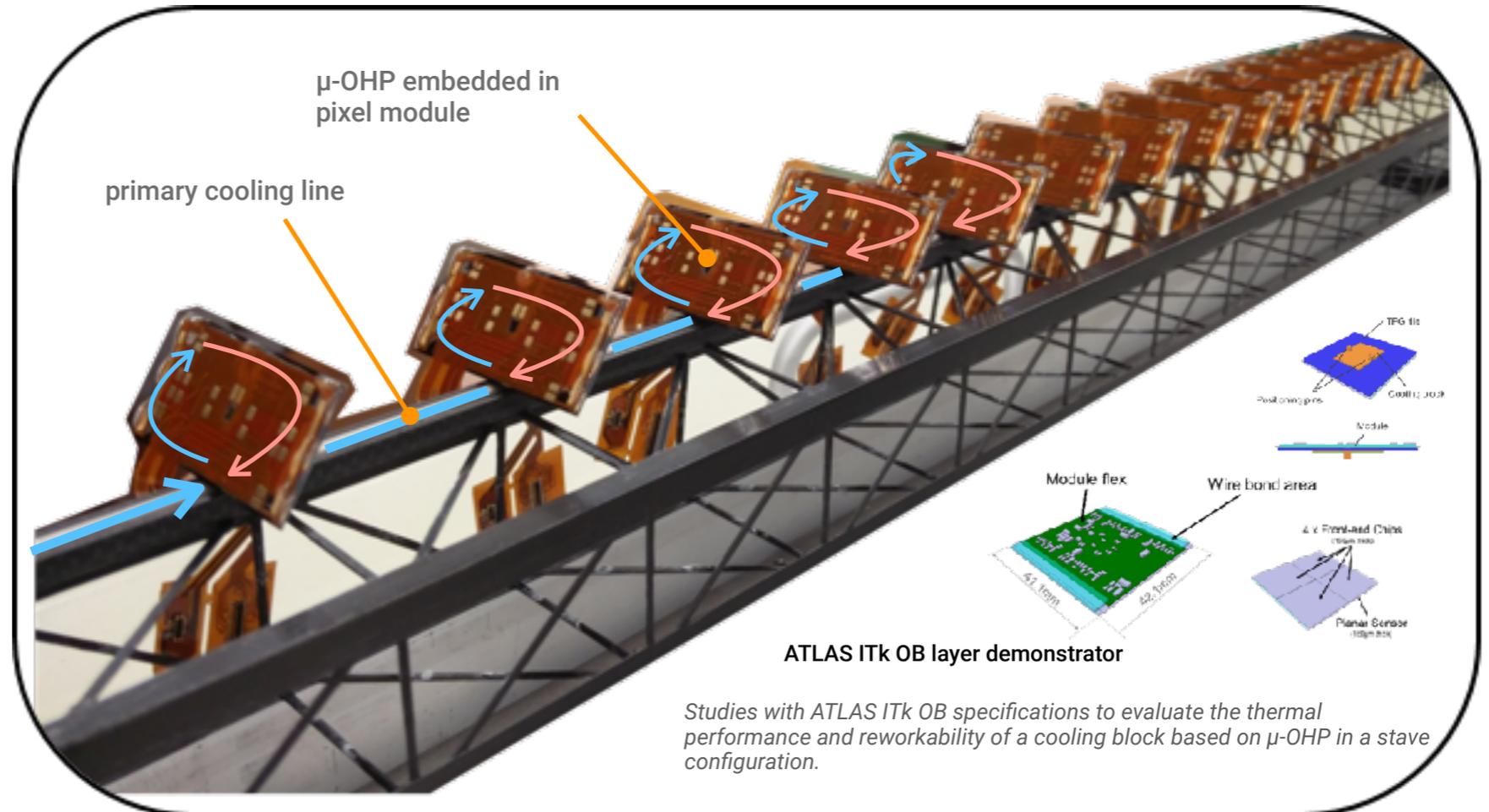
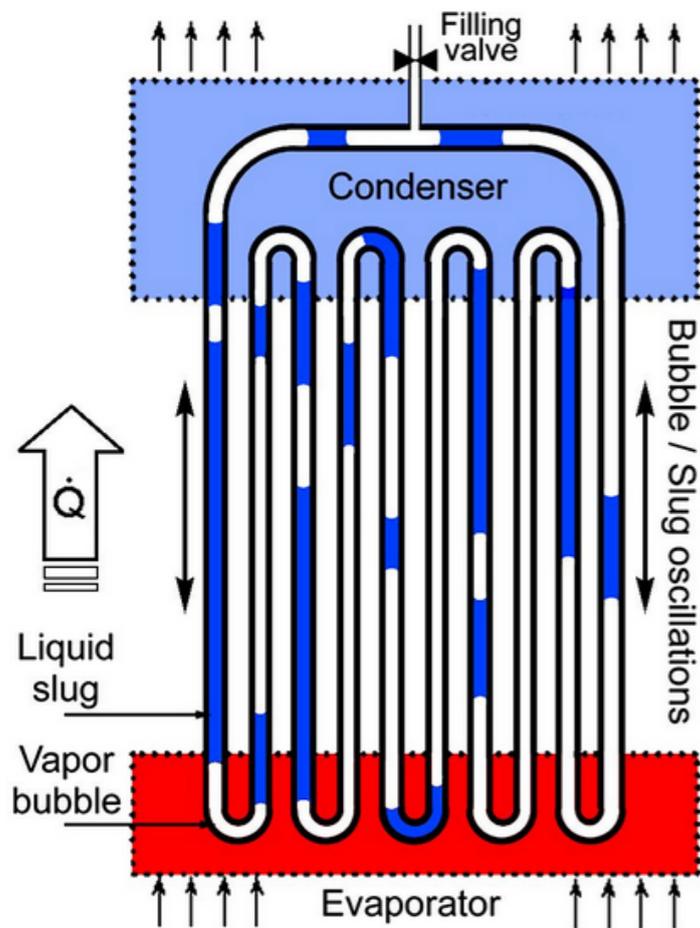
## $^{55}\text{Fe}$ source scan

- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA

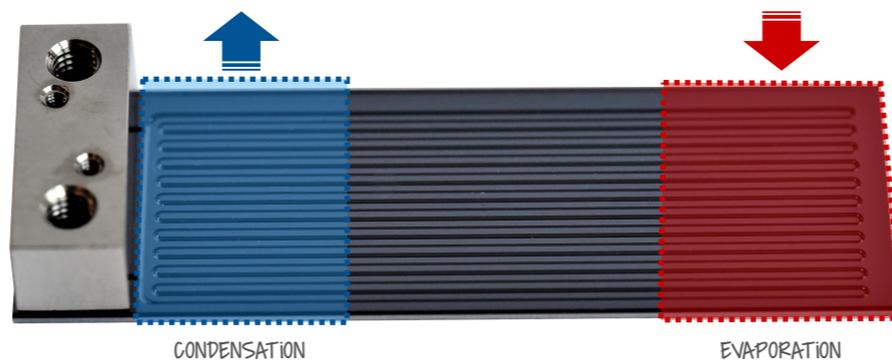
## Collection Efficiency

- Readout issue reduced the efficiency of ALL detectors to  $\sim 70\%$
- Comparable efficiency for the different ROIs

# Micro-oscillating heat pipes



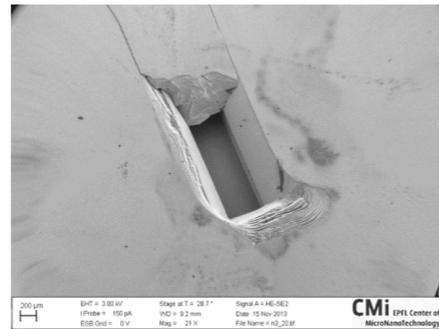
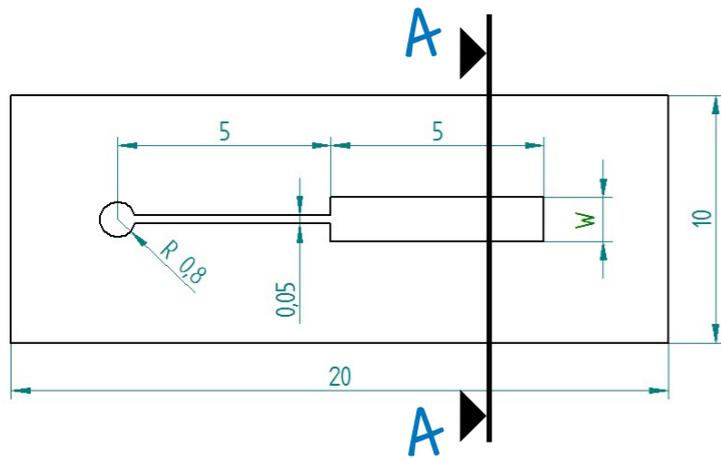
Studies with ATLAS ITk OB specifications to evaluate the thermal performance and reworkability of a cooling block based on  $\mu$ -OHP in a stave configuration.



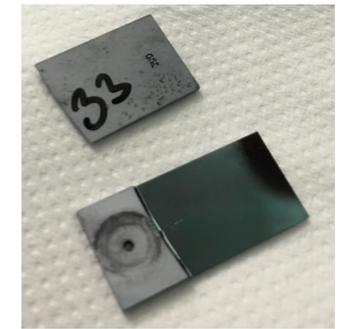
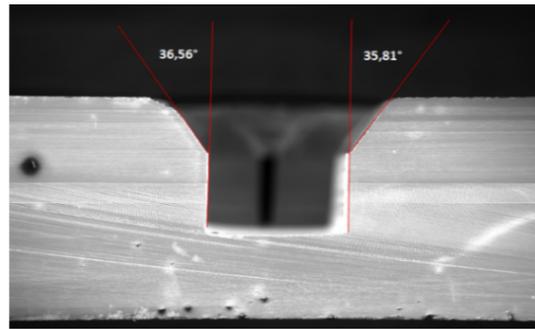
# Pressure Resistance

EDMS doc no [CERN-0000191313](#)

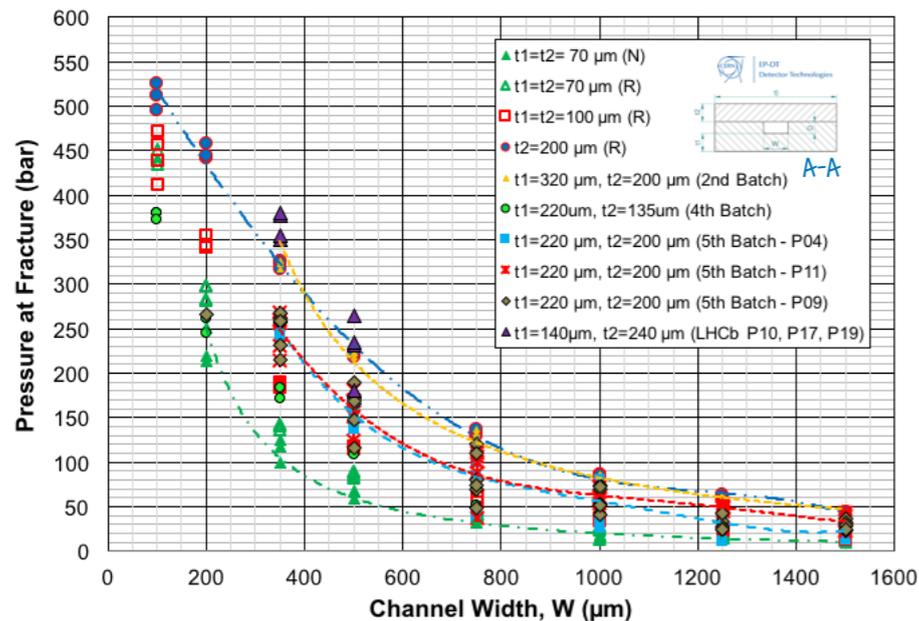
- **Standard samples** used for the **QA/QC** of the LHCb and NA62 cooling plates as well as for the investigation of **new fabrication techniques** (bonded wafers, buried channels, 3D-printed devices in plastics, ceramics,...).



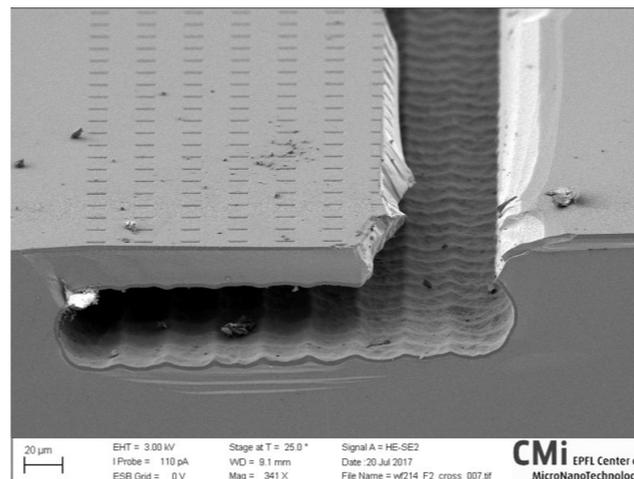
FRACTURE OF BONDED WAFERS



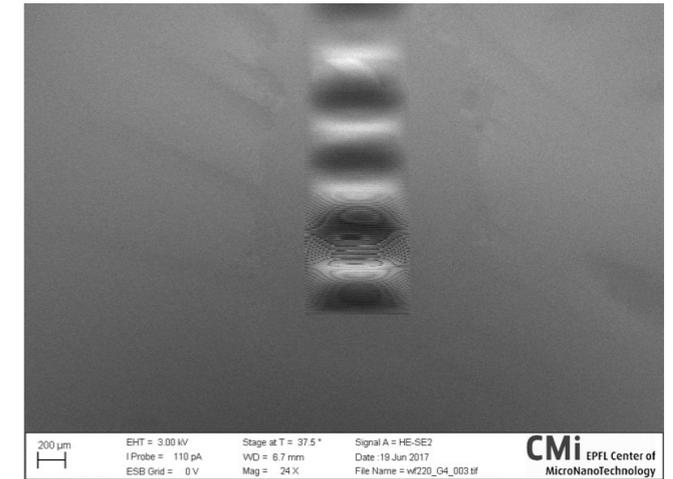
DELAMINATION OF BONDED WAFERS



BURIED CHANNELS



FRACTURE



DEFORMATION

# summary

- The NA62 experiment has pioneered the use of silicon microchannel cooling plates with **liquid C<sub>6</sub>F<sub>14</sub>** for the thermal management of the **GTK pixel detectors**.
- The LHCb experiment will pioneer the use of **evaporative CO<sub>2</sub>** in silicon microchannels for the **LS2 Upgrade of the VELO**.
- Current developments are aiming at eliminating connectors with **stand-alone microfluidic circuits** such as heat pipes and **embedding the microchannels into monolithic** pixel detectors with **CMOS-compatible microfabrication** processes.