Large Silicon Systems
3rd FCC Physics and Experiment Workshop
CERN, 13-17 January 2020

Attilio Andreazza
(Università di Milano and INFN)
Outline

• Silicon systems proposed for FCC-ee
  – CLD
  – IDEA

• “Standard” solutions: strip detectors
  – What we can learn from the HL-LHC upgrades

• Can we do something better?
  – Full pixel approach
  – Timing for particle ID

A collection of ideas from recent developments
FCC-ee Detectors: CLD

Full Silicon Tracker

• Pixel vertex detector:
   – Barrel, 3 double layers, r=1.7, 2.7, 5.7 cm
   – Disks, 3 double layers, |z|=16, 23, 30 cm
   – 0.6-0.7% $X_0$ per double layer

• Inner tracker:
   – Strips and pixels
   – 12.7<R<57.5 cm, |z|<2.2 m
   – 1.1-1.5% $X_0$ per layer

• Outer tracker:
   – Strips
   – 67.5<R<210 cm, |z|<2.2 m
   – 1.1-1.5% $X_0$ per layer
• **Vertex detector:** 5 (Depleted)MAPS layers \( r = 1.7 \text{ – } 34 \text{ cm} \)
• **Drift chamber (112 layers):** 4 m long, \( r = 35 \text{ – } 200 \text{ cm} \)
• **Si wrapper:** Strips, barrel at \( r=2 \text{ m} \) and drift chamber endplates \( z=2 \text{ m} \)

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• Similar approaches for ILC, CLIC, CepC:
  – High resolution **pixel vertex detector** \( O(\text{few m}^2) \)
  – Either **full silicon tracker** or **central gas chamber + Si wrapper** \( O(100 \text{ m}^2) \)

<table>
<thead>
<tr>
<th>Physics process</th>
<th>Measurands</th>
<th>Detector subsystem</th>
<th>Performance requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ZH, Z \to e^+e^-, \mu^+\mu^- )</td>
<td>( m_H, \sigma(ZH) )</td>
<td>Tracker</td>
<td>( \Delta(1/p_T) = 2 \times 10^{-5} \oplus \frac{0.001}{p(\text{GeV}) \sin 3/2 \theta} )</td>
</tr>
<tr>
<td>( H \to \mu^+\mu^- )</td>
<td>( \text{BR}(H \to \mu^+\mu^-) )</td>
<td>Vertex</td>
<td>( \sigma_{r\phi} = \frac{10}{p(\text{GeV}) \sin 3/2 \theta} \text{ (m)} )</td>
</tr>
<tr>
<td>( H \to b\bar{b}/c\bar{c}/gg )</td>
<td>( \text{BR}(H \to b\bar{b}/c\bar{c}/gg) )</td>
<td>ECAL</td>
<td>( \sigma_{E}/E = 3 \sim 4% \text{ at } 100 \text{ GeV} )</td>
</tr>
<tr>
<td>( H \to q\bar{q}, WW^<em>, ZZ^</em> )</td>
<td>( \text{BR}(H \to q\bar{q}, WW^<em>, ZZ^</em>) )</td>
<td>HCAL</td>
<td>( \Delta E/E = \frac{0.20}{\sqrt{E(\text{GeV})}} \oplus 0.01 )</td>
</tr>
<tr>
<td>( H \to \gamma\gamma )</td>
<td>( \text{BR}(H \to \gamma\gamma) )</td>
<td>ECAL</td>
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</table>

**High precision measurement at end of tracking volume**

**Challenging requirements on detector material**

**Finely segmented vertex detector**
Depleted MAPS are an attractive candidate for the vertex region:

- Monolithic + low power = light structure
- I’ll not try to summarize here the Tuesday afternoon session

After years of R&D monolithic sensors for HEP move to CMOS MAPS in mainstream technology

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc

Smaller feature size technologies allow lower analog and digital power consumption per channel and smaller pixels but power density is very important to contain voltage drops especially for large area devices.

Very fast charge collection in smaller pixels gives better timing resolution and also better radiation tolerance

Depleted substrate

But also CLIC Mu2e ARCADIA JADEPIX...
• Strips are the natural solution for the large area of the trackers:
  – Far from the interaction region: lower particle rate
  – Less channels: less power, less data connection
  – Simpler detector than pixels
## CMS Outer Tracker modules

<table>
<thead>
<tr>
<th></th>
<th>2S module</th>
<th>PS module</th>
</tr>
</thead>
<tbody>
<tr>
<td>~2 × 90 cm(^2) active area</td>
<td>~2 × 45 cm(^2) active area</td>
<td></td>
</tr>
<tr>
<td>2 × 1016 strips: ~5 cm × 90 (\mu \text{m})</td>
<td>2 × 960 strips: ~2.4 cm × 100 (\mu \text{m})</td>
<td></td>
</tr>
<tr>
<td>2 × 1016 strips: ~5 cm × 90 (\mu \text{m})</td>
<td>32 × 960 macro-pixels: ~1.5 mm × 100 (\mu \text{m})</td>
<td></td>
</tr>
<tr>
<td>Front-end power</td>
<td>~5 W</td>
<td>Front-end power</td>
</tr>
<tr>
<td>Sensor power (−20°C)</td>
<td>~1.0 W</td>
<td>Sensor power (−20°C)</td>
</tr>
</tbody>
</table>

### Area
- **2S**: 192 m\(^2\)
- **PS**: 25 m\(^2\)
- **Pixels**: 4.9 m\(^2\)

### Power density
- **2S**: 27 mW/cm\(^2\)
- **PS**: 89 mW/cm\(^2\)
- **Pixels**: 700 mW/cm\(^2\)

### Module cost (TDR)
- **2S**: 26990 kCHF
- **PS**: 20780 kCHF
- **Pixels**: 11691 kCHF

### Cost per m\(^2\)
- **2S**: 140 kCHF/m\(^2\)
- **PS**: 830 kCHF/m\(^2\)
- **Pixels**: 2400 kCHF/m\(^2\)
## ATLAS Strip modules

### Table:

<table>
<thead>
<tr>
<th></th>
<th>Strip</th>
<th>Pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>165 m²</td>
<td>13 m²</td>
</tr>
<tr>
<td>Power density</td>
<td>43 mW/cm²</td>
<td>700 mW/cm²</td>
</tr>
<tr>
<td>Module cost (TDR)</td>
<td>36900 kCHF</td>
<td>25067 kCHF</td>
</tr>
<tr>
<td></td>
<td>224 kCHF/m²</td>
<td>1900 kCHF/m²</td>
</tr>
</tbody>
</table>

**Ref. 7-8**
Strip tracking parts are not that different from the current ATLAS and CMS upgrades:
- CLD has a coverage of 195 m²
- IDEA is about 2x50 m²

Lesser radiation damage and particle rate will probably make things simpler for the services:
- May operate at a higher temperature
- Lower power dissipation
- Data concentration on fewer data links
IS THERE ANYTHING NEW?
Option 1: Passive CMOS

- Implement passive structures in standard CMOS processes on high resistivity substrate
  - Alternative fabrication process for standard strip and pixel sensors: "fast and cheap"
  - Stitching to build large area sensors: should receive soon a run in LFoundry 150 nm

[Diagram showing strip layout and different pixel types]
Option 1: Passive CMOS

- Approach initially developed for pixel detectors, but actually interesting for strips where there is a lack of producers for very large detector surfaces.
  
  - ATLAS estimated of 400-500 kCHF/m² for a full CMOS run (including yield and spares)
  - Can be reduced since not all available layers at a foundry are needed: partial mask set
  - Potential to build “monolithic” strips by integrating readout electronics in the lattice
  - Possibility of large detector tiles

- **Cons:** very large startup costs: stitching+HR substrate usually requires to book full engineering runs)
Option 2: Full DMAPS Detector

• DMAPS used in the vertex, can operate also in the outer part of the tracker.

• **Performance-wise** is an improvement:
  – Unambiguous, precise measurement in both coordinate instead of asymmetric precision of stereo strips
  – One thin silicon layer instead of strip doublets

• More **practical** points:
  – **Homogeneous detector**
  – **Production size well within the capability of CMOS foundries**
  – The target power density of next generation DMAPS detector is comparable with HL-LHC strips
  – Cost is not so different, if one considers half silicon area is needed
  – **Stitching and/or multi-chip modules** are required to avoid excessive fragmentation (10x ALICE ITS)

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Sensor proposal: ATLASPix

**ATLASPix** is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 μm by 50 μm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

**ATLASPix3**

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200Ωcm, 180nm) just delivered
- 132 columns with 150μm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two end of column (EoC) blocks. EoC1 is attached to hit buffers and EoC2 to trigger buffers.

Similar detectors from LFoundry and TowerJazz will become available shortly.
Module Flex

Università and INFN di Milano: Attilio Andreazza, Mauro Citterio, Fabrizio Sabatini

Purpose is to build a **pseudo-quad module** for ATLAS
Test system functionality for large size detectors
Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests

Two basic ideas:
- Connector
- Integrated Pigtail
Option 3: Particle Identification

- Hadron identification is a feature of last generation $e^+e^-$ experiments
- Central tracking with gas detectors can provide good $dE/dx$

IDEA Drift Chamber
Hadron separation at $N\sigma$ by cluster counting method
Option 3: Particle Identification

- Hadron identification is a feature of last generation $e^+e^-$ experiments
- Central tracking with gas detectors can provide good $dE/dx$
- Can be complemented with timing measurements (TOF)
- Approach available also for full-silicon trackers

K/p separation with TOF detector at 2 m

dE/dx confusion region
Silicon timing detectors

- Recent developments have shown the silicon detector can achieve the required timing resolution.
- The key ingredient is signal multiplication (LGAD, 3D)

For application to the outermost tracking layers of FCC-ee:

- Higher spatial resolution
  (~10 μm pitch, compared to ~1 mm of HL-LHC timing layers)
- 100% fill factor
- Production process scalable to large volumes

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• A promising approach is to separate multiplication and charge collection functions:
  – Uniform multiplication layer
  – Segmented collection/induction electrodes

Improving the fill factor: iLGAD

Segmented multiplication layer:
  • Spatially inhomogeneous gain
  • Degraded resolution for inter-strip hits
  • Fill-factor problem

Non-segmented multiplication layer:
  • Uniform gain distribution
  • Promising timing results: ~20 ps
  • Unirradiated 285-μm iLGAD, laser-induced signal at 20°C
  • Thinner sensors under development
A promising approach is to separate multiplication and charge collection functions:

- Uniform multiplication layer
- Segmented collection/induction electrodes

**Resistive AC-coupled Silicon Detector**

- Non-segmented $p^+$ multiplication layer
- Resistive n-layer
- AC-coupled readout pads with thin dielectric layer
- AC pads define the readout pitch
- Position from interpolation of signal on nearby electrodes
  - Feasible if occupancy is low
  - Observed space resolution of few micrometers
• Most detector designs for future e+e- colliders foresee large area silicon tracking systems.
• From a principle point of view, they don’t look more challenging than the current HL-LHC upgrades.
• Nevertheless some of the current R&D may open new perspectives also in these systems.
• Some personally selected ideas presented here:
  – Applications of CMOS processes
  – Timing layers for hadron identification
• It will help to get people committed to a critical component of FCC-ee detectors.

Hope that was interesting enough and thanks for listening!
References

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BACKUP
IDEA Layout

Dual Readout Calorimeter

- Detector length 1300 cm
- Detector height 1100 cm
- Yoke 100 cm
- Magnet z = ± 300 cm
- DCH z = ± 200 cm
- Cal Rin = 250 cm
- Cal Rout = 450 cm
- DCH Rout = 200 cm
- DCH Rin = 30 cm

Silicon Wrapper

Preshower