Large Silicon Systems

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UNIVERSITÀ DEGLI STUDI DI MILANO
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Outline

- Silicon systems proposed for FCC-ee
  - CLD
  - IDEA
- "Standard" solutions: strip detectors
  - What we can learn from the HL-LHC upgrades
- Can we do something better?
  - Full pixel approach
  - Timing for particle ID

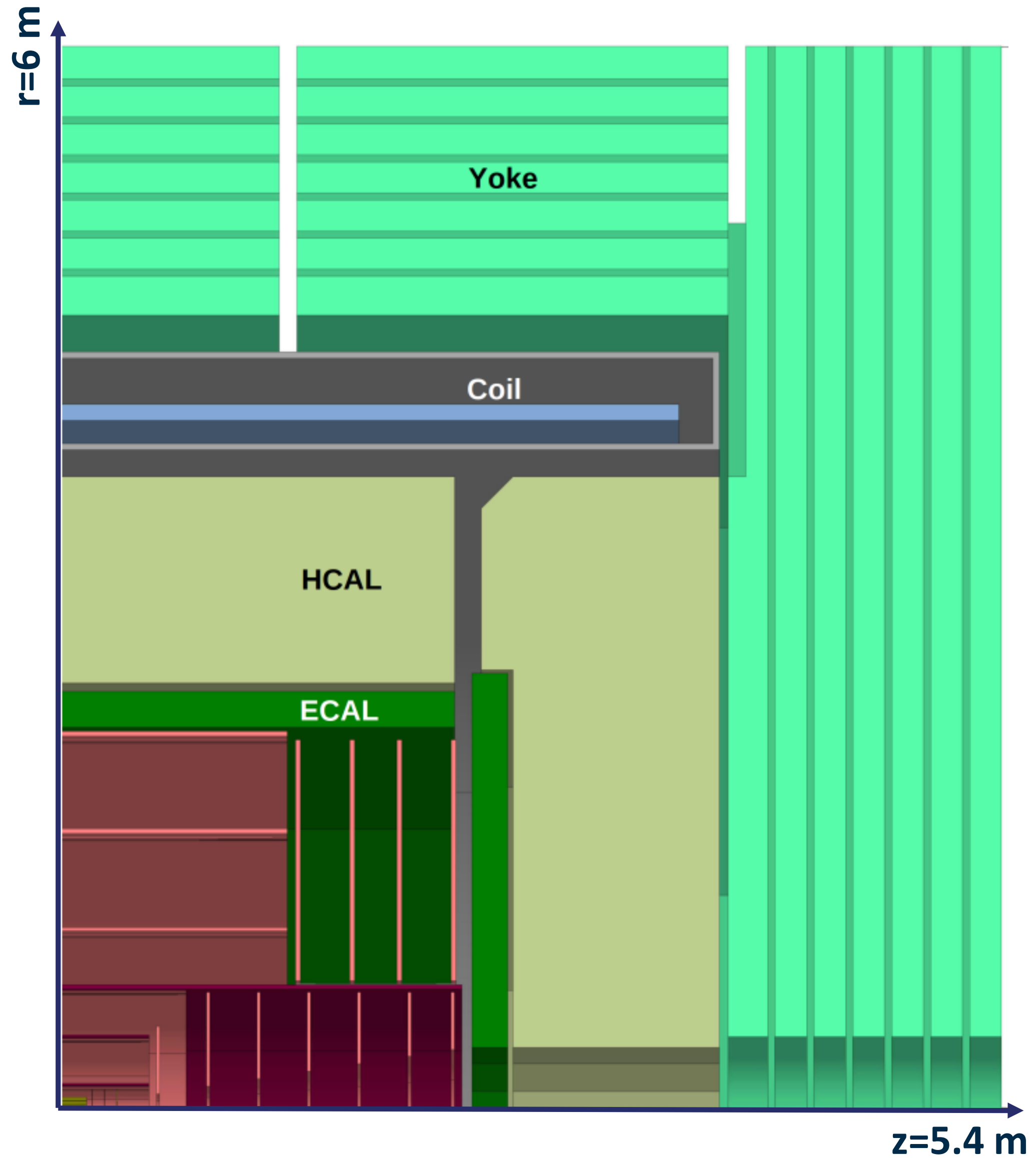
A collection of ideas from recent developments

FCC-ee Detectors: CLD

Ref. 1

Full Silicon Tracker

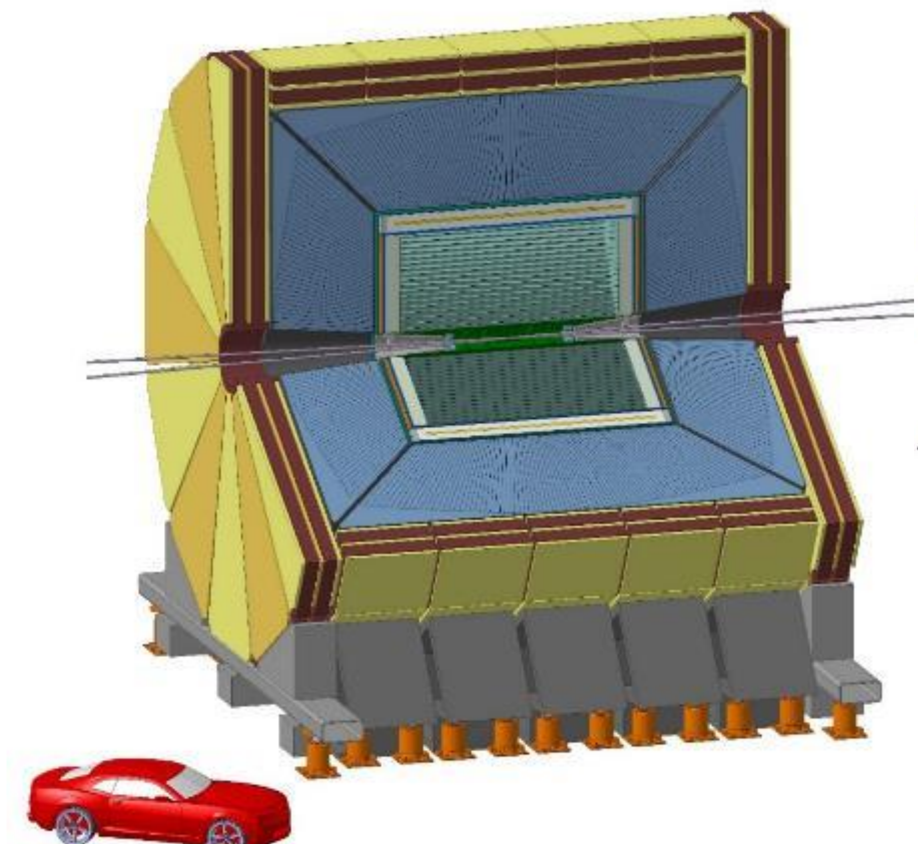
- Pixel vertex detector:
  - Barrel, 3 double layers, r=1.7, 2.7, 5.7 cm
  - Disks, 3 double layers, |z|=16, 23, 30 cm
  - 0.6-0.7% X_0 per double layer
- Inner tracker:
  - Strips and pixels
  - 12.7<R<57.5 cm, |z|<2.2 m
  - 1.1-1.5% X_0 per layer
- Outer tracker:
  - Strips
  - 67.5<R<210 cm, |z|<2.2 m
  - 1.1-1.5% X_0 per layer

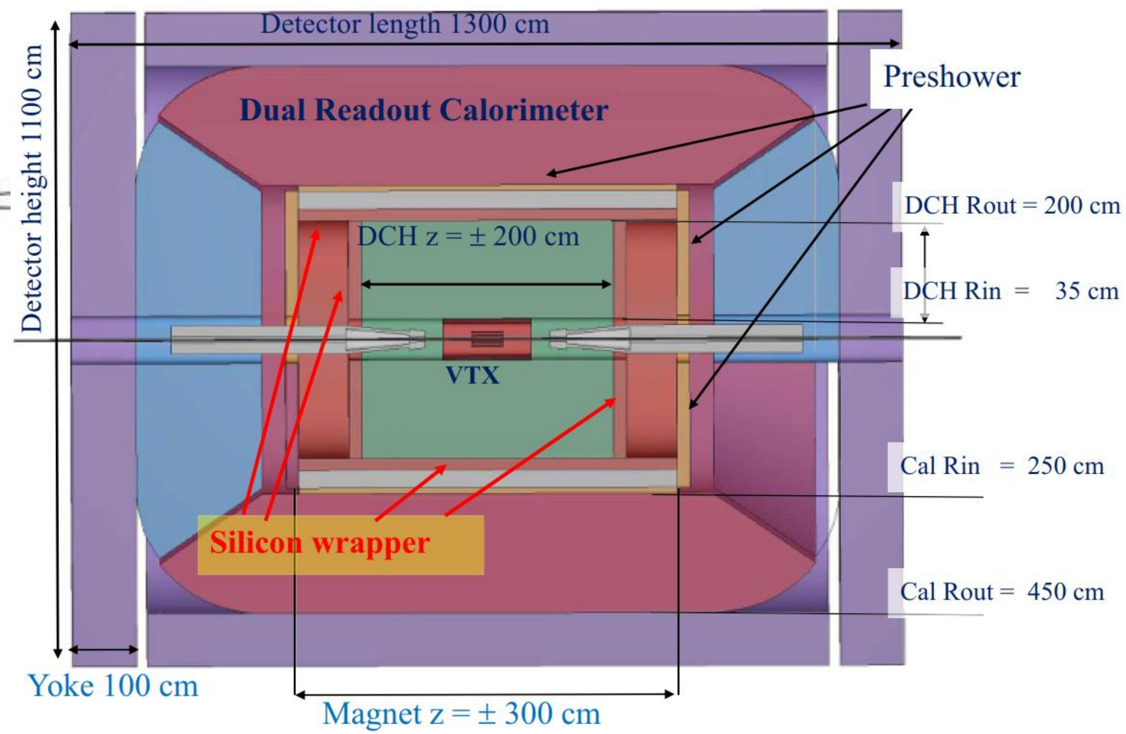


FCC-ee Detectors: IDEA

Ref. 2

- **Vertex detector: 5 (Depleted)MAPS layers r = 1.7 – 34 cm**
- Drift chamber (112 layers): 4 m long, r = 35 – 200 cm
- **Si wrapper: Strips, barrel at r=2 m and drift chamber endplates z=2 m**





Detector requirements

- Similar approaches for ILC, CLIC, CepC:
  - High resolution **pixel vertex detector** — O(few m^2)
  - Either **full silicon tracker** or **central gas chamber + Si wrapper** — O(100 m^2)

High precision measurement at end of tracking volume

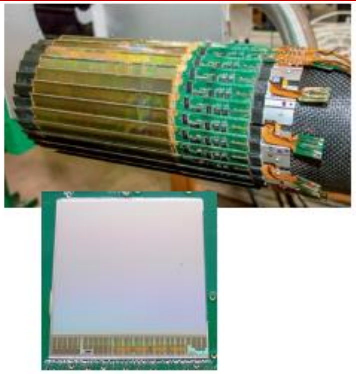
Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) = 2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} = 5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ 3 ~ 4% at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E = \frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

Challenging requirements on detector material

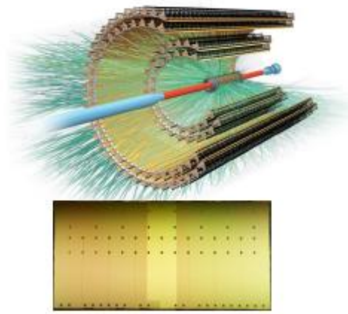
Finely segmented vertex detector

Vertex: Depleted MAPS

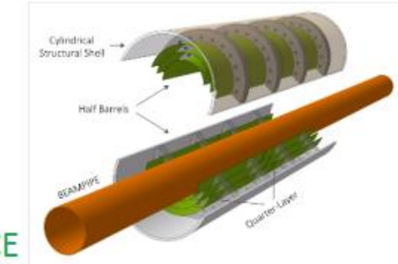
Ref. 3



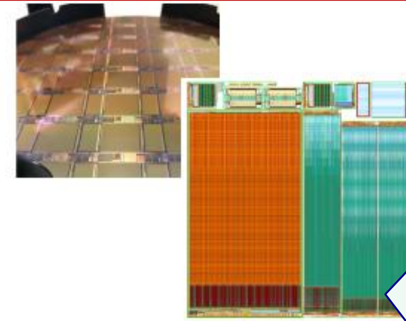
MIMOSA28 in STAR
First MAPS system in HEP



ALPIDE in ALICE
First MAPS in HEP with sparse readout similar to hybrid sensors
First MAPS in HEP to cover 10 m^2



ALICE
Stitching for low-mass cylindrical tracker



ATLAS MAPS development
Increased radiation toleranc
Serial power
...

But also
CLIC
Mu2e
ARCADIA
JADEPIX
...

After years of R&D monolithic sensors for HEP move to CMOS MAPS in mainstream technology

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc

Smaller feature size technologies allow lower analog and digital power consumption per channel and smaller pixels but power density is very important to contain voltage drops especially for large area devices.

Very fast charge collection in smaller pixels gives better timing resolution and also better radiation tolerance

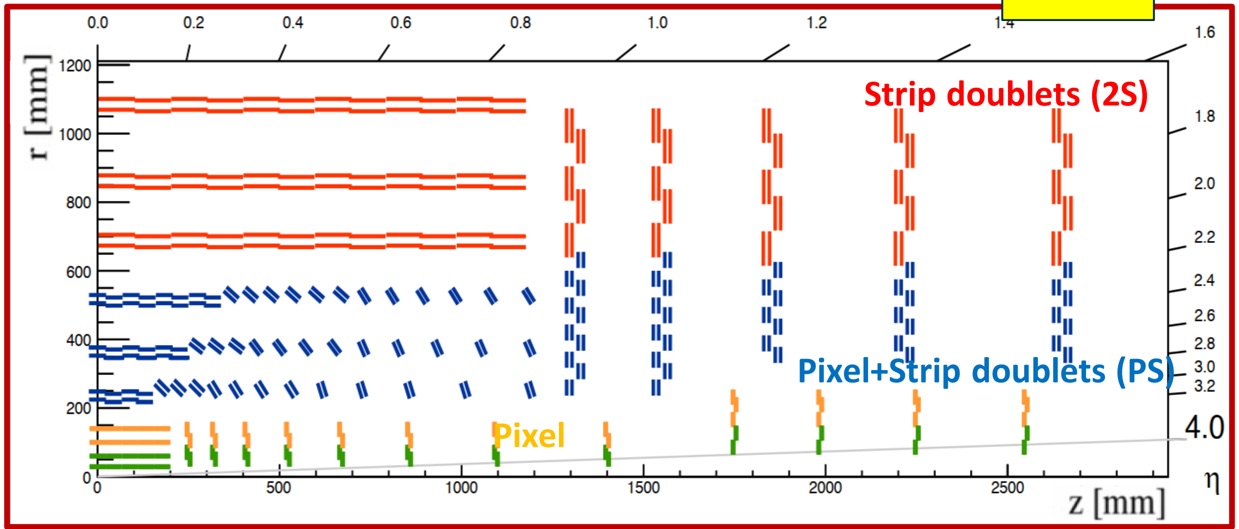
Depleted substrate

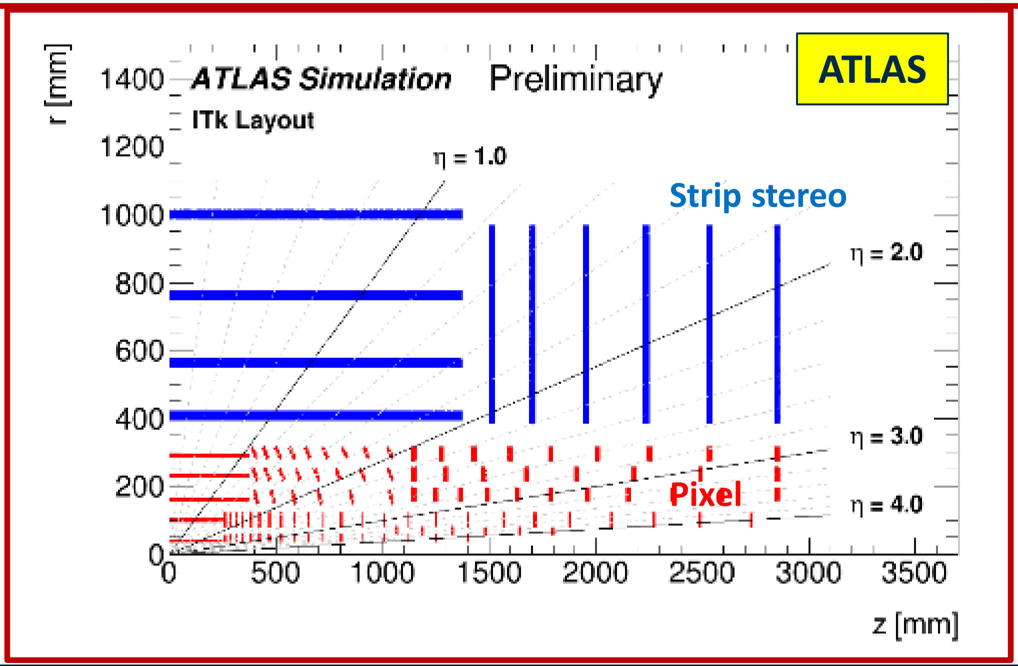
- Depleted MAPS are an attractive candidate for the vertex region:
  - Monolithic + low power = light structure
  - **I'll not try to summarize here the Tuesday afternoon session**

Tracker: Strips

Ref. 4-6

- Strips are the natural solution for the large area of the trackers:
  - Far from the interaction region: lower particle rate
  - Less channels: less power, less data connection
  - Simpler detector than pixels

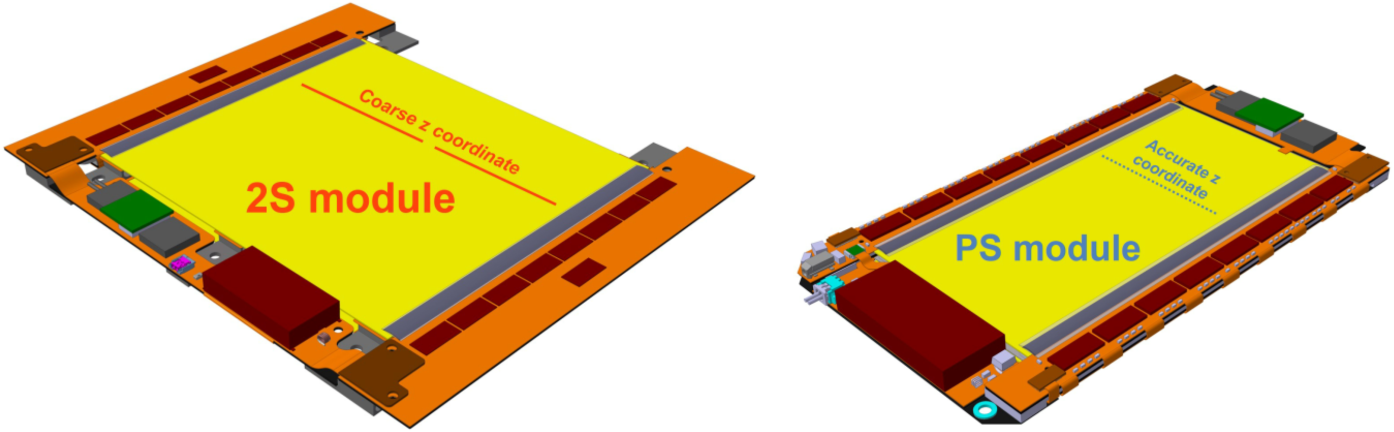




CMS Outer Tracker modules

Ref. 4-5

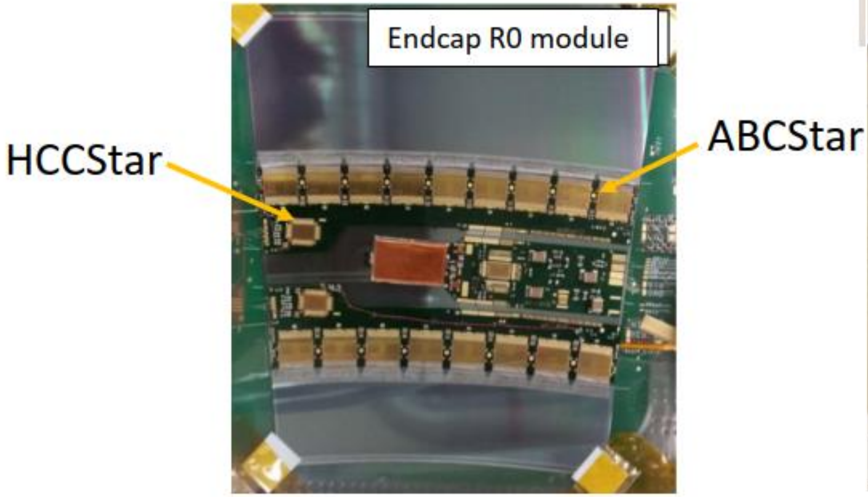
2S module	PS module
$\sim 2 \times 90$ cm^2 active area	$\sim 2 \times 45$ cm^2 active area
2×1016 strips: ~ 5 cm $\times$ 90 μm 2×1016 strips: ~ 5 cm $\times$ 90 μm	2×960 strips: ~ 2.4 cm $\times$ 100 μm 32×960 macro-pixels: ~ 1.5 mm $\times$ 100 μm
Front-end power ~ 5 W Sensor power ($-20\,^\circ$C) ~ 1.0 W	Front-end power ~ 8 W Sensor power ($-20\,^\circ$C) ~ 1.4 W

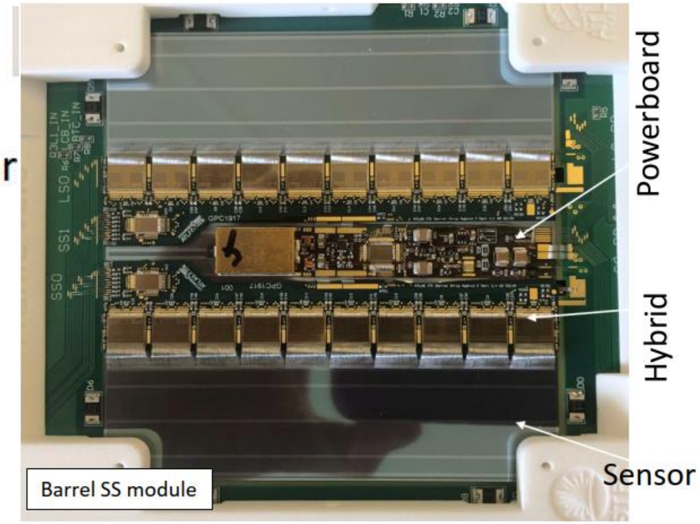


	2S	PS	Pixels
Area	192 m^2	25 m^2	4.9 m^2
Power density	27 mW/cm^2	89 mW/cm^2	700 mW/cm^2
Module cost (TDR)	26990 kCHF	20780 kCHF	11691 kCHF
	140 kCHF/m^2	830 kCHF/m^2	2400 kCHF/m^2

ATLAS Strip modules

Ref. 7-8





	Strip	Pixels
Area	165 m^2	13 m^2
Power density	43 mW/cm^2	700 mW/cm^2
Module cost (TDR)	36900 kCHF	25067 kCHF
	224 $kCHF/m^2$	1900 $kCHF/m^2$

Strips for FCC-ee

- Strip tracking parts are not that different from the current ATLAS and CMS upgrades:
  - CLD has a coverage of 195 m^2
  - IDEA is about 2x50 m^2
- Lesser radiation damage and particle rate will probably make things simpler for the services:
  - May operate at a higher temperature
  - Lower power dissipation
  - Data concentration on fewer data links

IS THERE ANYTHING NEW?

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Option 1: Passive CMOS

- Implement passive structures in standard CMOS processes on high resistivity substrate
  - Alternative fabrication process for standard strip and pixel sensors: **“fast and cheap”**
  - **Stitching** to build large area sensors: **should receive soon a run in LFoundry 150 nm**

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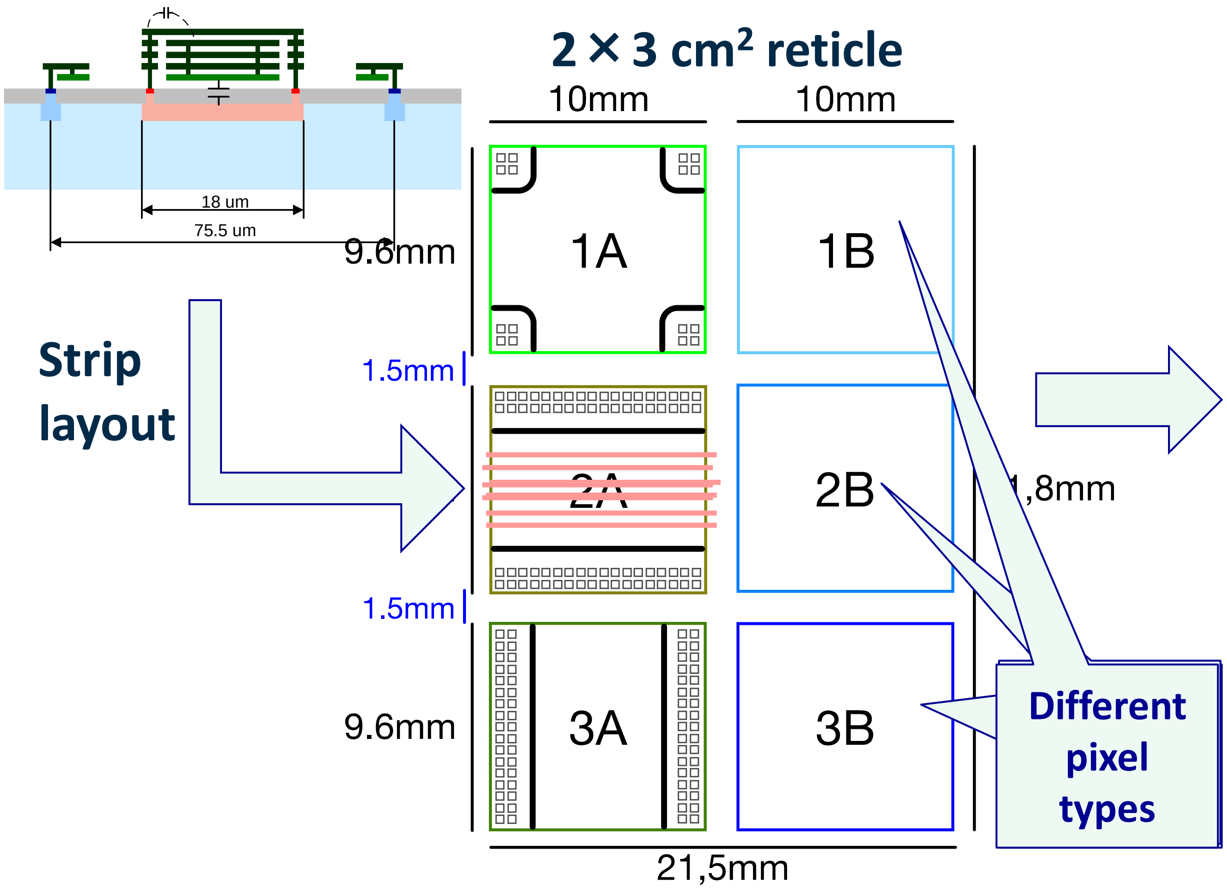
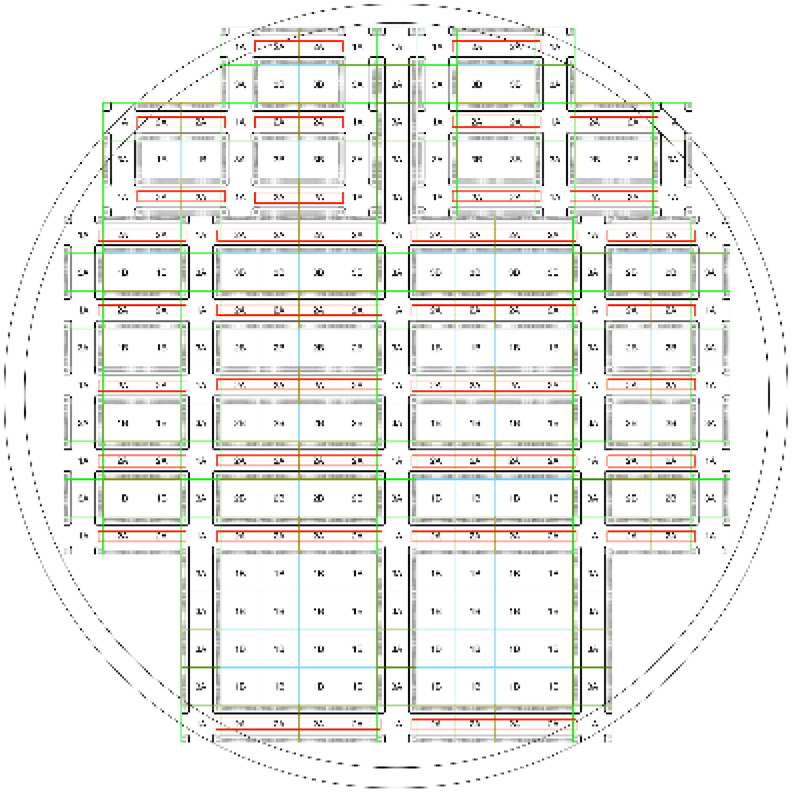




Option 1: Passive CMOS

- Approach initially developed for pixel detectors, but actually interesting for strips where there is a lack of producers for very large detector surfaces.
  - ATLAS estimated of 400-500 kCHF/m^2 for a full CMOS run (including yield and spares)
  - Can be reduced since not all available layers at a foundry are needed: partial mask set
  - Potential to build “monolithic” strips by integrating readout electronics in the lattice
  - Possibility of large detector tiles

- **Cons:** very large startup costs: stitching+HR substrate usually requires to book full engineering runs)

Option 2: Full DMAPS Detector

Ref. 9-10

- DMAPS used in the vertex, can operate also in the outer part of the tracker.
- **Performance-wise** is an improvement:
  - Unambiguous, precise measurement in both coordinate instead of asymmetric precision of stereo strips
  - One thin silicon layer instead of strip doublets
- More **practical** points:
  - **Homogeneous detector**
  - **Production size well within the capability of CMOS foundries**
  - The target power density of next generation DMAPS detector is comparable with HL-LHC strips
  - Cost is not so different, if one considers half silicon area is needed
  - **Stitching and/or multi-chip modules** are required to avoid excessive fragmentation (10x ALICE ITS)

One example: ATLASPIX3

Ref. 10

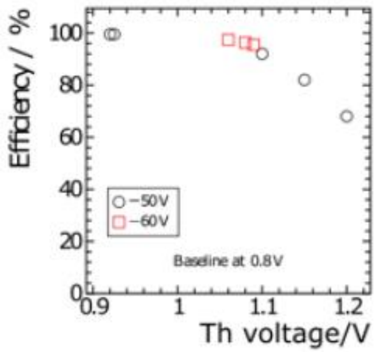
Sensor proposal: ATLASPix

Physics | Lancaster University

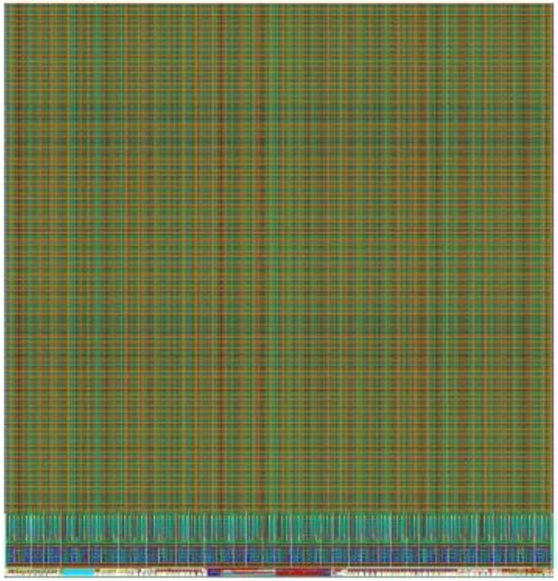
ATLASPix is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 μm by 50 μm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

I. Peric et. al., NIM A924 (2019) 99-103



ATLASPix3



ATLASPix3

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200Ωcm, 180nm) **just delivered**
- 132 columns with 150µm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two **end of column (EoC) blocks**. EoC1 is attached to hit buffers and EoC2 to trigger buffers.

Similar detectors from LFoundry and TowerJazz will become available shortly

One example: ATLASPIX3

Ref. 10

Physics | Lancaster University

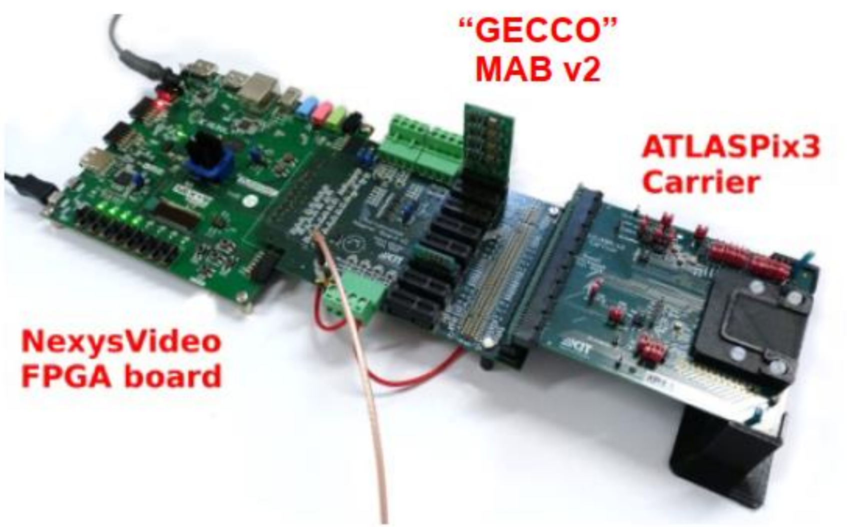
Module Flex

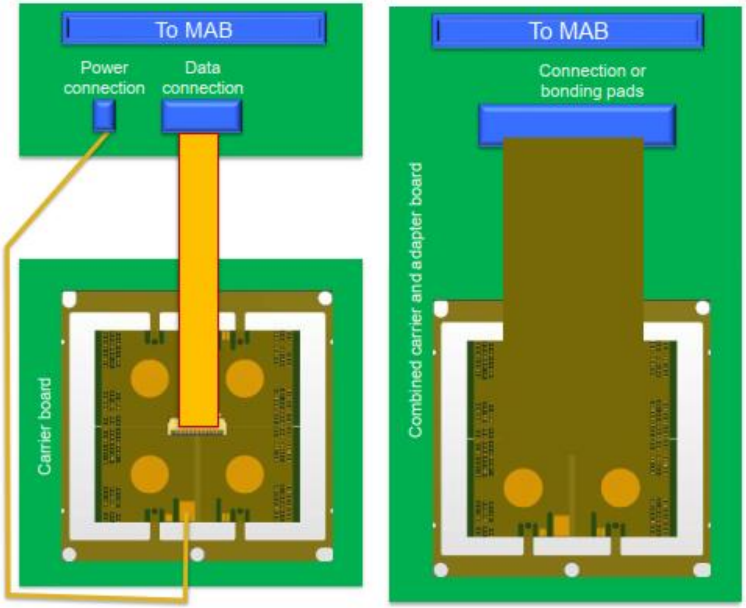
Università and INFN di Milano: Attilio Andreazza, Mauro Citterio, Fabrizio Sabatini

Purpose is to build a **pseudo-quad module** for ATLAS
Test system functionality for large size detectors

Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests

Two basic ideas:
- Connector
- Integrated Pigtail

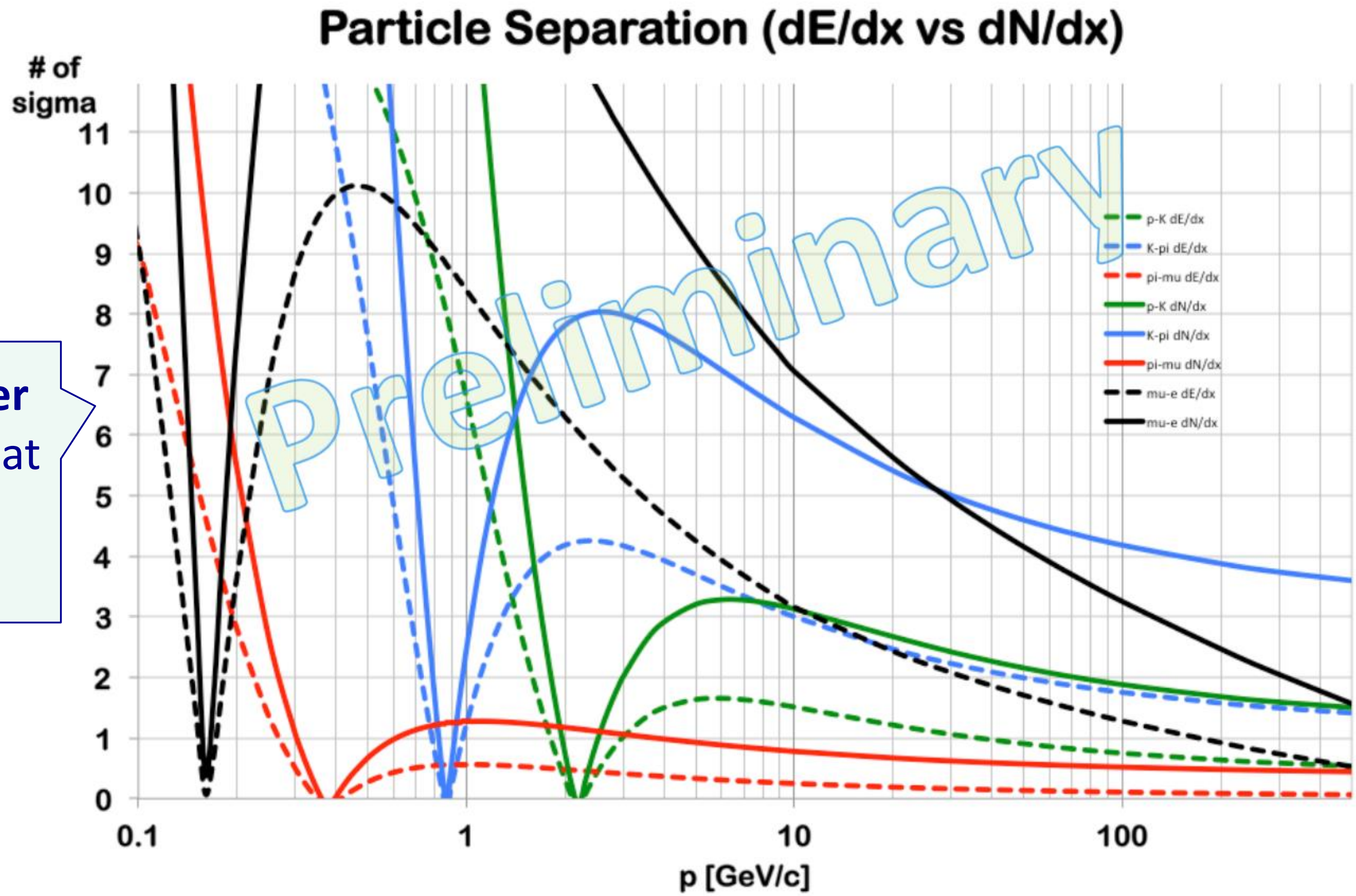




Option 3: Particle Identification

Ref. 2

- Hadron identification is a feature of last generation e^+e^- experiments
- Central tracking with gas detectors can provide good dE/dx

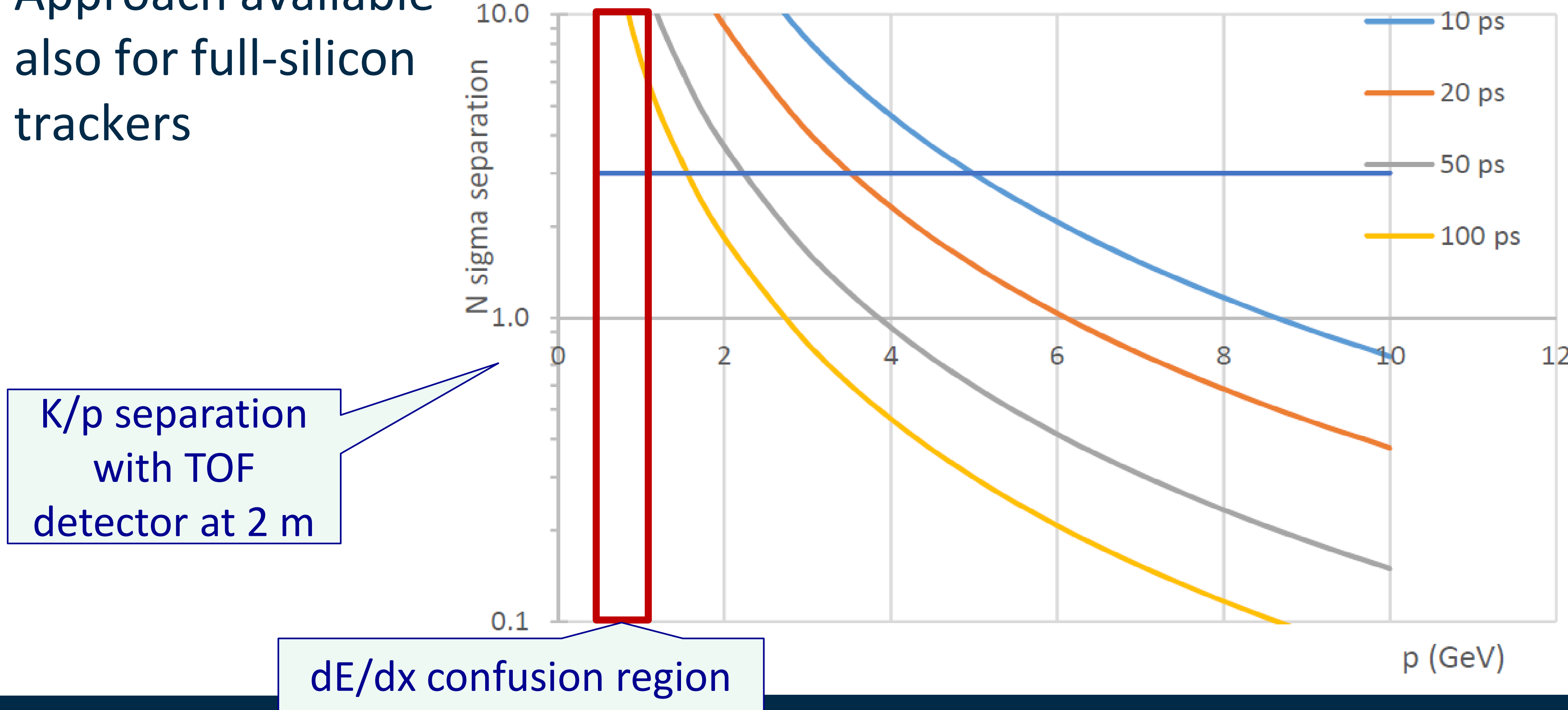


IDEA Drift Chamber
Hadron separation at Nσ by cluster counting method

Option 3: Particle Identification

Ref. 2

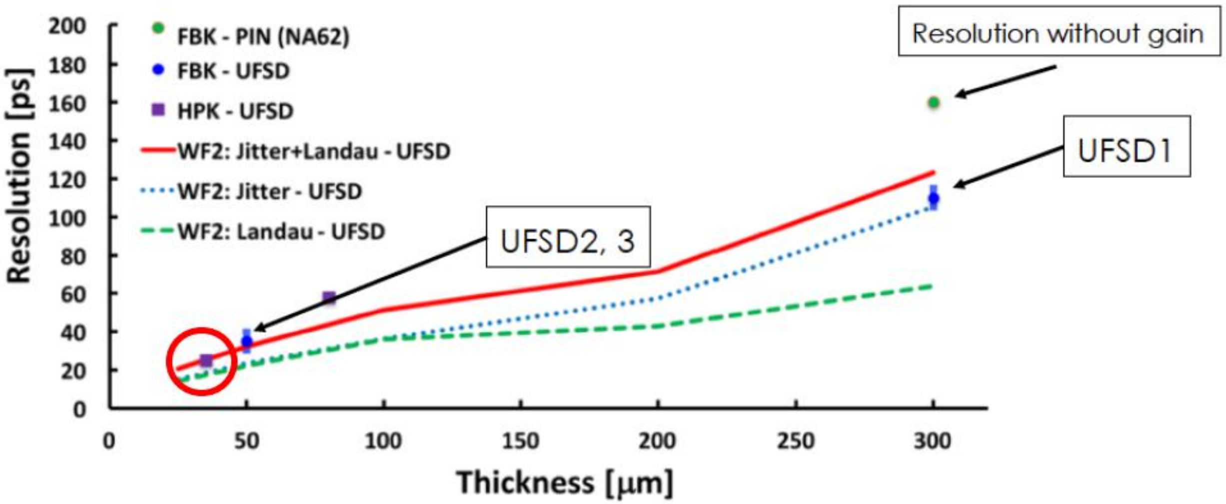
- Hadron identification is a feature of last generation e^+e^- experiments
- Central tracking with gas detectors can provide good dE/dx
- Can be complemented with timing measurements (TOF)
- Approach available also for full-silicon trackers

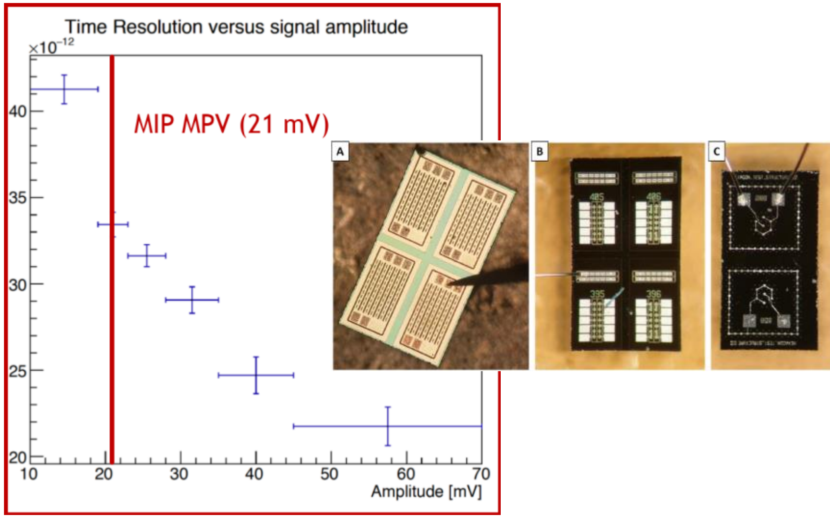


Silicon timing detectors

Ref. 11 15

- Recent developments have shown the silicon detector can achieve the required timing resolution.
- The key ingredient is signal multiplication (LGAD, 3D)





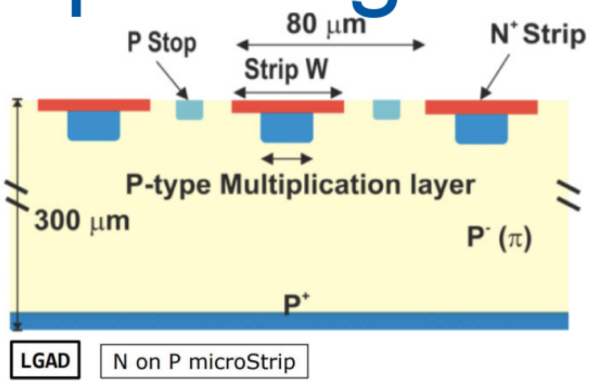
- For application to the outermost tracking layers of FCC-ee:
  - Higher spacial resolution (~10 μm pitch, compared to ~1 mm of HL-LHC timing layers)
  - 100% fill factor
  - Production process scalable to large volumes

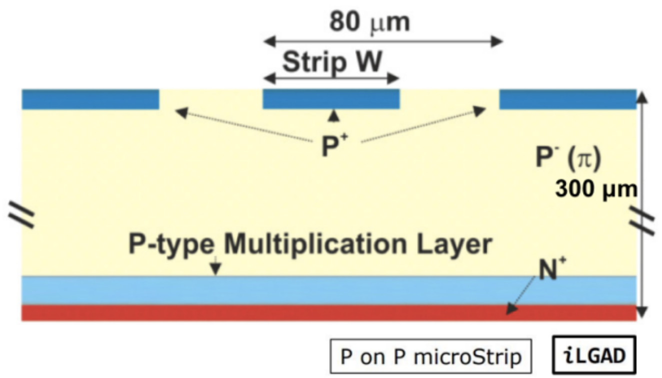
Silicon timing detectors

Ref. 12-13

- A promising approach is to separate multiplication and charge collection functions:
  - Uniform multiplication layer
  - Segmented collection/induction electrodes

Improving the fill factor: iLGAD





E. Currás et al., arXiv:1904.02061

Segmented multiplication layer:

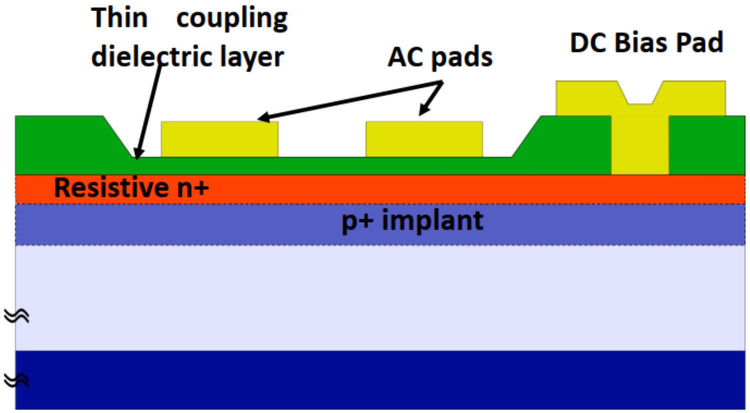
- Spatially inhomogeneous gain
- Degraded resolution for inter-strip hits
- Fill-factor problem

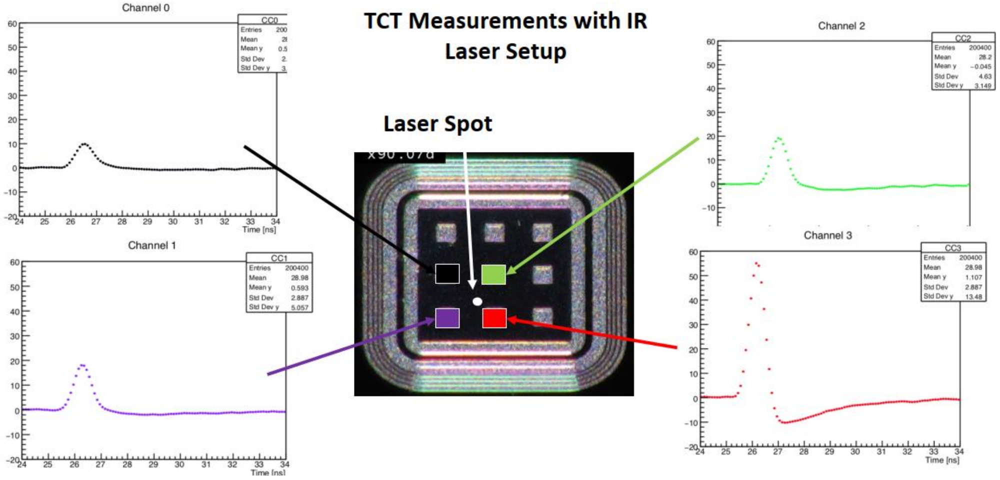
Non-segmented multiplication layer:

- Uniform gain distribution
- Promising timing results: ~20 ps
  - Unirradiated 285-μm iLGAD, laser-induced signal at 20°C
  - Thinner sensors under development

Silicon timing detectors

- A promising approach is to separate multiplication and charge collection functions:
  - Uniform multiplication layer
  - Segmented collection/induction electrodes





Resistive AC-coupled Silicon Detector

- Non-segmented p^+ multiplication layer
- Resistive n-layer
- AC-coupled readout pads with thin dielectric layer
- AC pads define the readout pitch
- Position from interpolation of signal on nearby electrodes
  - Feasible if occupancy is low
  - Observed space resolution of few micrometers

Conclusion and outlook

- Most detector designs for future e+e- colliders foresee large area silicon tracking systems.
- From a principle point of view, they don't look more challenging than the current HL-LHC upgrades.
- Nevertheless some of the current R&D may open new perspectives also in these systems.
- Some personally selected ideas presented here:
  - Applications of CMOS processes
  - Timing layers for hadron identification
- It will help to get people committed to a critical component of FCC-ee detectors.

Hope that was interesting enough and thanks for listening!

References

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   S. Wonsak, The ATLAS ITk Strip Detector System for the Phase-II LHC Upgrade, Vertex 2019
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12. S. Otero-Ugobono, LGAD and 3D as timing detectors, Vertex 2019
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14. G. Paternoster et al., Novel Strategies for Fine-Segmented LGADs, Hiroshima2019
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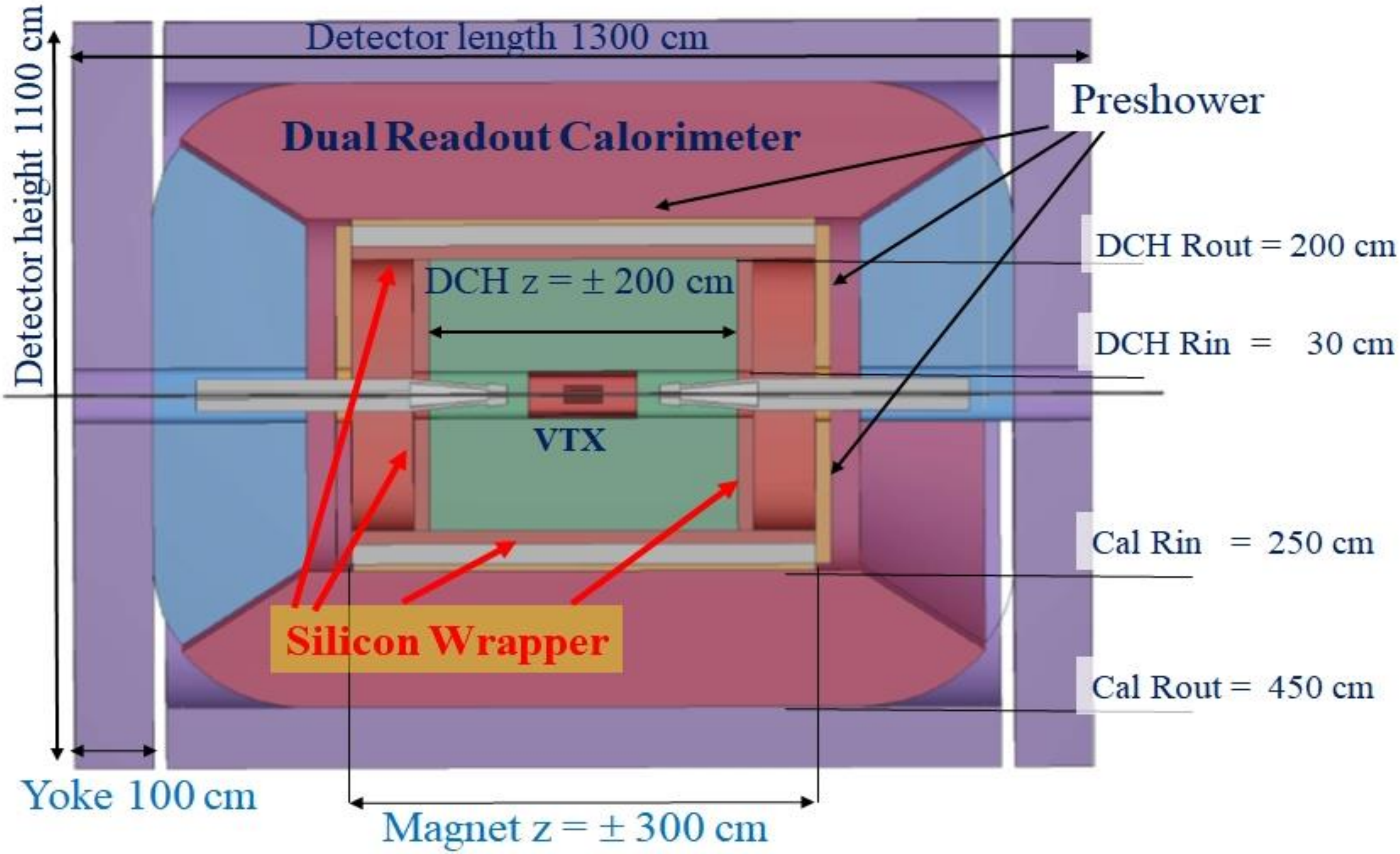
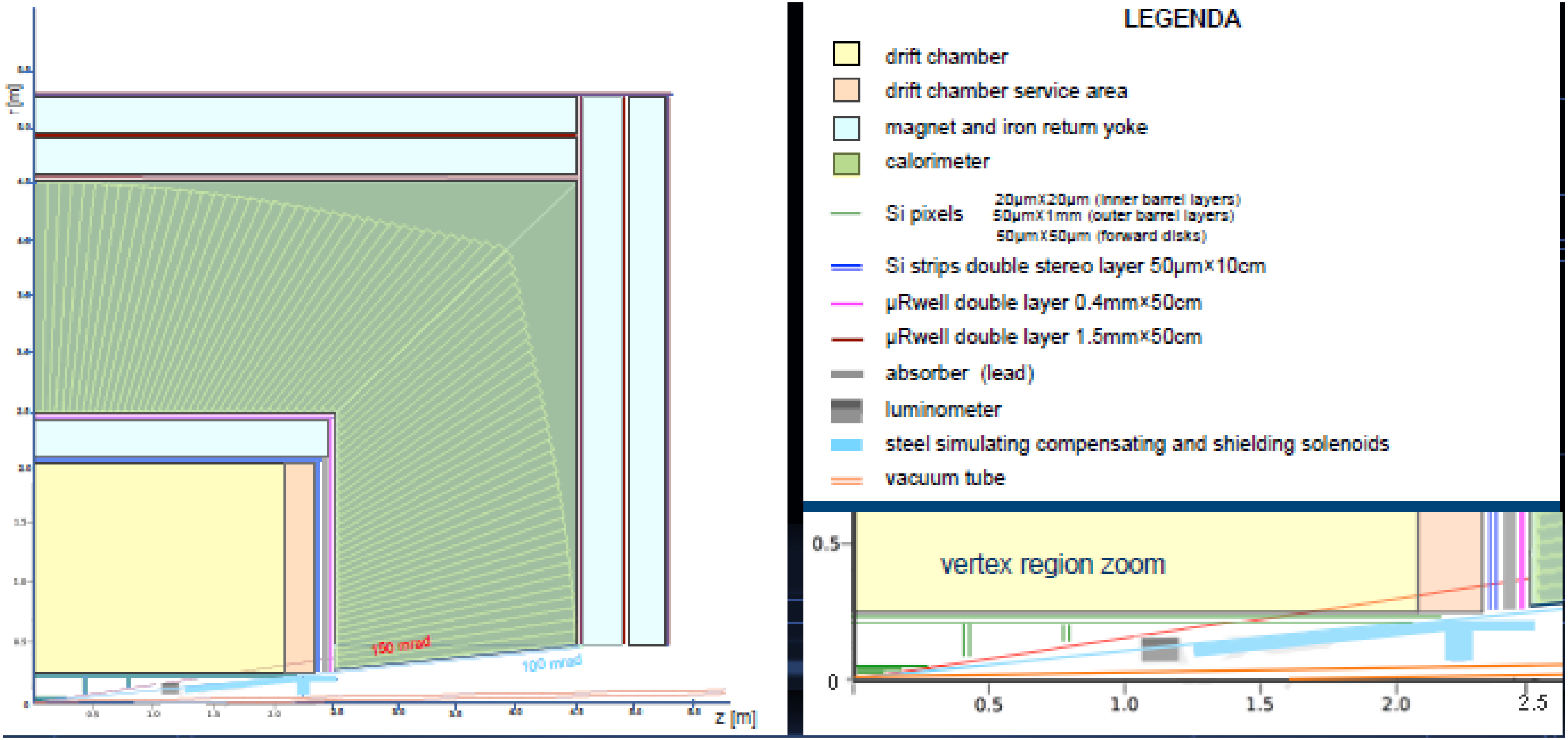
BACKUP

IDEA Layout


Detector length 1300 cm
Detector height 1100 cm
Preshower
Dual Readout Calorimeter
DCH Rout = 200 cm
DCH z = ± 200 cm
DCH Rin = 30 cm
VTX
Cal Rin = 250 cm
Silicon Wrapper
Cal Rout = 450 cm
Yoke 100 cm
Magnet z = ± 300 cm

IDEA Layout


r [m]
150 mrad
100 mrad
z [m]
LEGENDA
drift chamber
drift chamber service area
magnet and iron return yoke
calorimeter
Si pixels
20µmX20µm (inner barrel layers)
50µmX1mm (outer barrel layers)
50µmX50µm (forward disks)
Si strips double stereo layer 50µm×10cm
µRwell double layer 0.4mm×50cm
µRwell double layer 1.5mm×50cm
absorber (lead)
luminometer
steel simulating compensating and shielding solenoids
vacuum tube
vertex region zoom
0.5
0
0.5
1.0
1.5
2.0
2.5