

# Recent results and plans of the 3D IC consortium



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on behalf of the 3D consortium



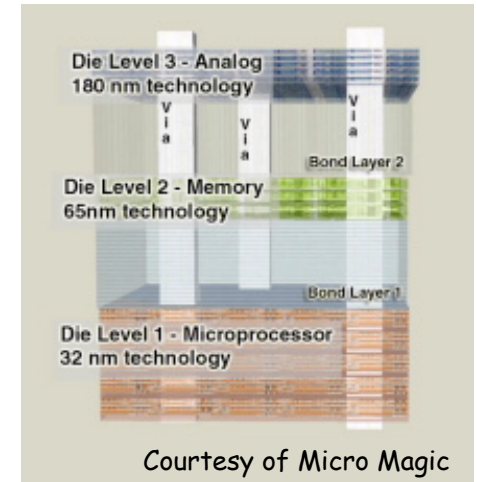
19<sup>th</sup> International Workshop on Vertex Detectors, 6-11 June, 2010, Loch Lomond, Scotland

# Motivations

- ✓ The experiments at the future high luminosity colliders and B-factories need fast, highly granular (=> **small pixel pitch**), low material budget (=> **low mass cooling, thin** silicon wafers) particle trackers
- ✓ Significant progress has been made in the last decade to address these issues by integrating sensors and front-end electronics within the pixel cell
  - ✓ **Monolithic Active Pixel Sensors** (MAPS) are a promising solution for low-mass, high granularity pixel trackers. After several years of R&D, MAPS are reaching a good maturity level, but there is still room for substantial improvements
  - ✓ **SOI Pixel Sensors**
  - ✓ **3D circuits**: offers improved performance over other approaches for HEP

# 3D Integrated Circuits

- ✓ The move to 3D is being driven entirely by industry needs (reduce R, L, C for higher speed, provide increased functionality, reduce cross-talk, ...)
- ✓ A 3D chip (different from a 3D detector) is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded and interconnected to form a monolithic circuit
- ✓ Processing of each layer can be optimized
- ✓ MAPS can **benefit from technological advances**
  - ✓ 100% fill factor
  - ✓ PMOS transistors in pixel
  - ✓ Increase functional density without going to smaller feature size
  - ✓ ...

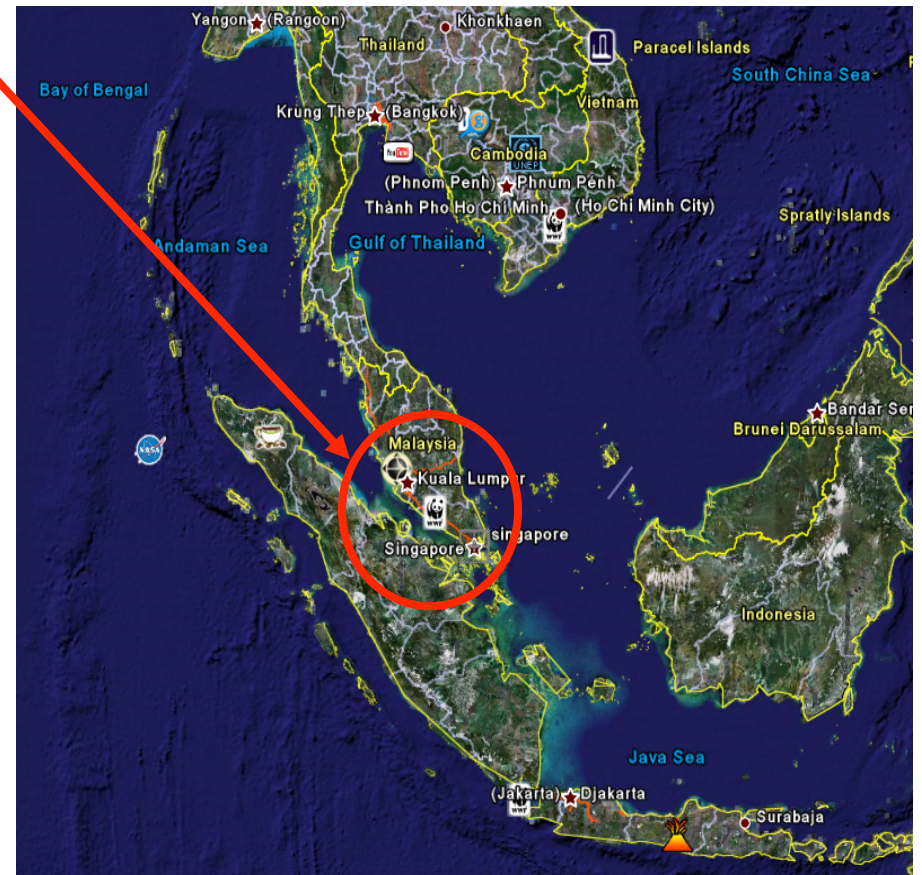


## 3D IC Consortium

- ✓ In late 2008 a large number of international laboratories and universities with interest in High Energy Physics formed a consortium for the development of 3D integrated circuits (web page: <http://3dic.fnal.gov>)
- ✓ The Consortium has made a considerable effort to meet the deadline of end of May '09 for a multiproject run in the Tezzaron/Chartered 130 nm technology
- ✓ Multi-Project Wafer runs allow to share the price by sharing the reticule area (prototype fabrication, low volume productions: some hundreds to hundred thousands parts)
- ✓ Consortium **presently** comprised of 17 members from 7 countries
  - ✓ Fermilab, Batavia
  - ✓ University at Bergamo
  - ✓ University at Pavia
  - ✓ University at Perugia
  - ✓ INFN Bologna
  - ✓ INFN at Pisa
  - ✓ INFN at Rome
  - ✓ CPPM, Marseilles
  - ✓ IPHC, Strasbourg
  - ✓ IRFU Saclay
  - ✓ LAL, Orsay
  - ✓ LPNHE, Paris
  - ✓ CMP, Grenoble
  - ✓ University of Sherbrooke
  - ✓ University of Bonn
  - ✓ AGH University of Science & Technology, Poland
  - ✓ Universitat de Barcelona
- ✓ Benefits:
  - ✓ Sharing of designs
  - ✓ Development of special software programs
  - ✓ Development of libraries and test structures
  - ✓ Design review
  - ✓ Sharing of results
  - ✓ Frequent meetings
  - ✓ Cost reduction

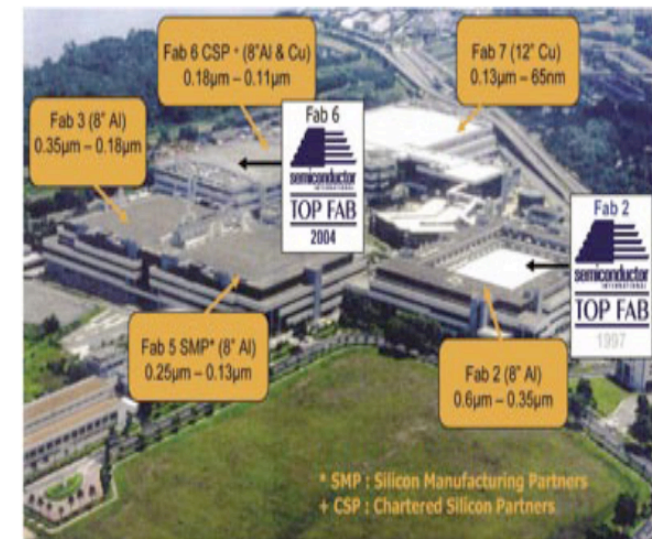
# Tezzaron Semiconductor

- ✓ Founded in 2000, located in Naperville, Illinois
- ✓ Has fabricated a number of 3D chips for commercial customers
- ✓ Tezzaron uses the "Via Middle" process
- ✓ Wafers with "vias middle" are made by Chartered Semiconductor in Singapore
- ✓ Wafers are bonded in Singapore by Tezzaron
  - ✓ Facility can handle up to 1000 wafers/month
- ✓ Bonded wafers are finished by Tezzaron
  - ✓ Bond pads
  - ✓ Bump bond pads
- ✓ Potential Advantages
  - ✓ Lower cost
  - ✓ Faster turn around
  - ✓ One stop shopping!
- ✓ Process is available to customers from all countries



# Chartered Semiconductor

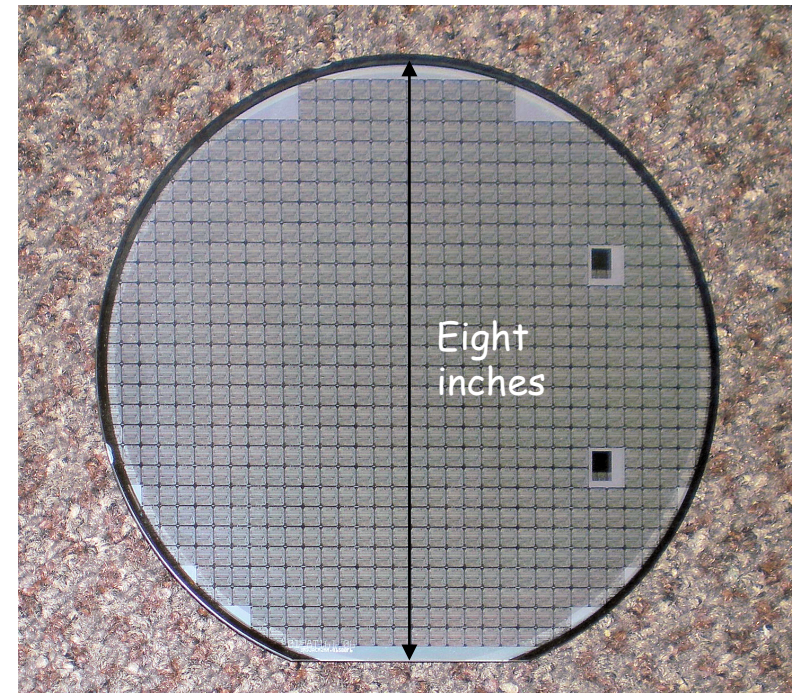
- ✓ Chartered Semiconductor (now subsidiary company of GlobalFoundries) is one of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5  $\mu\text{m}$  down to 45 nm
- ✓ Offers Common Chartered-IBM platform for processes at 90 nm and below
- ✓ Chartered 0.13  $\mu\text{m}$  mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - ✓ Chartered has made nearly 1,000,000 eight inch wafers in the 0.13 $\mu\text{m}$  process
- ✓ Extension to 300mm wafers and 45nm TSVs underway
- ✓ Chartered 0.13  $\mu\text{m}$  process has different layer arrangement and transistor thresholds than IBM process
- ✓ Commercial tool support for Chartered Semiconductor
  - ✓ DRC - Calibre, Hercules, Diva, Assura
  - ✓ LVS - Calibre, Hercules, Diva, Assura
  - ✓ Simulation - HSPICE, Spectre, ELDO, ADS
  - ✓ Libraries - Synopsys, ARM, Virage Logic



Chartered Campus

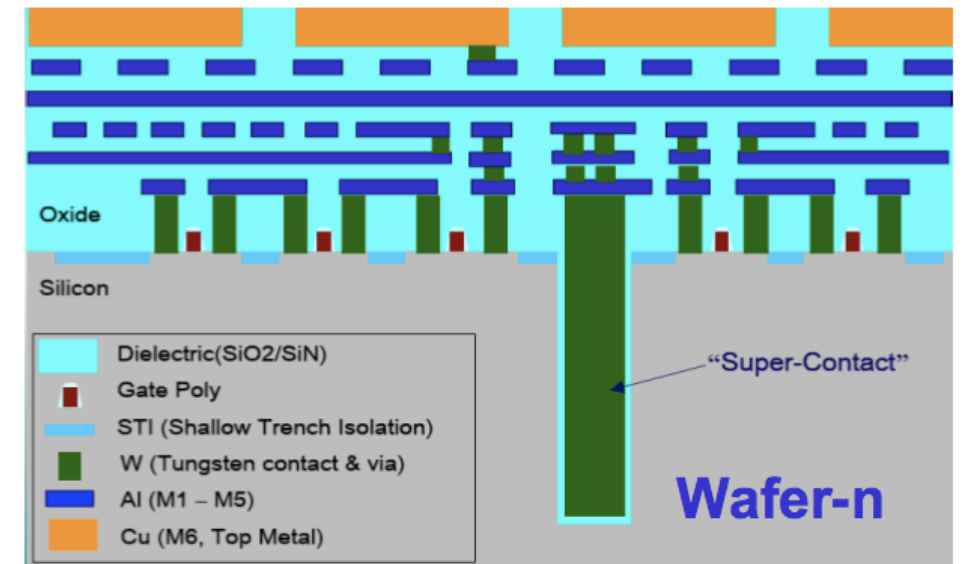
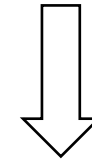
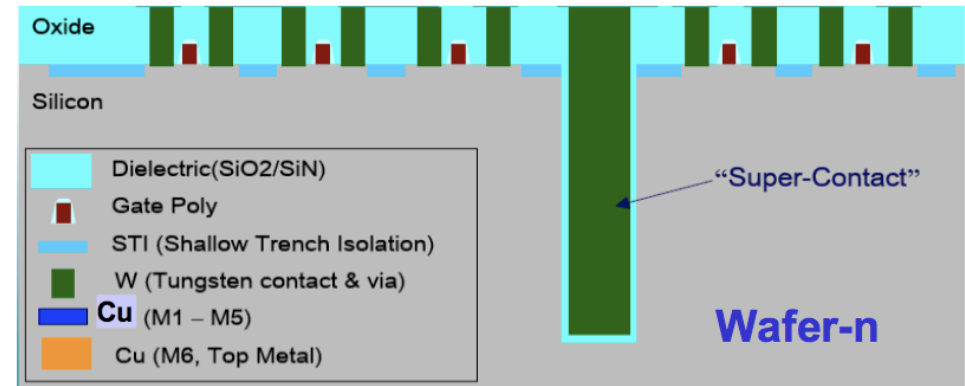
# Chartered 0.13um Process

- ✓ 8 inch wafers
- ✓ Large reticule ~ 26 mm x 31 mm
- ✓ Options chosen
  - ✓ Deep N-well
  - ✓ MiM capacitors - 1 fF/um<sup>2</sup> (single mask)
  - ✓ Single poly
  - ✓ 6 levels of metal (8 available) + RDL
  - ✓ Low power option chosen
    - ✓ Standard V<sub>t</sub>
    - ✓ Low V<sub>t</sub>
    - ✓ Zero V<sub>t</sub> (native NMOS)
  - ✓ I/O transistors - 3.3 V
  - ✓ High resistance poly resistors
  - ✓ Embedded through silicon vias (via first processing)



# Tezzaron vertical integration process

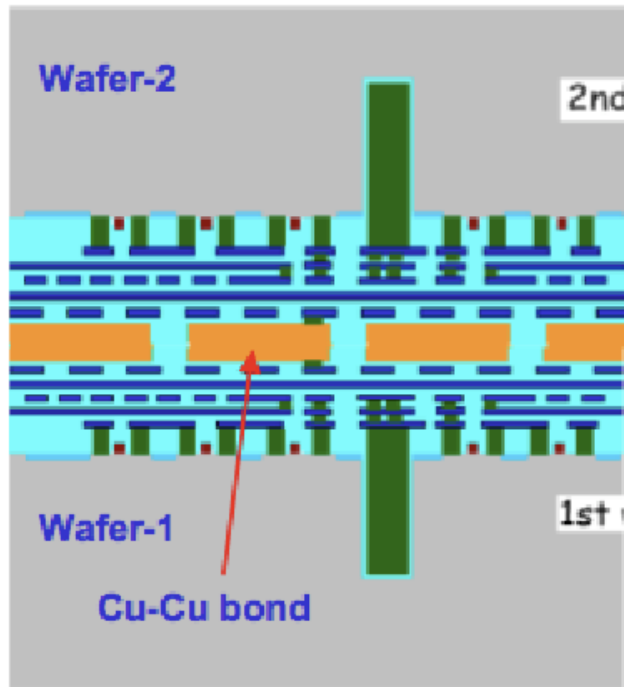
- ✓ Tezzaron uses a "via middle" approach for the fabrication of 3D chip
- ✓ Step 1: On all wafer to be stacked complete transistor fabrication, form TSV, passivation and fill TSV at same time connections are made to transistors
- ✓ Step 2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7um).





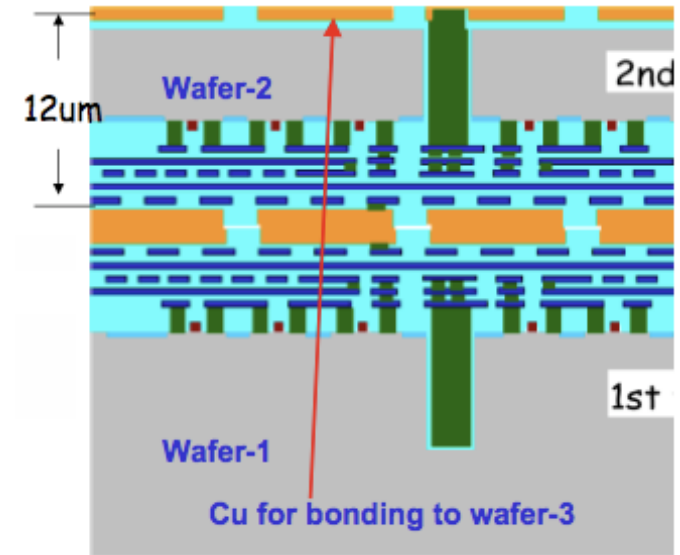
# Tezzaron vertical integration process

Step 3: bond wafer 2 to wafer 1  
(Cu-Cu thermo-compression bond)

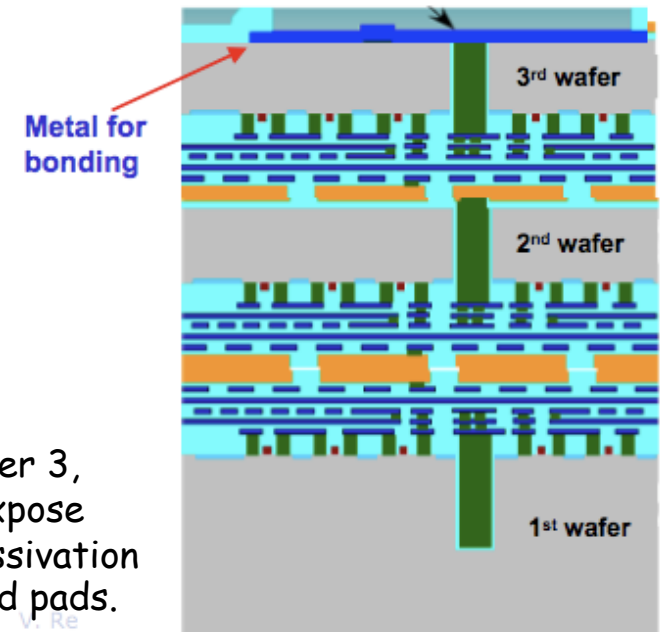


Step 4: thin the wafer 2 to about 12µm to expose TSV.

Add Cu to back of wafer 2 to bond wafer 2 to wafer 3  
OR add metallization on back of wafer 2 for bump bonding or wire bonding

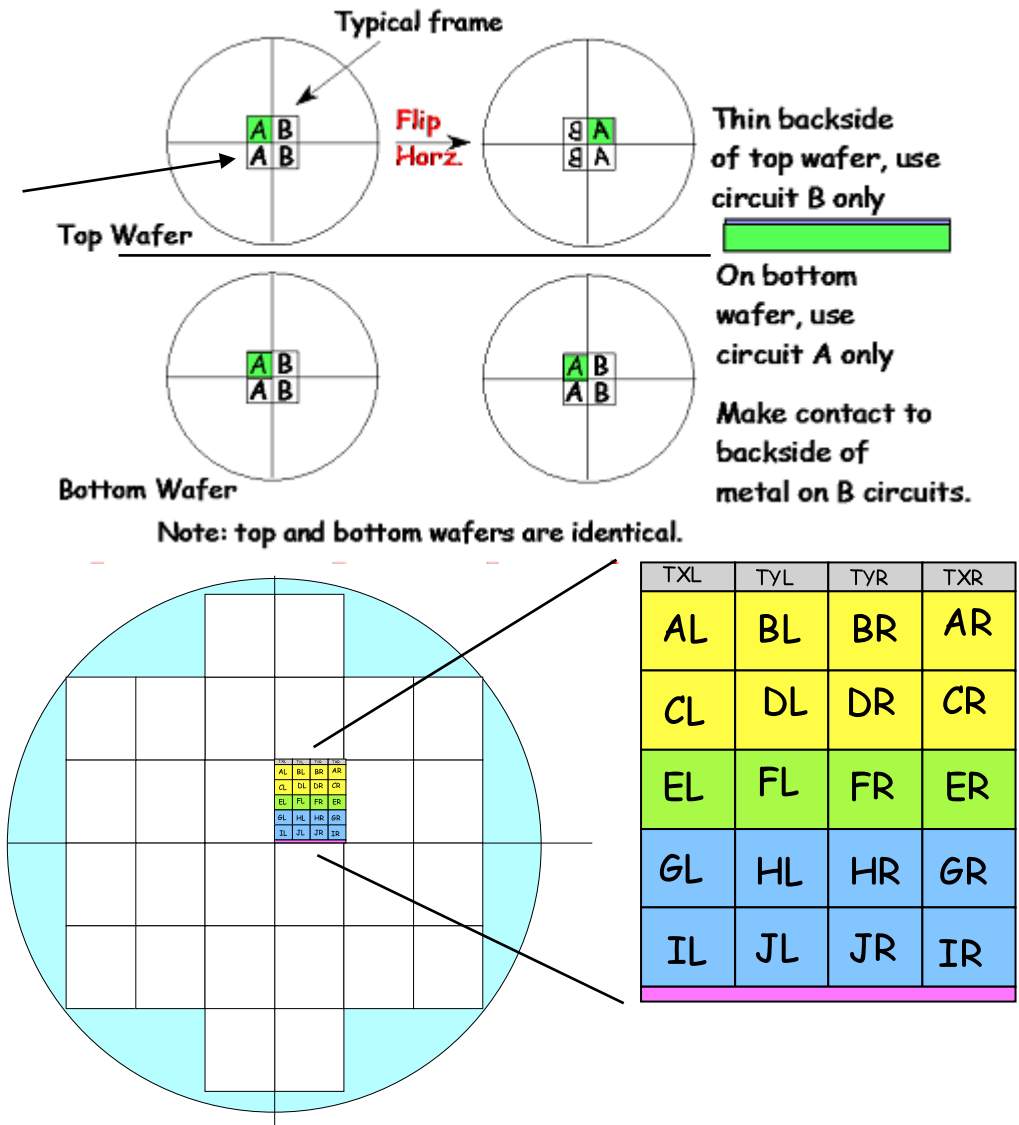


Step 5: stack wafer 3, thin wafer 3 to expose TSV, add final passivation and metal for bond pads.

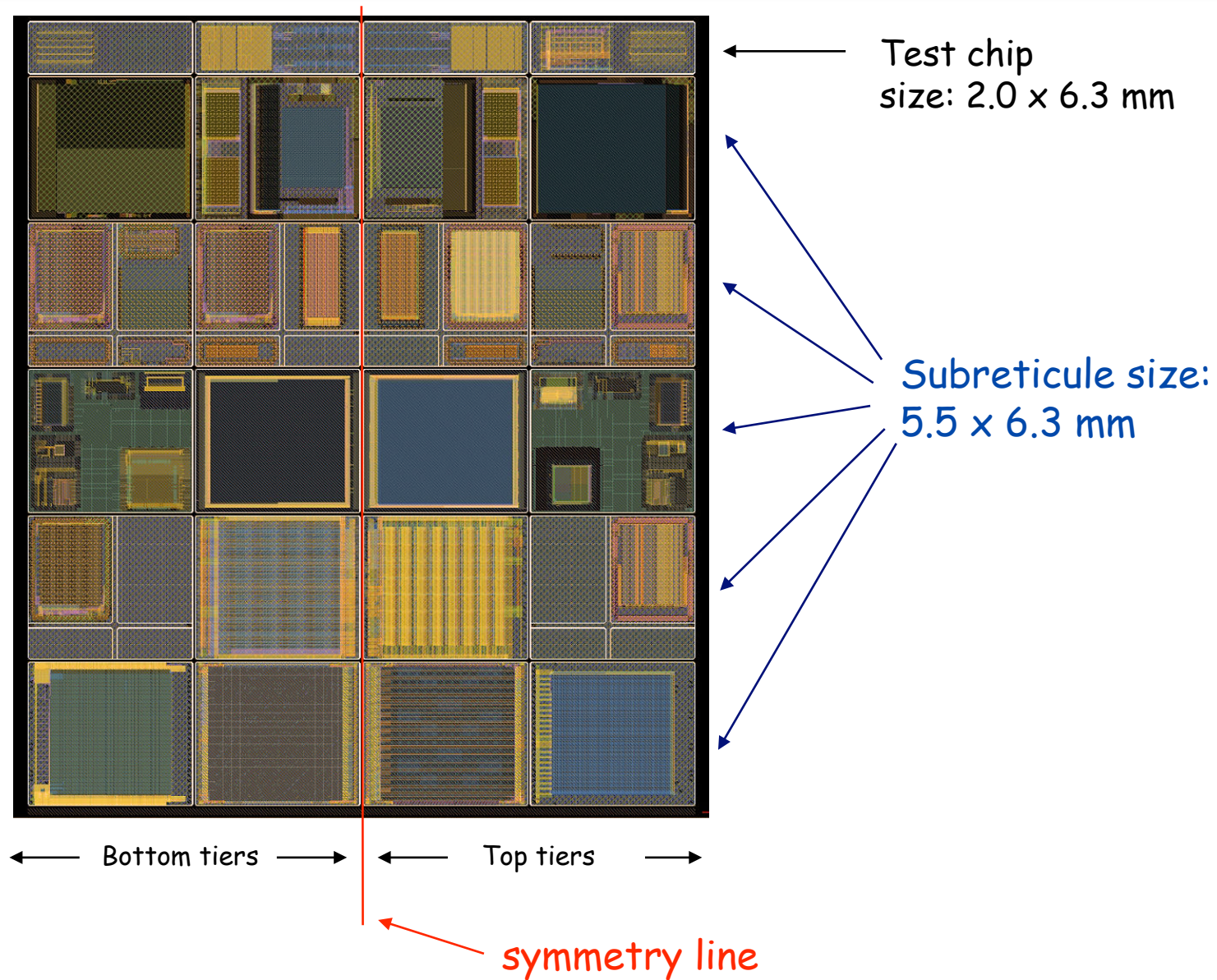


# Frame for the First MPW Run

- ✓ 3D chip has two tiers
- ✓ One set of masks used for both top and bottom tiers to reduce mask cost
  - ✓ Identical wafers bonded face to face by Tezzaron
  - ✓ Backside metallization by Tezzaron.
- ✓ Frame divided into 12 subreticules among consortium members
- ✓ More than 25 two-tier designs (circuits and test devices)
  - ✓ CMS strips, ATLAS pixels
  - ✓ ILC pixels
  - ✓ B factory pixels
  - ✓ X-ray imaging
  - ✓ Test circuits
    - ✓ Radiation
    - ✓ Cryogenic operation
    - ✓ Via and bonding reliability
    - ✓ SEU tolerance



# MPW Full Frame

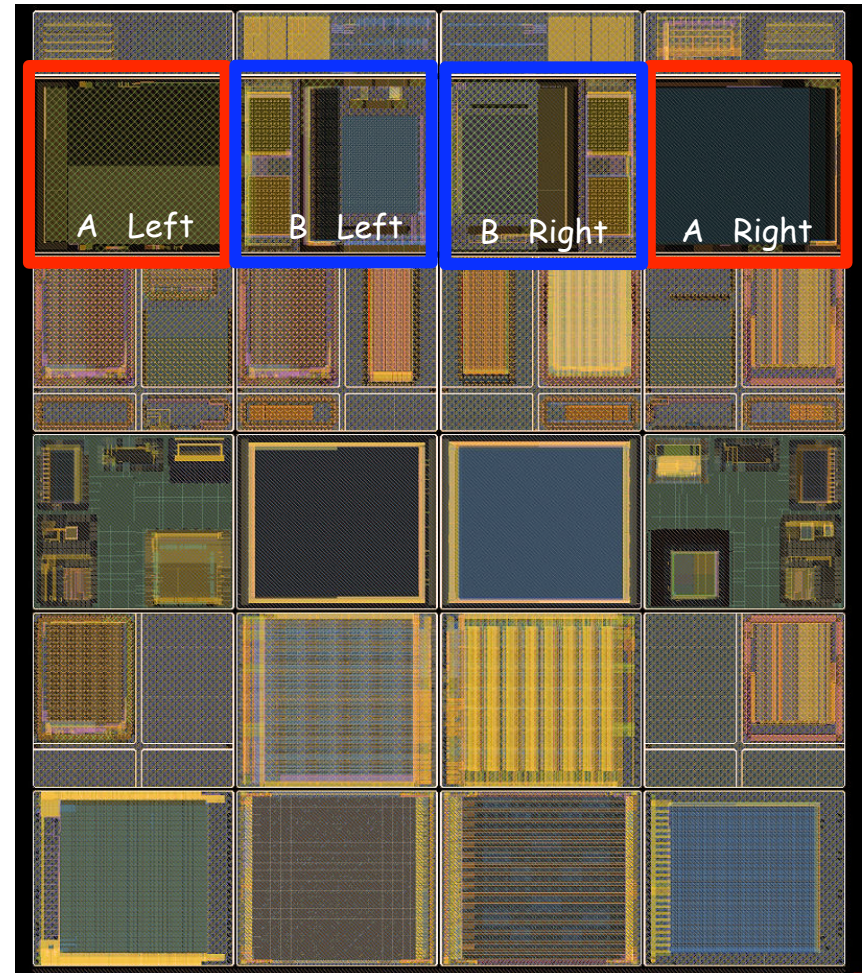


# MPW Run Goals

- ✓ Evaluation of the Chartered process (planar process)
  - ✓ Suitability of process for MAPS
  - ✓ Noise performance and radiation tolerance
  - ✓ Performance of a large number of different circuits exploring many different operating conditions
  
- ✓ Evaluation of 3D processing
  - ✓ Effect of thinning and bonding processes on device performance
  - ✓ Yield of the bond connections between tiers and of the TSV
  - ✓ TSV parasitic effects on the device performance
  - ✓ Digital coupling between the two tiers
  
- ✓ This run should allow for evaluation of many factors
- ✓ Establishment of guidelines for future submissions
- ✓ Better understanding of the 3D design process

# Subreticules A - B

- ✓ **Subreticule A** - Two subcircuits to be bonded to sensors from XFAB (0.35um with HR EPI). An amplifier may be integrated in each sensor pixel
  1. ILC application (**Strasbourg, Saclay**) Rolling shutter, low power tracker, 34 X 240 array, 20 um pitch pixels. Amp, Disc. & latch on analog tier, 1 bit memory& readout on digital tier
  2. ILC and bio-medical applications (**Strasbourg, Bergamo, Pavia**) Self triggering pixel tracker, 245 x 245 array, 20 um pitch with fast X-Y projection readout
  
- ✓ **Subreticule B** - Three subcircuits
  1. MAPS for ILC (**Saclay, Strasbourg**) 42x240 array, 20 um pixel MAPS operating in rolling shutter mode, 80 ns/row, Sensor, amp, Disc & latch (NMOS only) on analog tier. 1 bit memory & readout on digital tier
  2. MAPS for ILC (**Strasbourg**) 128 x192 array, 12x24 um pixel MAPS with 5 bit time stamp, 2<sup>nd</sup> hit marker, full serial readout. Future goal: to use separate sensor tier and to reduce the pixel size to 12x12 um.
  3. 2 separate memory cores (**CMP**) one standard design and one with built-in SEL hardness circuitry.



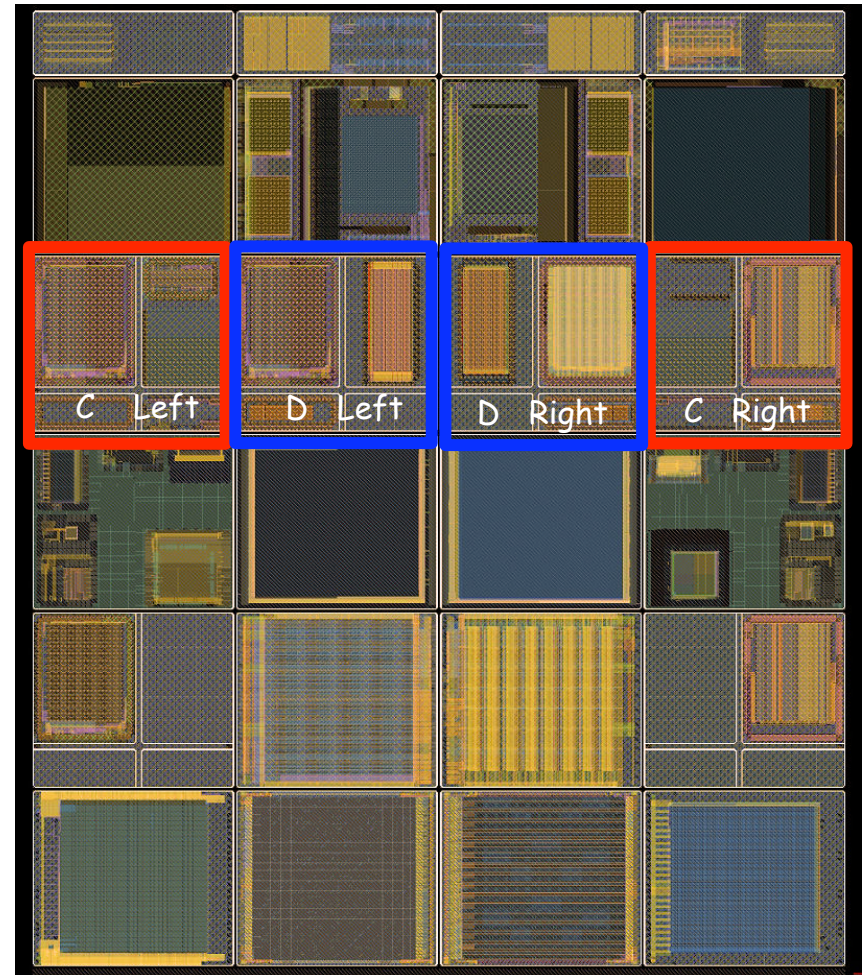
# Subreticules C - D

## ✓ Subreticule C - 4 subreticules

1. ATLAS 2D pixel design based on earlier design in IBM 0.13 um (FEI4)\* (CPPM/Bonn)
  - ✓ Left (analog) side - 14 col, 60 rows, 50x166 um pixels with simple readout
2. SEU resistant register and TSV/bond interface daisy chain to measure TSV as well as bond yield. (CPPM)
3. Test structures to evaluate transistor performance with TSVs in close proximity (CPPM)
4. Test structures to test robustness of circuits under wire bond pads (CPPM)

## ✓ Subreticule D - 3 subreticules

1. ATLAS 3D pixel design foreseen for ATLAS upgrade\* (CPPM/Bonn)
  - ✓ Left (analog) side - 14 col, 60 rows, 50x166 um pixels (same as subreticule C)
  - ✓ Mating right side contains special features such as time stamp, time over threshold, and 4 pixel grouping.
2. Small pixel array for SLHC\* (LAL)
  - ✓ 24 x 64 array of 50 um pixels
  - ✓ ASD, threshold adjustment DAC/pixel, 24 DFF register/pixel
3. TSV capacitance test circuits (CPPM)



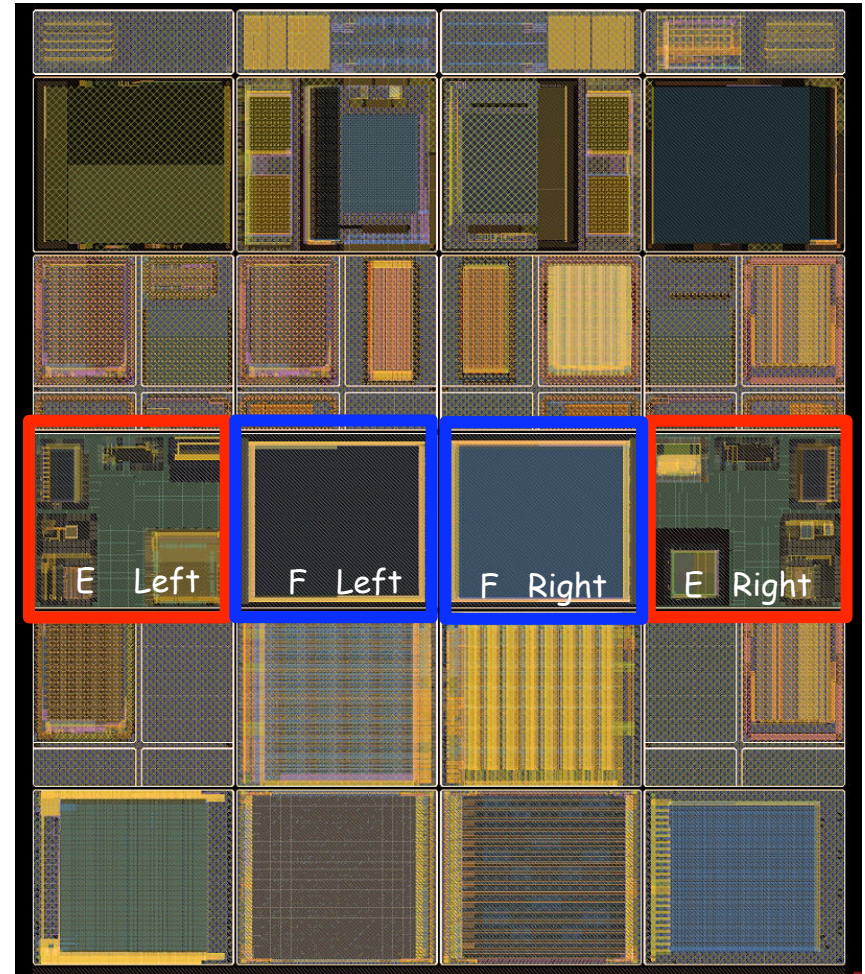
# Subreticules E - F

## ✓ Subreticule E - 7 sub-circuit areas

1. 3D MAPS with 32 x 64 array of 25 um pixels with DCS, 3T FE, discriminator, auto-zeroing. All control logic in digital tier. (Roma)
2. 3D MAPS test structures - Two 3 x 3 40um pitch arrays. One with shaperless preamplifiers. Other is designed with ELT input devices. (Pavia/Bergamo/Pisa)
3. 3D MAPS test structure with 8 x 32 array of 40 um pixels, DNW sensors, data push architecture (Pavia/Bergamo/Pisa/Bologna)
4. Two test structures for the subreticule F DNW MAPS device (Pavia/Bergamo): small matrices, 20um pitch.
5. Two 3D test structures (Pavia, Bergamo, Perugia)
6. 2D version of 3D MAPS device in subreticule F, 64 x64 array of 28 um pixels (Pavia/Bergamo)
7. 2D sub-matrices with 10 and 20 um pixels to test signal to noise performance of MAPS in the Chartered process (Roma)

## ✓ Subreticule F - (Pavia, Bergamo) 3D MAPS

- ✓ 3D MAPS device with 256 x 240 array of 20 um pixels with DNW sensors and sparsification for ILC. The device may be tested with both a full thickness sensor substrate or with sensor thinned to 6 microns.



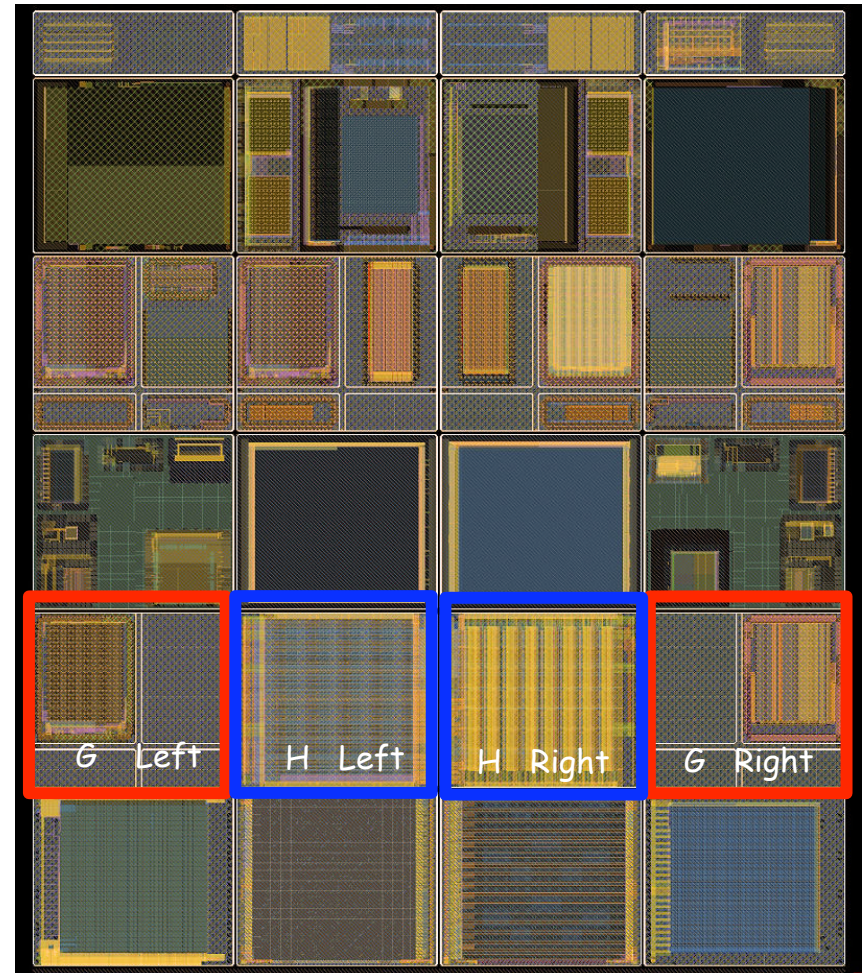
# Subreticules G - H

## ✓ Subreticule G - Orsay/LBNL

1. ATLAS 2D pixel design based on earlier design in IBM 0.13  $\mu\text{m}$  (FEI4)
2. Same design as chip C1 except input is designed for a opposite polarity input signal.

## ✓ Subreticule H - FNAL/CPM/LBNL - 3D chip (VICTR) used as a demonstrator for implementation of PT cut algorithm for tracker trigger in SCMS

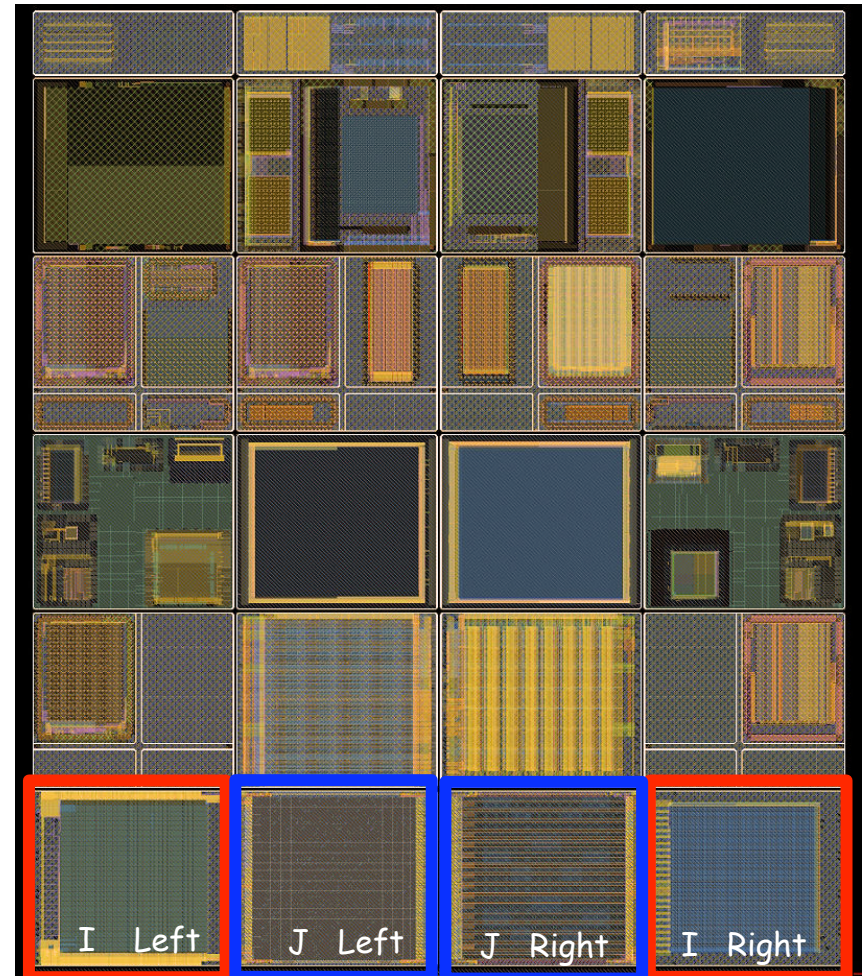
- ✓ Processes signals from 2 closely spaced parallel silicon strip sensor planes (phi and Z planes).
- ✓ Top tier looks for hits from long phi strips and bottom tier looks for coincidence between phi strips and shorter Z strips connected to bottom tier.
- ✓ Designed for 80 micron pitch sensors
- ✓ Serial readout of all top and bottom strips along with coincidence information
- ✓ Downloadable hit patterns
- ✓ Fast OR outputs
- ✓ Circuit to be thinned to 24 microns and connections made to both the top and bottom of the chip.





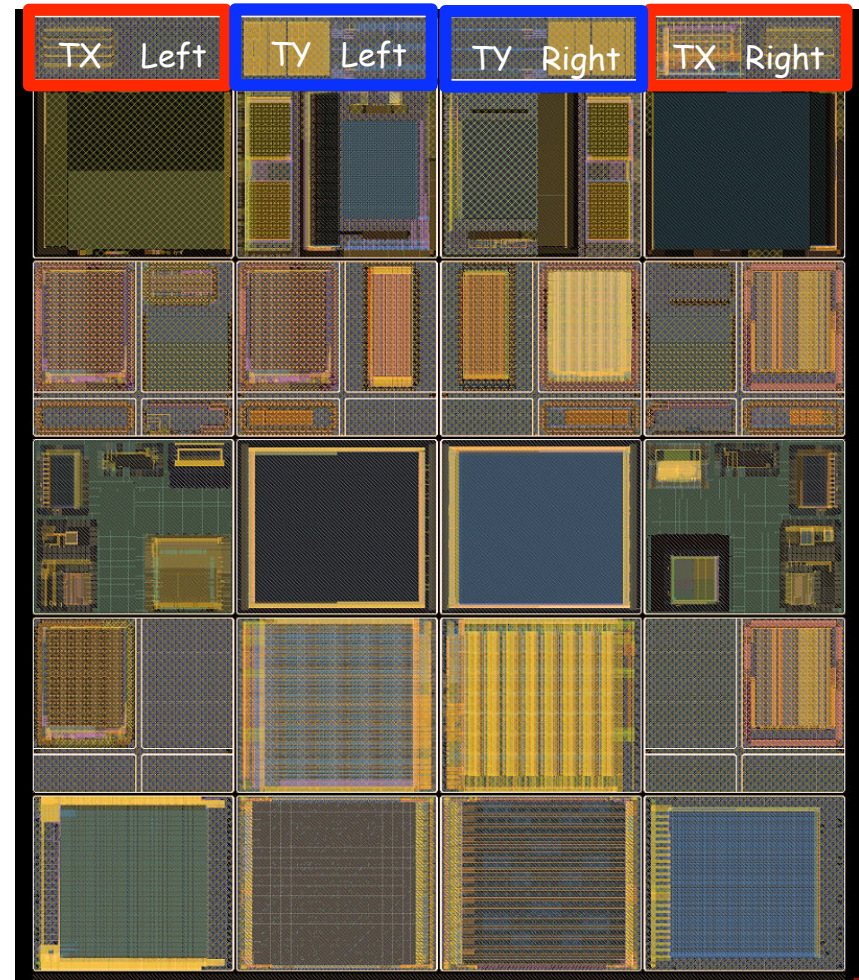
# Subreticules I - J

- ✓ **Subreticule I** - FNAL - 3D demonstrator chip (VIP2b) for ILC vertex detector with separate bonded sensor
  - ✓ Adapted from earlier MIT LL designs in SOI technology
  - ✓ 192 x 192 array of 24 micron pixels
  - ✓ 8 bit digital time stamp
  - ✓ Data sparsification
  - ✓ DCS analog signal information output
  - ✓ Separate test input for every pixel cell
  - ✓ Serial output bus
- ✓ **Subreticule J** - Three subcircuits FNAL/AGH-UST/BNL - 3D demonstrator chip (VIPIC) for X-ray Photon Correlation Spectroscopy to be bonded to a separate sensor.
  - ✓ 64 x 64 array of 80 micron pixels
  - ✓ Separate Analog and digital tiers
  - ✓ Sparsified, binary readout
  - ✓ High speed frame readout
  - ✓ Optimized for 8 KeV photons
  - ✓ Triggerless operation
  - ✓ 16 Parallel serial output lines
  - ✓ Two 5 bit counters/pixel for dead timeless recording of multiple hits per time slice
  - ✓ Innovative binary tree pixel addressing scheme



# Subreticules TX - TY

- ✓ **Subreticule TX** - Test transistors for noise, radiation, and cryo measurements
  1. NMOS and PMOS transistor array with nominal  $V_t$ , low  $V_t$ , thick gate oxide I/O, 0  $V_t$ , and 0  $V_t$  thick gate oxide. Measured devices are thinned. (PAVIA).
  2. NMOS and PMOS transistor array with different numbers of fingers/transistor for measurements at cryo temperatures. Devices can be measured on thick or thin substrate. (FNAL)
- ✓ Test circuits for VIP2b in subreticule I - (FNAL) Double correlated sampler, Single channel FE, Front ends with different W/L input transistors, Stand alone discriminator
- ✓ **Subreticule TY** -- (FNAL)
  1. Two long daisy chains of bond interconnects to measure interconnect yield.
    - ✓ Two different daisy chains having different bond interface patterns
    - ✓ Each daisy chain has 140000 bond interconnects with multiple taps
  2. Test transistors based on a standard set of devices (~46) used by CERN to characterize different processes.
    - ✓ Devices can be measured under different conditions: on standard wafers (2D wafers), on thin substrate bonded to a thick second wafer, on thick substrate bonded to a thinned second wafer

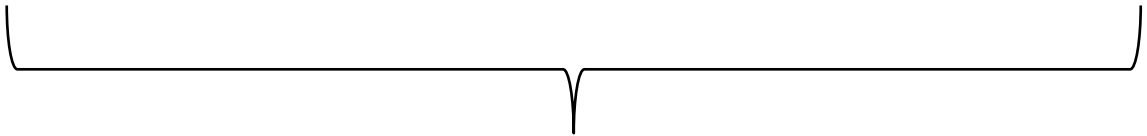


# 3D technology options for the SuperB SVT

- Design of the SVT layer0 at SuperB has to comply with severe requirements
  - Large background,  $>5\text{MHz/cm}^2$ , small thickness,  $<0.5X_0$
- Two options made available by 3D technologies are being pursued

Vertical integration between 3D ROC and high resistivity pixels

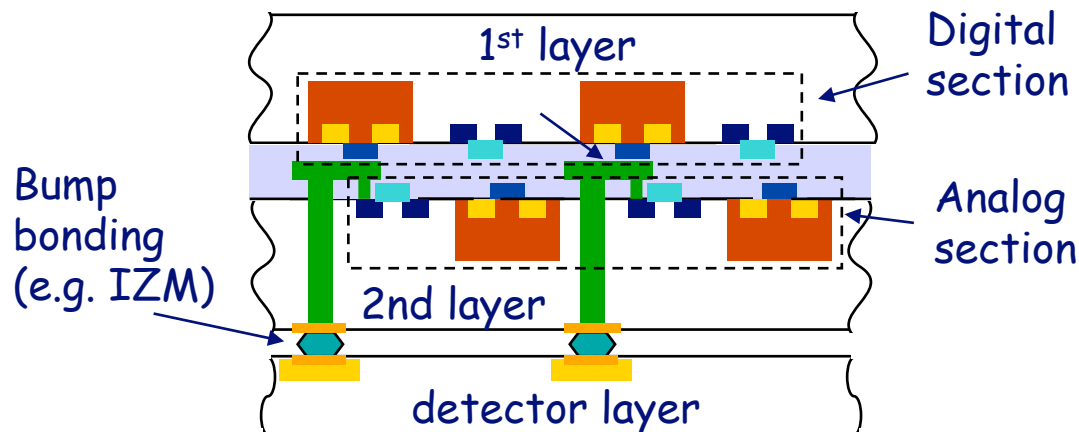
3D Deep N-well CMOS monolithic sensors (DNW-MAPS)

- 
- ✓ Analog channel optimization for MAPS and hybrid pixels
  - ✓ New readout architecture under development with higher efficiency and better time-stamp granularity ( $\approx 100\text{ns}$ )
    - ✓ Data push architecture with readout time-stamp ordered (time-stamp latched in-pixel)
    - ✓ Could evolve to a triggered architecture

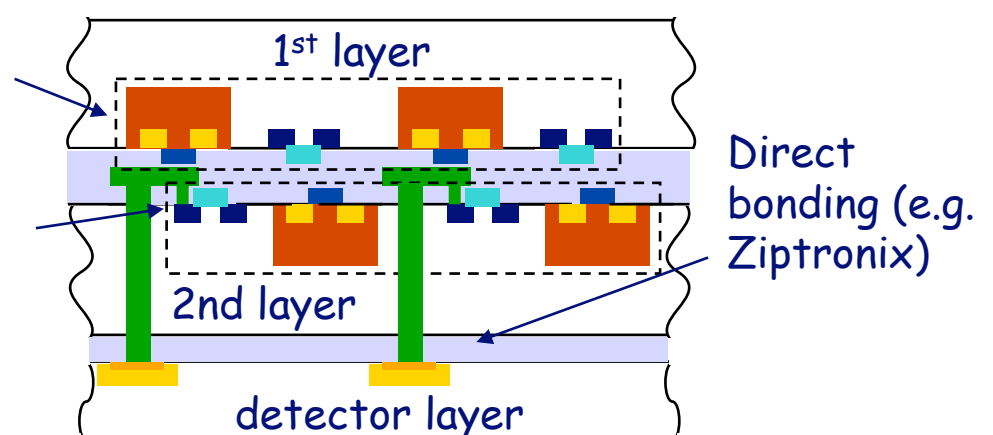
# VI between 3D ROC and High Resistivity Pixels

- ✓ High resistivity pixels:
  - ✓ larger signal available from detector
  - ✓ more advantageous trade-off between S/N and dissipated power
- ✓ Bump bonding can have significant mass and represent a high  $X_0$  for fine pitch assemblies or high density interconnections
- ✓ In the next MPW run, development of a 3D front-end chip (32x128, 50um pitch) to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique

Fine pitch (50um) bump bonding (IZM, Munich),  
with a 2D FE chip in progress,  
with a 3D FE chip in the future

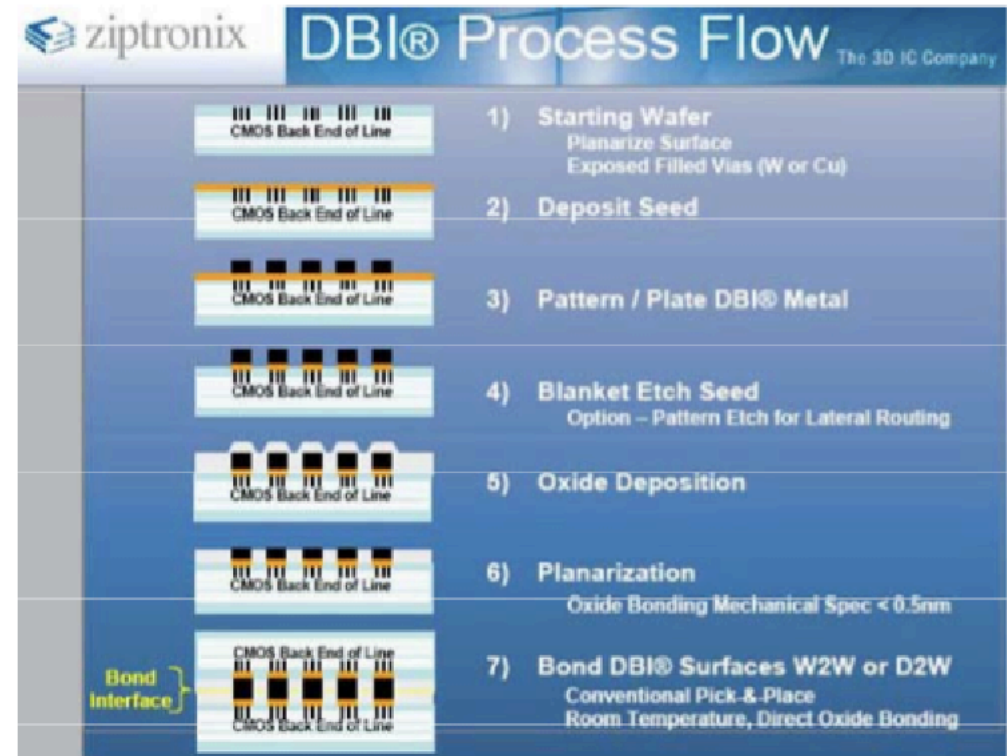
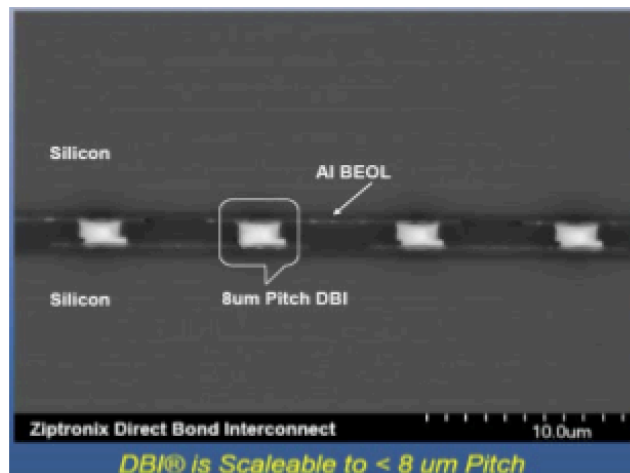


Other technologies (Direct Bonding by  
Ziptronix) will be investigated in the future



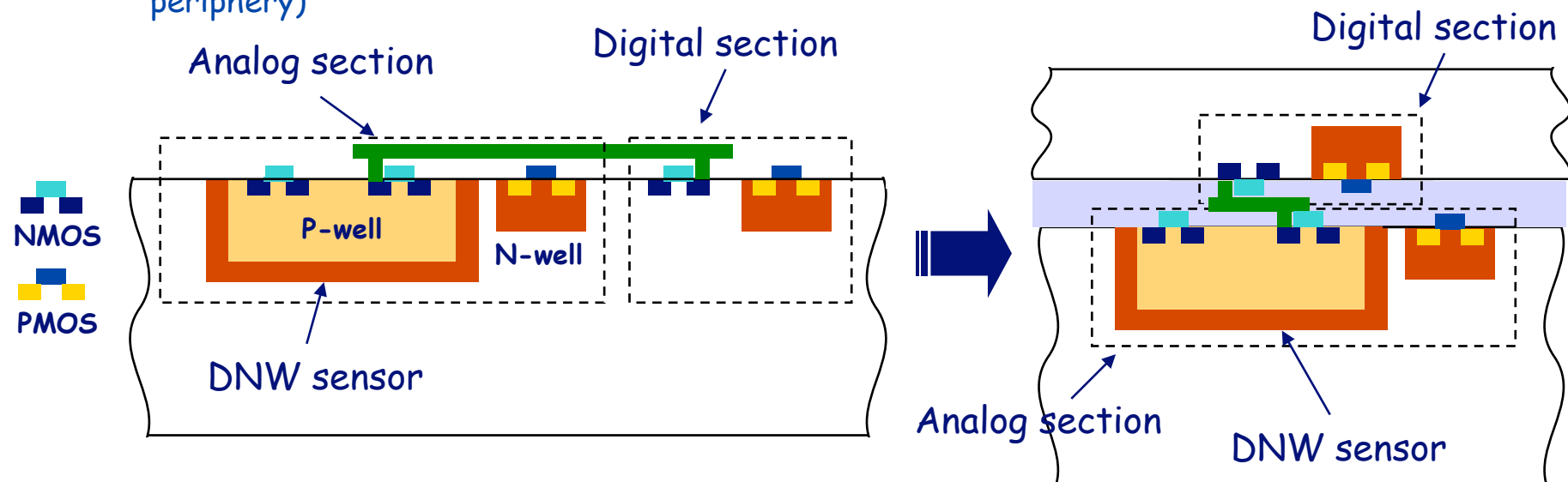
# VI between 3D ROC and High Resistivity Pixels: Ziptronix

- ✓ Ziptronix is located in North Carolina
- ✓ Tezzaron and Ziptronix have formed a good alliance
- ✓ Orders accepted from international customers
- ✓ Ziptronix uses Direct Bonding Interconnect (DBI) process  $X_0 < 0.001\%$
- ✓ Can provide fine pitch, very low mass interconnections



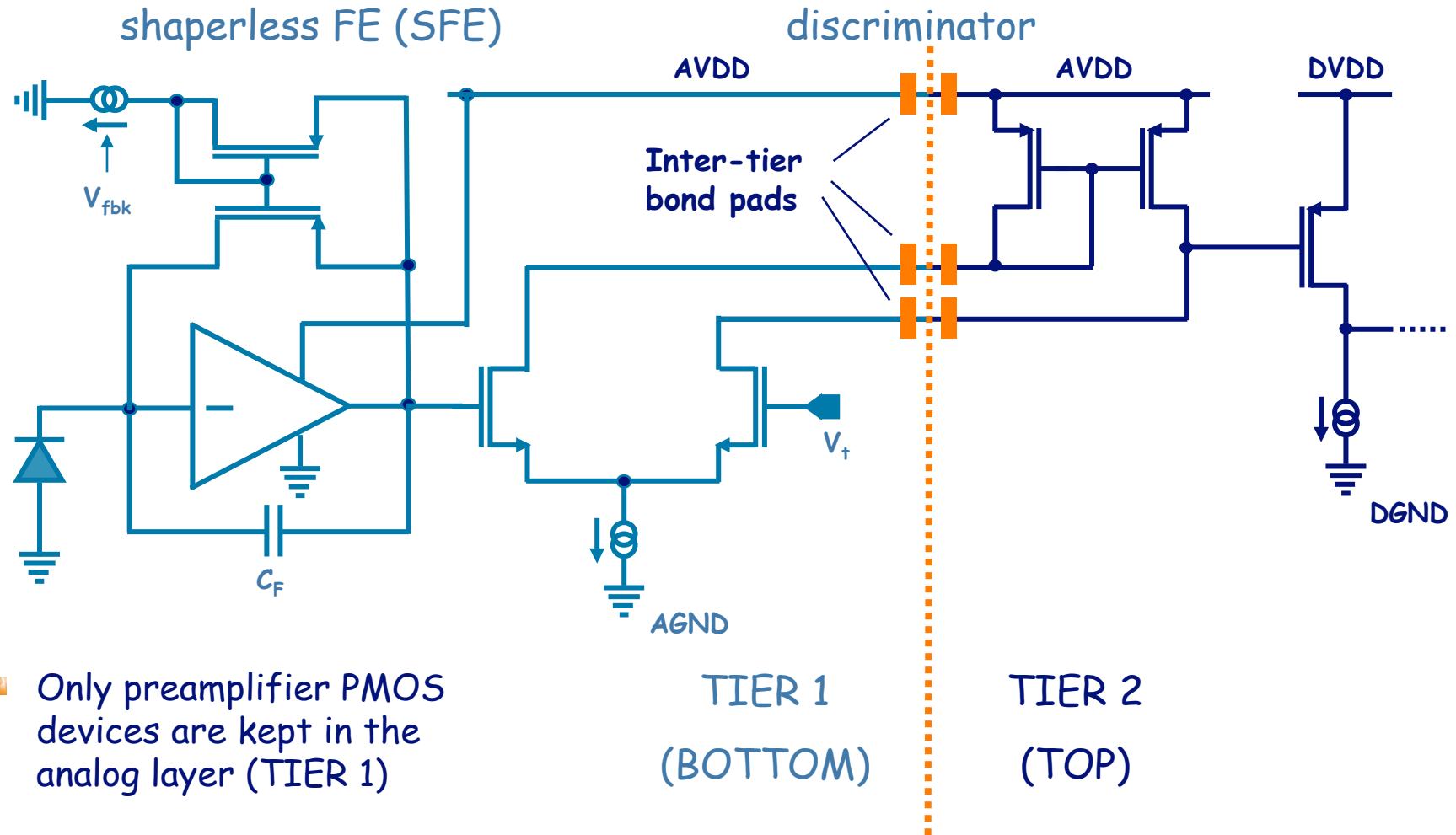
# 3D DNW MAPS

- ✓ Separate analog from digital section to minimize cross-talk between digital blocks and sensor/analog circuits
  - ✓ less PMOS in the sensor layer → improved collection efficiency
  - ✓ more room for both analog and digital power and signal routing (in planar CMOS MAPS scaling to suitably large matrices is forbidden by the need for point-to-point lines from macropixels to periphery)



- **Tier 1:** collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- **Tier 2:** digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

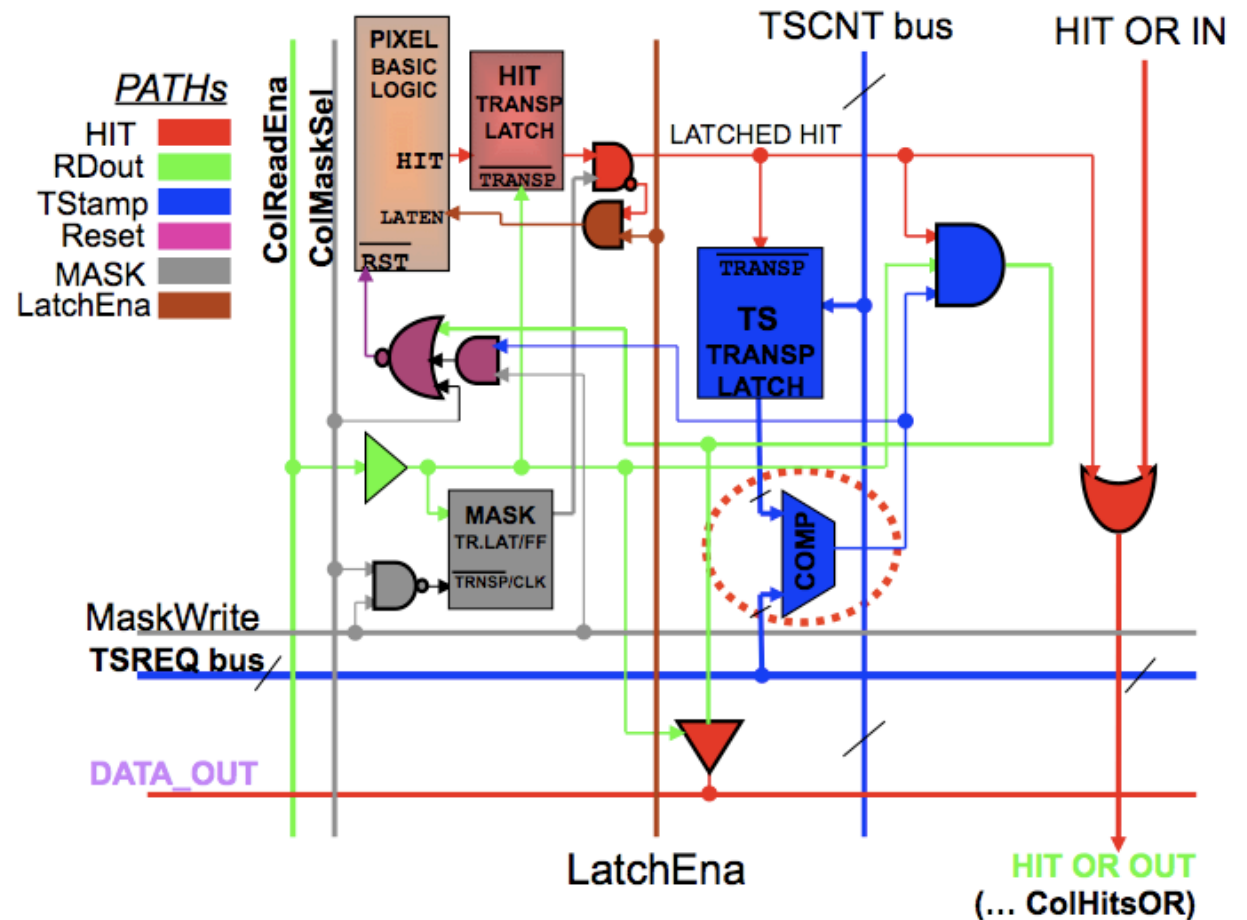
# Analog FE and discriminator



- Only preamplifier PMOS devices are kept in the analog layer (TIER 1)

# Pixel-level logic for a time-ordered readout

- ✓ A readout time stamp enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that time stamp
- ✓ A column is read only if HIT-OR-OUT=1
- ✓ DATA-OUT (1 bit) is generated if the active column has hits associated to a selected time stamp



Courtesy of F. Morsani (INFN PI)



# Conclusions

- ✓ A group of 15 institutions has come together to participate in the first HEP multi-project run for 3D circuits (now 17)
- ✓ This HEP MPW run was a learning experience for the HEP community
- ✓ The final frame was accepted by the mask house in March 2010
- ✓ Fabrication order for 31 wafer (8") in Chartered 0.13um
  - ✓ 3 wafers to be delivered for 2D testing in July
  - ✓ Remaining wafers assembled into 3D stacks (4 weeks later 2D)
- ✓ A consortium meeting was held late in March in Marseille to review the first MPW run and to plan for the future

## CMC-CMP-MOSIS partnership on 3D ICs

- ✓ CMC, CMP, MOSIS already cooperating since several years offering commonly some processes, and sharing the manufacturing prices. They are engaging this time to provide 3D-ICs services
- ✓ Roles of each partner:
  - ✓ MOSIS is the main contractor with Tezzaron and will cluster the final reticules
  - ✓ CMP is the main support center (3D LVS, Fill subroutines, Libraries, ...)
  - ✓ All three address their respective regions for the access to the process and the local technical support
- ✓ The new tool set is expected by the end of the June
- ✓ It is anticipated that the 3D consortium will use the services of MOSIS/CMP/CMC for future runs
- ✓ The Tezzaron process is the one chosen because of the opportunity of the successful first MPW run organized by Fermilab. Other processes can be explored if they offer different features than Tezzaron



## Future activity

- ✓ We have gained a great deal of experience which will help us in future submissions
- ✓ Preliminary evaluation of run #1
- ✓ 3D IC Consortium have already planned a second MPW run for the end of 2010
  - ✓ Sufficient expression of interest to fill a full frame rather than just a 1/2 frame as in the MPW run #1
- ✓ Italian collaboration (VIPIX) confirms interest in the next MPW run for 150mm<sup>2</sup> of 3D stacked chips (300mm<sup>2</sup> in terms of planar silicon). VIPIX is scheduling design work for a deadline at December 2010
  - ✓ DNW MAPS: 192x96, 50um pitch,
  - ✓ FE for hybrid pixels: 128x32, 50um pitch
  - ✓ DIGIMAPS structures (Roma3)
  - ✓ Stacked CMOS MAPS (Perugia)
- ✓ The 3D IC Consortium will continue to provide a venue to discuss design issues and compare test results

# Acknowledgments

I would like to acknowledge:

- ✓ The designers who contributed toward the first 3D Multi-Project Wafer run of the Consortium
- ✓ Valerio Re, Massimo Manghisoni, Lodovico Ratti and Ray Yarema for providing information and useful discussions