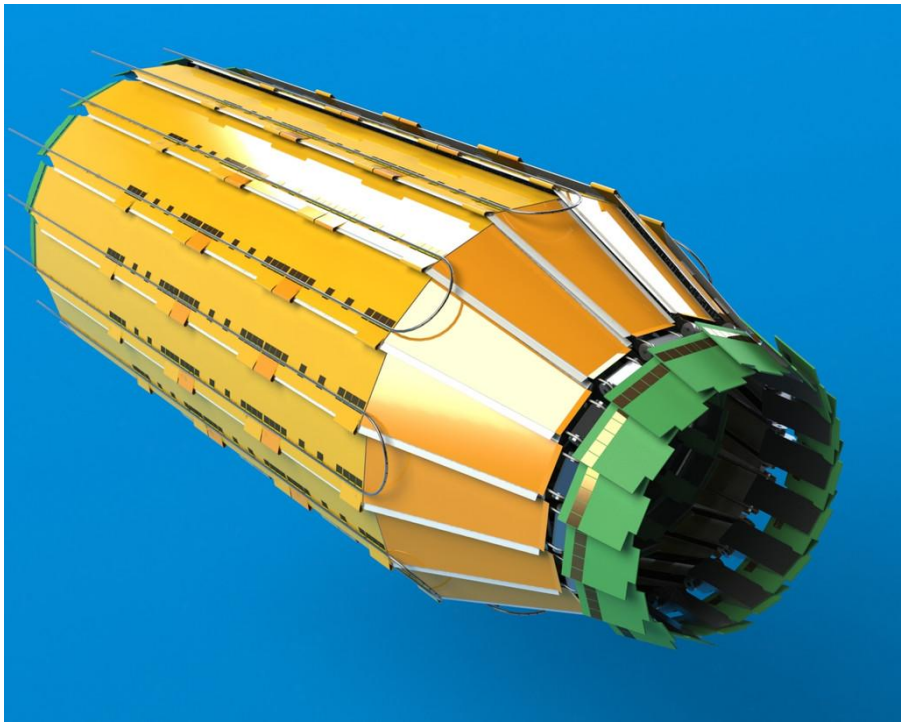
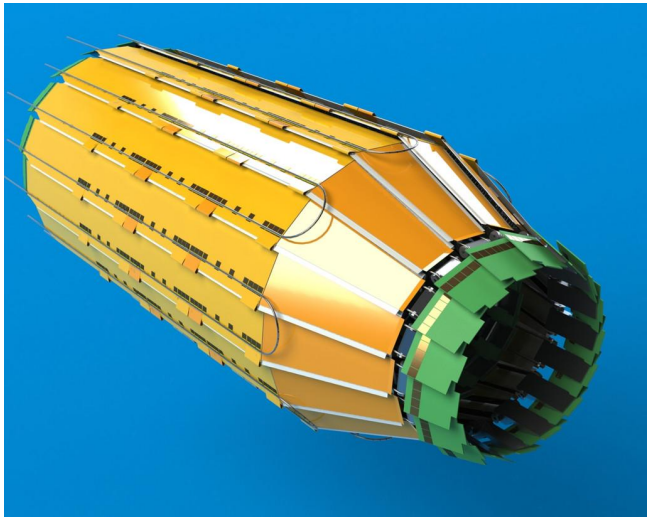


The Silicon Vertex Detector of the Belle II Experiment

Thomas Bergauer (HEPHY Vienna)

Vertex 2010 Loch Lomond 10 June 2010



Introduction

Belle II: The Future

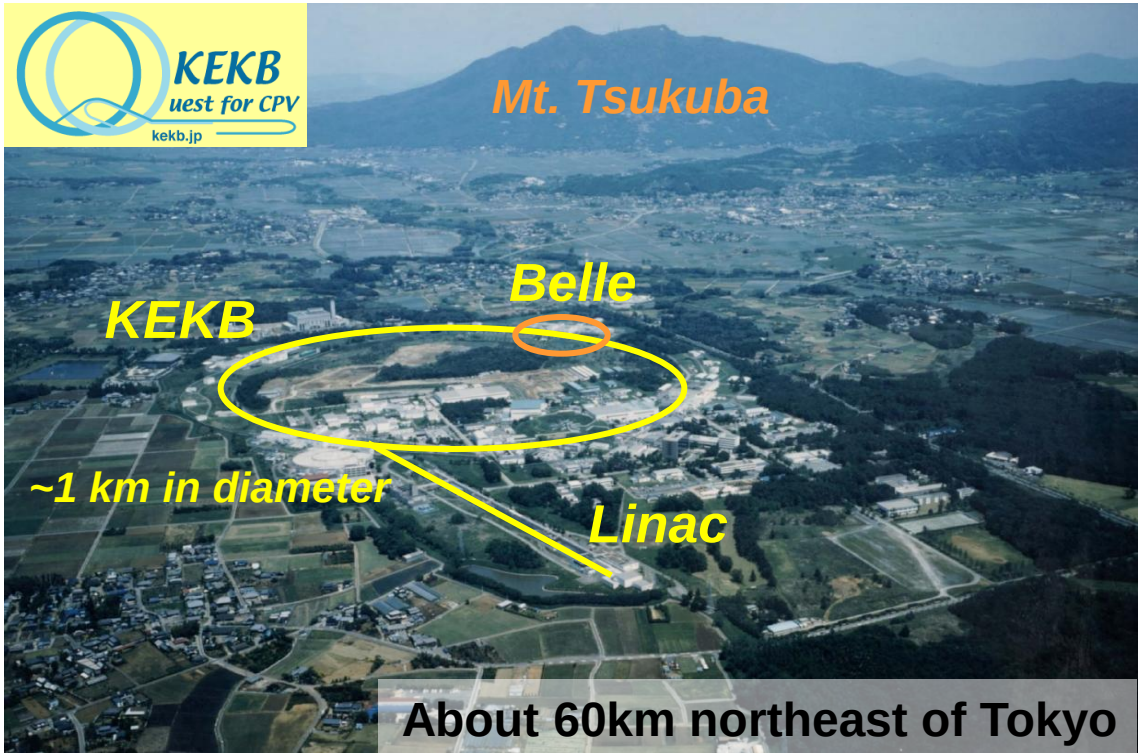
Double Sided Sensors

SVD-II Components

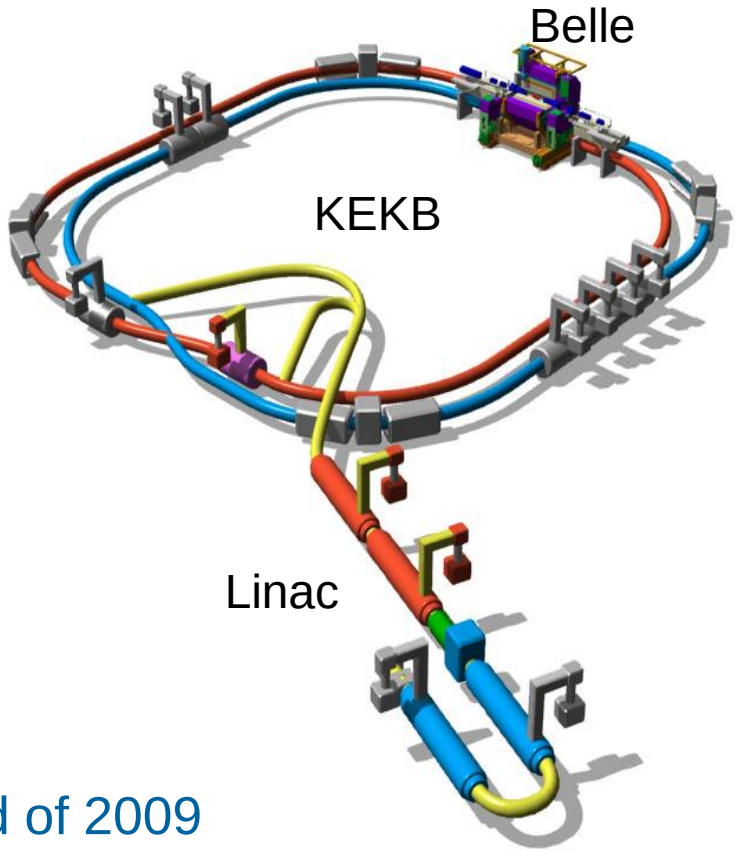
Readout System

Summary

KEKB and Belle @ KEK

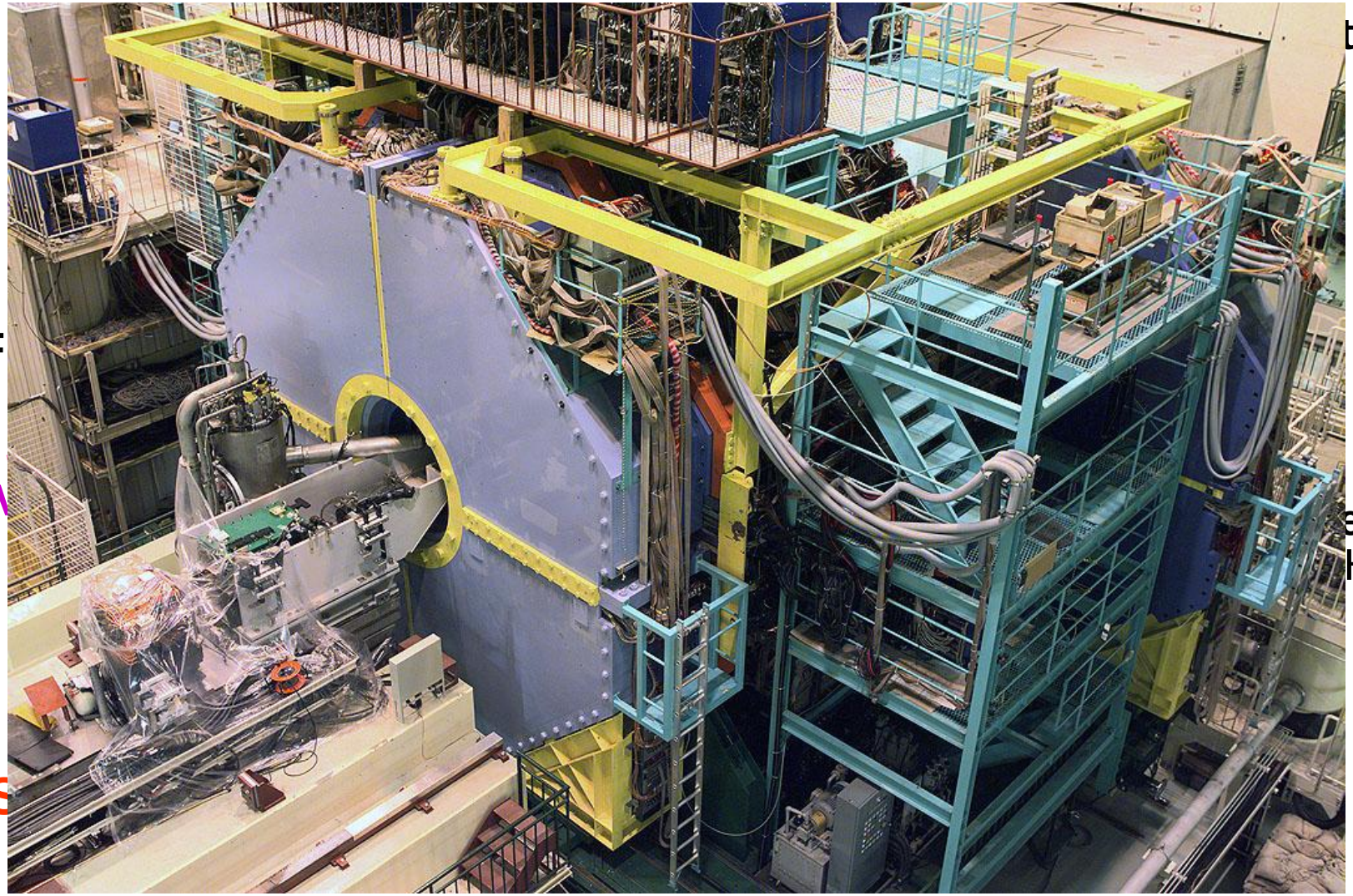


- **Asymmetric** machine: 8 GeV e^- on 3.5 GeV e^+



- Center of mass **energy**: Y(4S) (10.58 GeV)
- **High intensity** beams (1.6 A & 1.3 A)
- Integrated luminosity 1 ab^{-1} recorded by end of 2009

Belle Detector (1999– 20. June 2010)



TOF

8 GeV

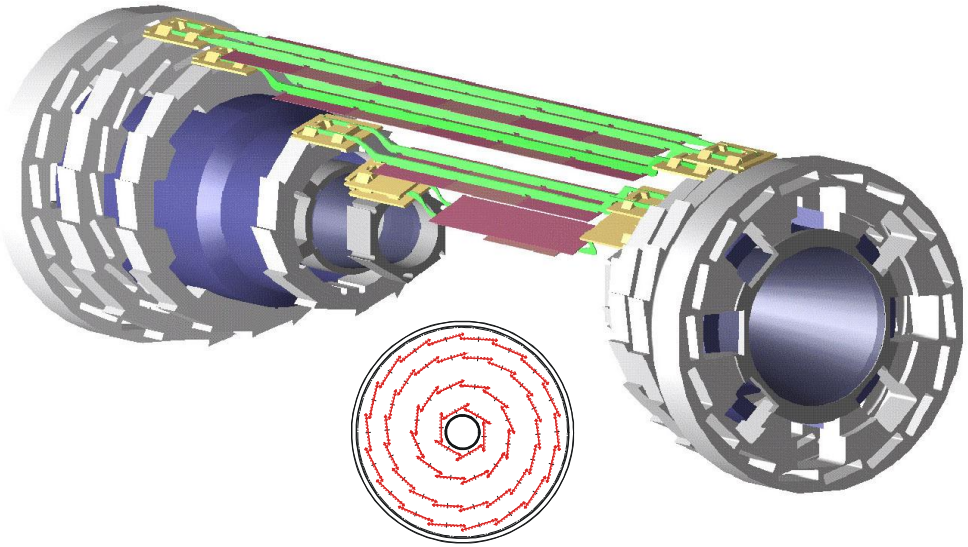
ter

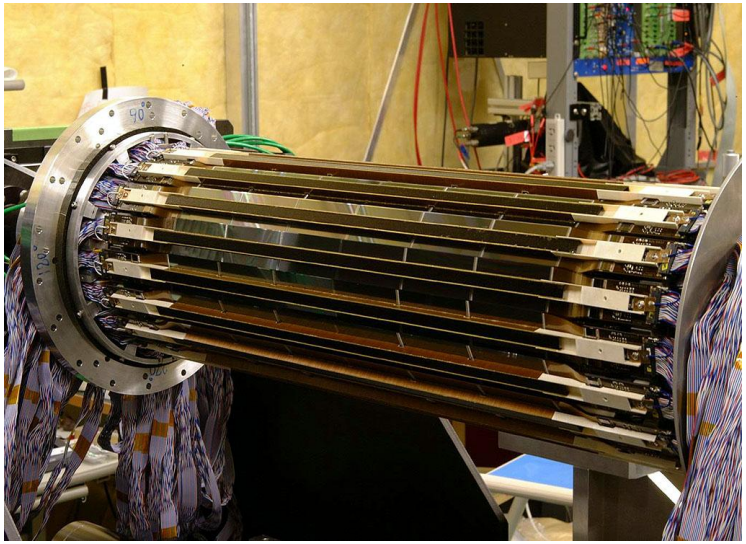
er

H_5

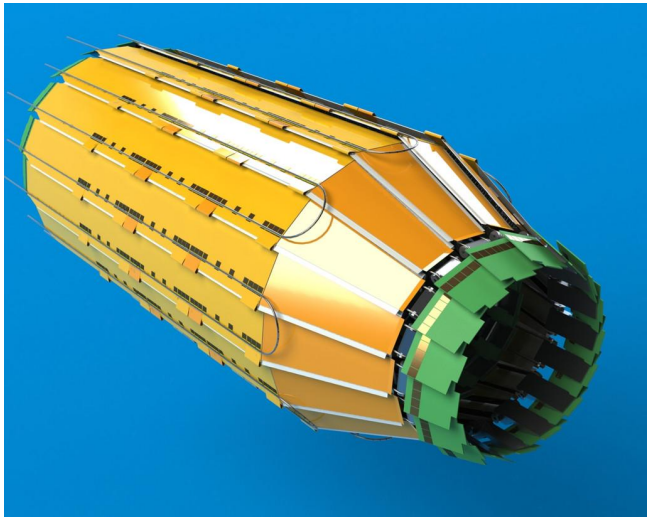
S

The Present SVD – Overview





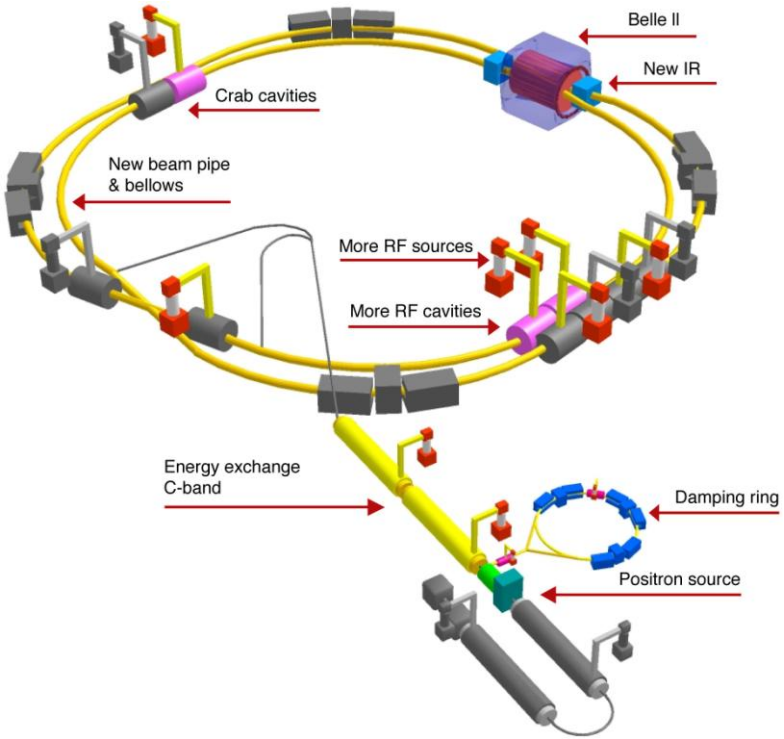
- **4 layers** (6/12/18/18 ladders), r = 2.0…8.8 cm
- 17°…150° polar angle coverage
- 246 **double sided** silicon detectors (DSSDs), 0.5 m^2 overall active area
- **VA1TA** readout chip (Viking variant; 800ns shaping time)
- **110592** channels in total

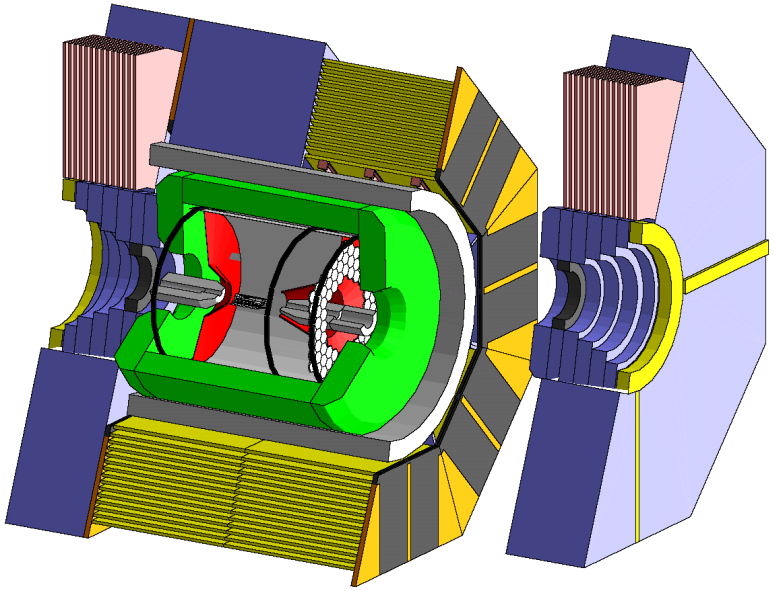


Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary

KEKB/Belle upgrade (2010–2014)

- Aim: super-high luminosity ~8×10^{35} $cm^{-2}s^{-1}$ $\rightarrow$ 1×10^{10} $B\bar{B}$ / year
- LoI published in 2004; TDR was written in spring this year and is presently under review
- Refurbishment of accelerator and detector required

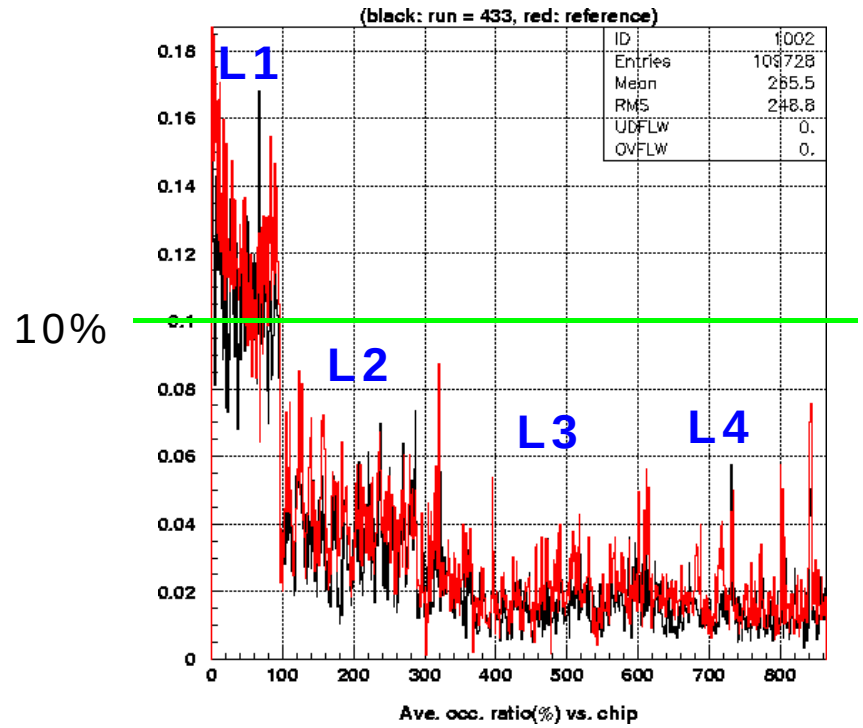




http://belle2.kek.jp

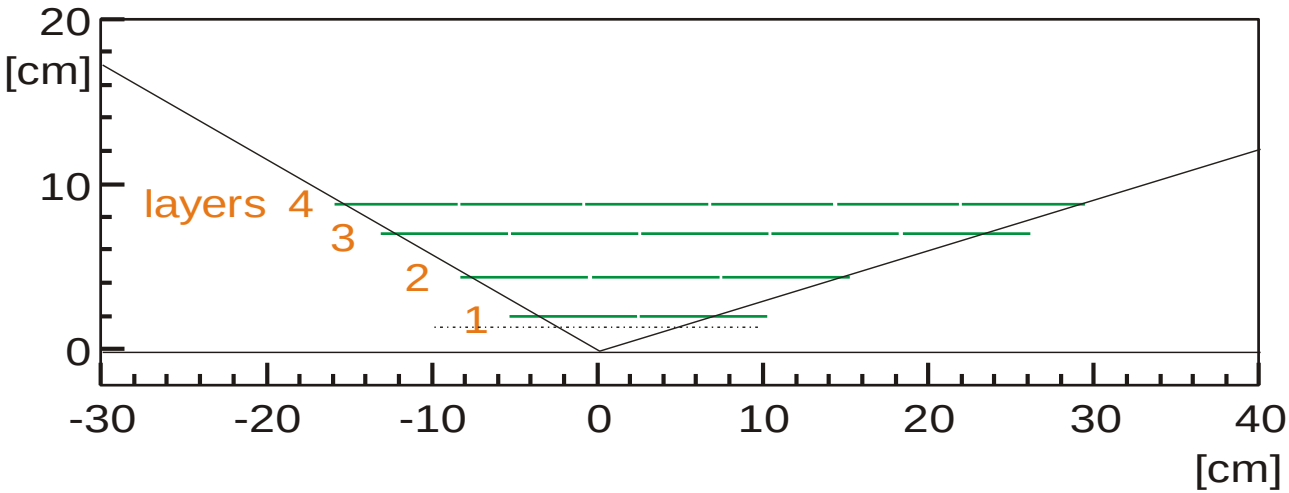
Belle II SVD Upgrade (2010–2014)

- Ultimately **40-fold increase in luminosity** (~8×10^{35} $cm^{-2}s^{-1}$)
- Present SVD limitations are
  - **occupancy** (currently ~10% in innermost layer)
    → need faster shaping
  - **dead time** (currently ~3%)
    → need faster readout and pipeline
- Needs Detector with
  - high **background tolerance**
  - **pipelined** readout
  - **robust tracking**
  - **low material budget** in active volume (low energy machine)

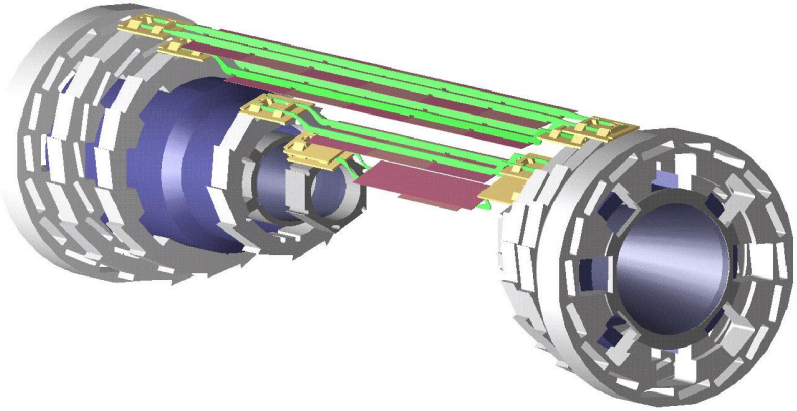


Current SVD is not suitable for Belle II

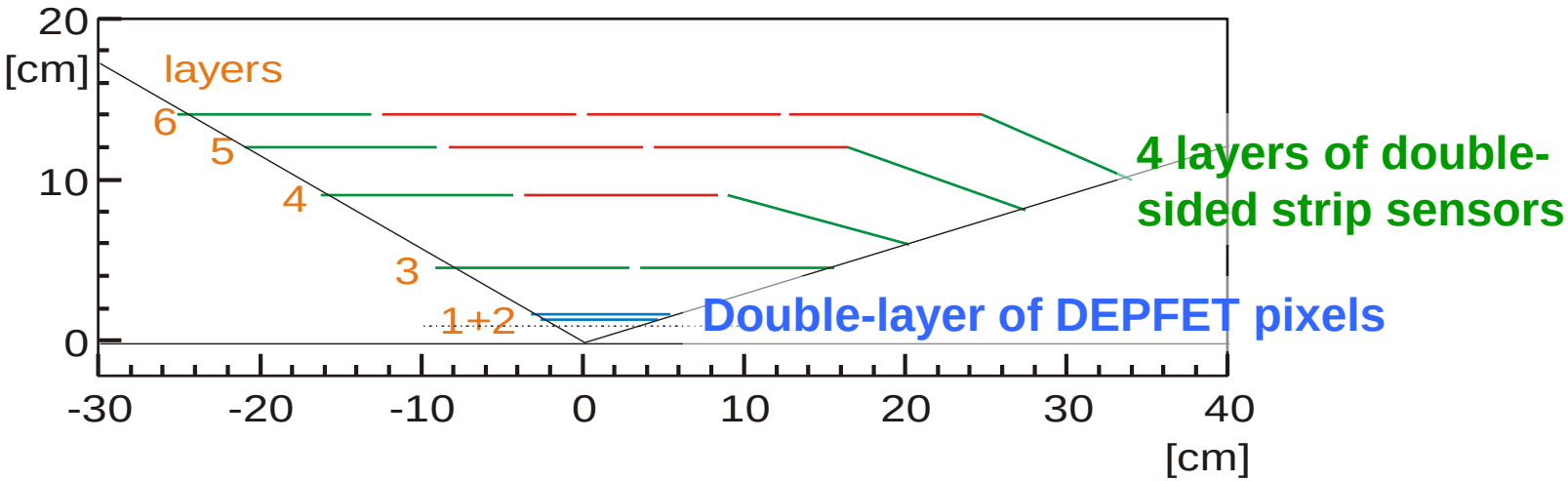
Present SVD Layout (until 2010)



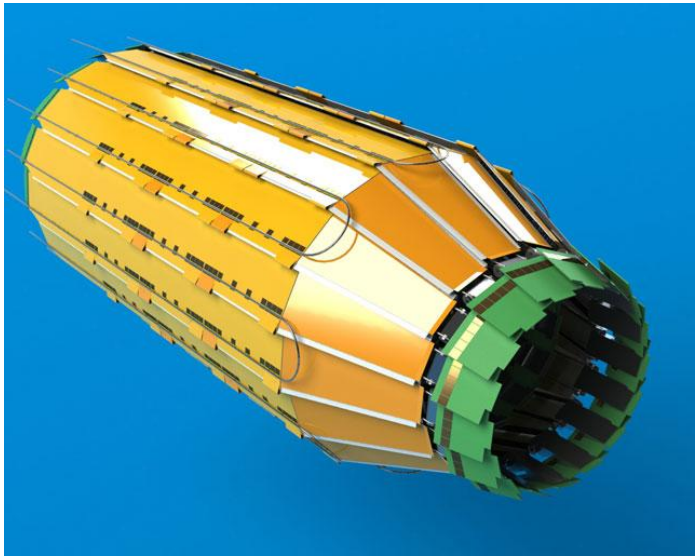
ed silicon detectors (DSSDs)

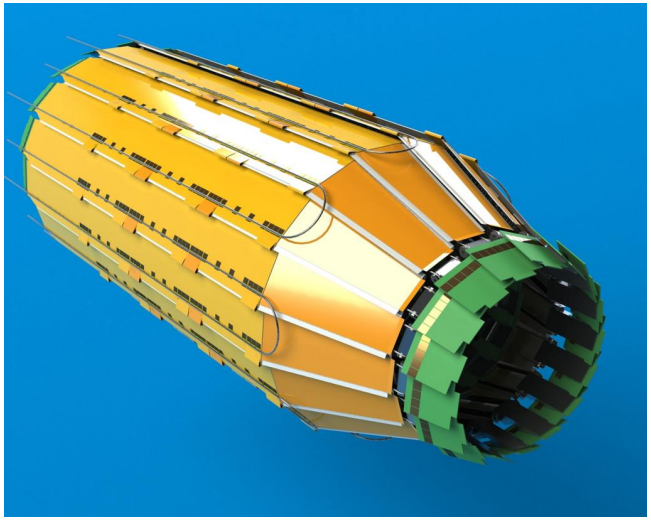


SVD-II Layout (2014-)



- Geometry optimization is underway
- New central pixel double-layer using **DEPFET**
- Strip layers extend to r~14 cm
- Every sensor is **read out individually** (no ganging) to maintain good S/N → chip-on-sensor concept



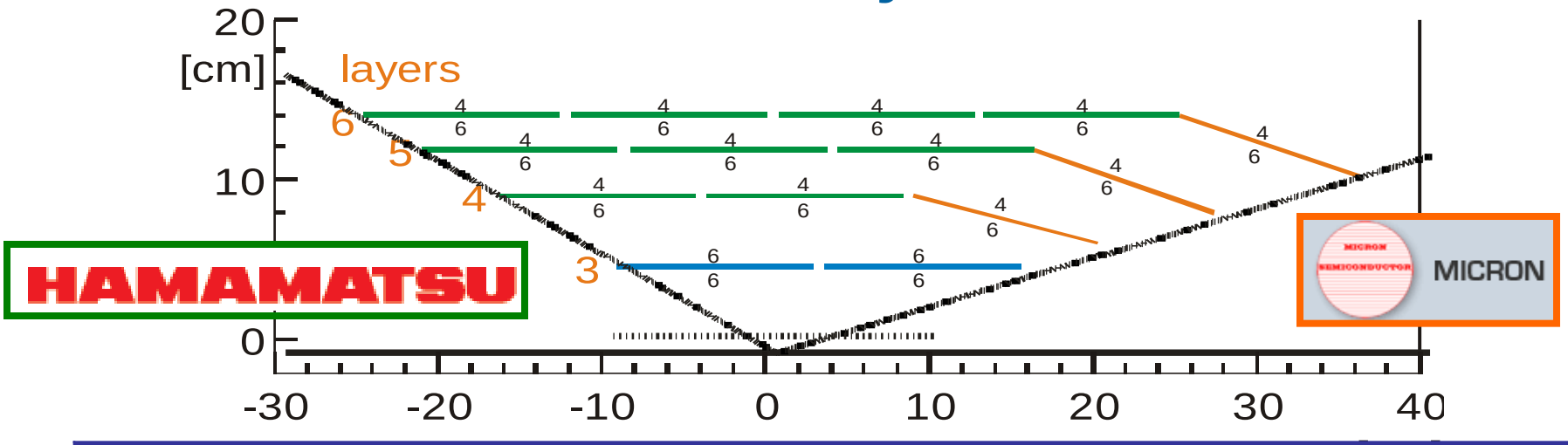


Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary

Vendors for 6” DSSD

- Aim is to use double sided silicon detectors with **AC-coupled** readout and **poly-silicon resistor** biasing from **6 inch wafer**
- **Hamamatsu** decided in the past to abandon the production of double sided sensors
- Thus, negotiations with **Canberra**, **SINTEF** and **Micron** started
- Finally **HPK** could be convinced to **restart DSSD** production on 6” wafers
- 6” prototypes ordered from
  - **Hamamatsu** (rectangular): First batch delivered in April
  - **Micron** (trapezoidal): First batch in July

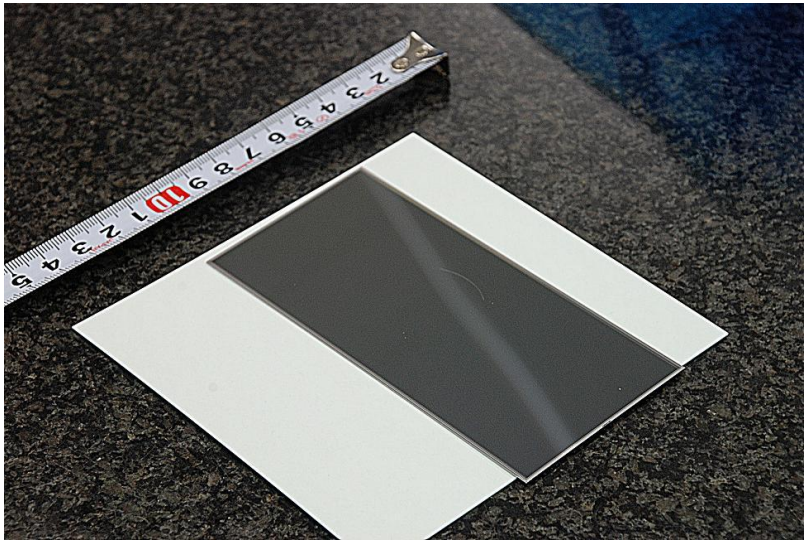
SVD Layout

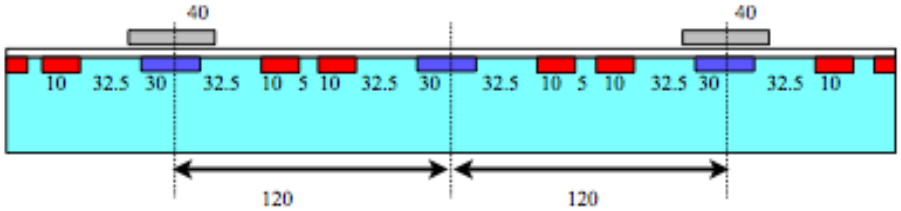


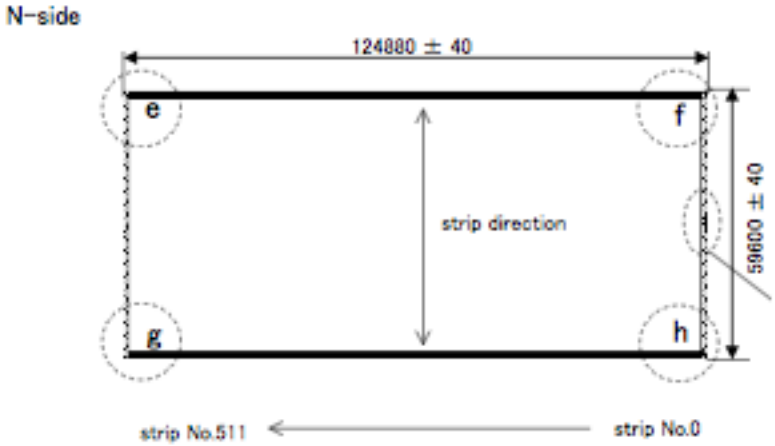
Layer	# Ladders	Rect. Sensors [50µm]	Rect. Sensors [75µm]	Wedge Sensors	APVs
6	17	0	68	17	850
5	14	0	42	14	560
4	10	0	20	10	300
3	8	16	0	0	192
Sum:	**49**	**16**	**130**	**41**	**1902**

First batch from HPK

- First 20 pieces of 6'' sensors have been delivered in April 2010
- Technical details:
  - Dimensions: 59.6 x 124.88 mm
  - p-side:
    - Readout pitch: 75 µm
    - 768 strips
  - n-side:
    - Readout pitch: 240 µm
    - 512 readout strips n-side
    - P-stop scheme







First Batch of 6” DSSD from HPK

- Electrical Characterization
  - IV, CV
  - Stripscan (p- and n-side)
  - Longterm stability vs. temperature and humidity
  - Inter-strip resistance and capacitance currently under investigation
- Pull-tests to show bondability ok

Trapezoidal Sensors (Micron)

- Full wafer designed using self-developed framework
- Including test structures and mini sensors to test different p-stop designs
- Delivery due July 2010

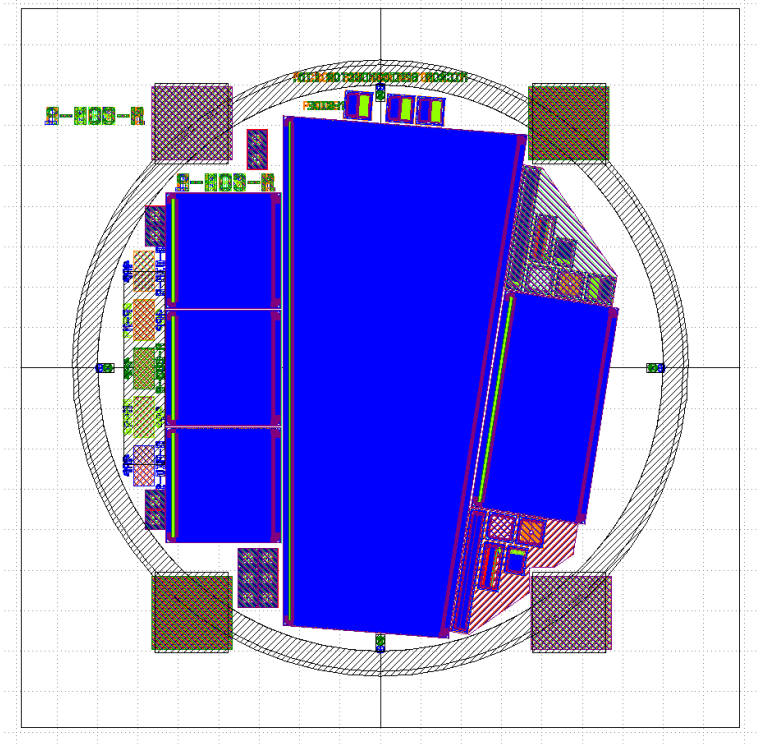
Sensor “programming language”

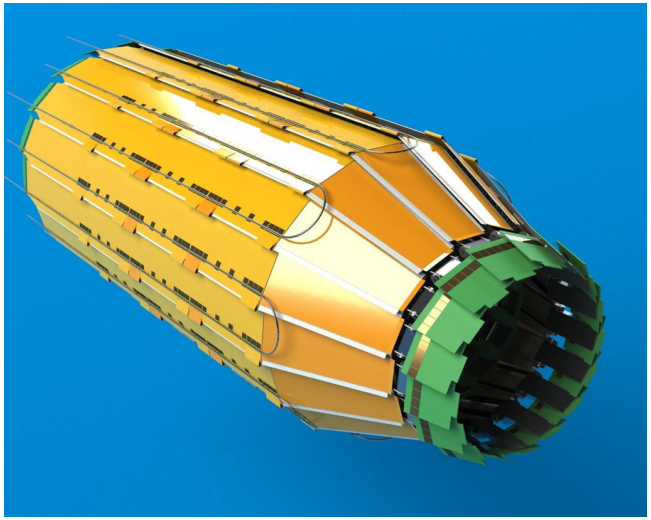
```
mentor@dbserver:~/AMPLE/ONSEMI/FUNCTIONS
// Sensor
extern SensorPitch=50;
extern SensorSizeX=10000;
extern SensorSizeY=100000;
extern SensorCutMargin=100;
extern SensorGuardSpacing=50;
extern SensorGuardBiasSpacing=100;
extern SensorBiasStripSpacing=50;

// GuardRing
extern GuardNRings=10;
extern GuardWidth=100;
extern GuardCornerRadius=30;
extern GuardCornerPoints=20;

// BiasRing
extern BiasWidth=100;
extern BiasCornerRadius=30;
                                        53,1          42%
```

Trapezoidal sensor with test structures

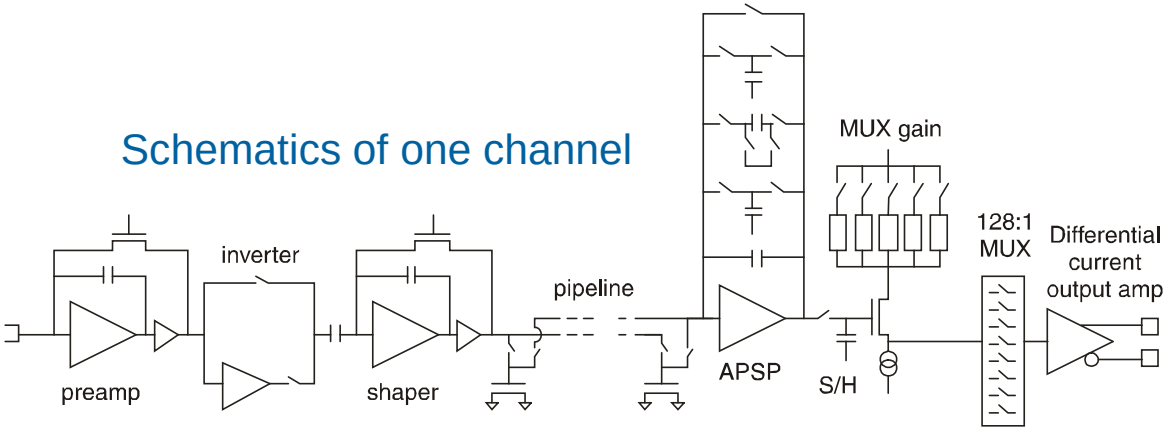


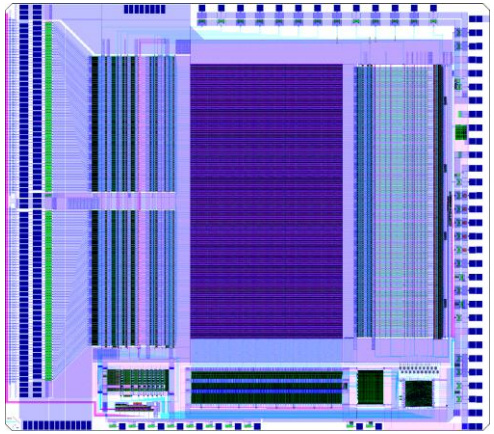


Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary

APV25 Readout Chip

Schematics of one channel





- Developed for **CMS** (LHC) by IC London and RAL (70k chips installed)
- 0.25 µm CMOS process (**>100 MRad tolerant**)
- **40 MHz clock** (adjustable), 128 channels
- **192 cell analog pipeline** → no dead time
- **50 ns shaping time** → low occupancy
- **Noise:** 250 e + 36 e/pF → must minimize capacitive load!!!
- **Multi-peak mode** (read out several samples along shaping curve)
- **Thinning** to 100µm successful

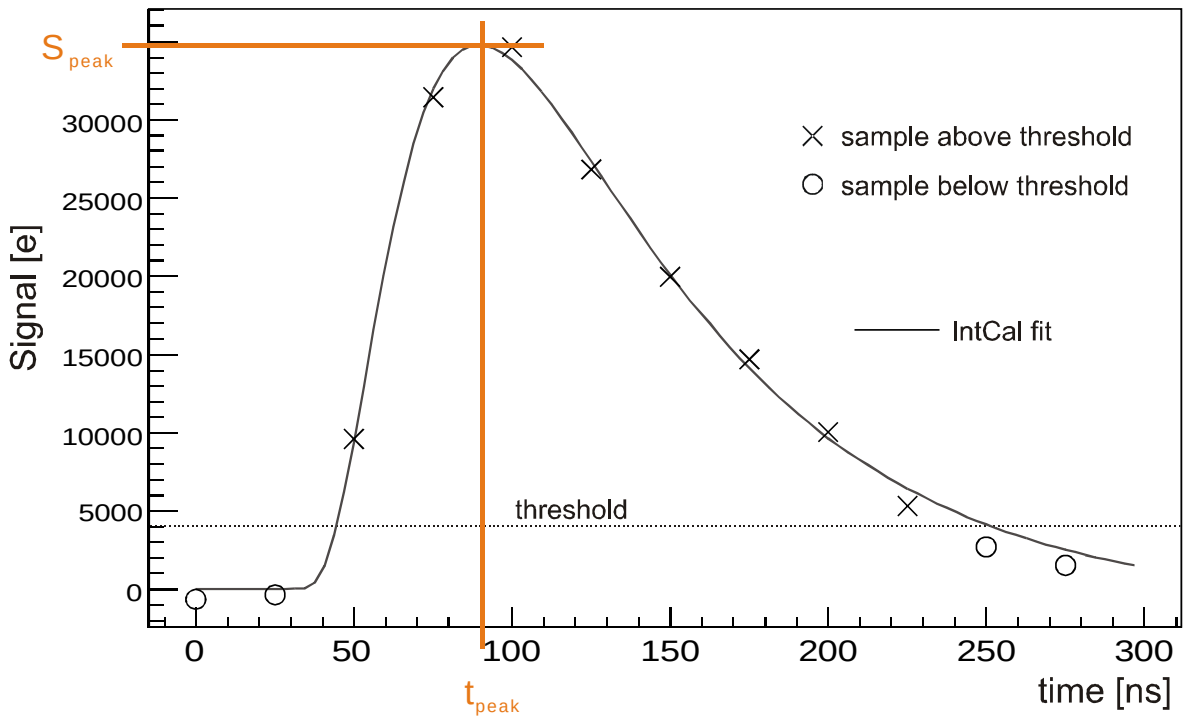
APV25 – Hit Time Reconstruction

- Possibility of recording **multiple samples** (**x**) along shaped waveform (feature of APV25)

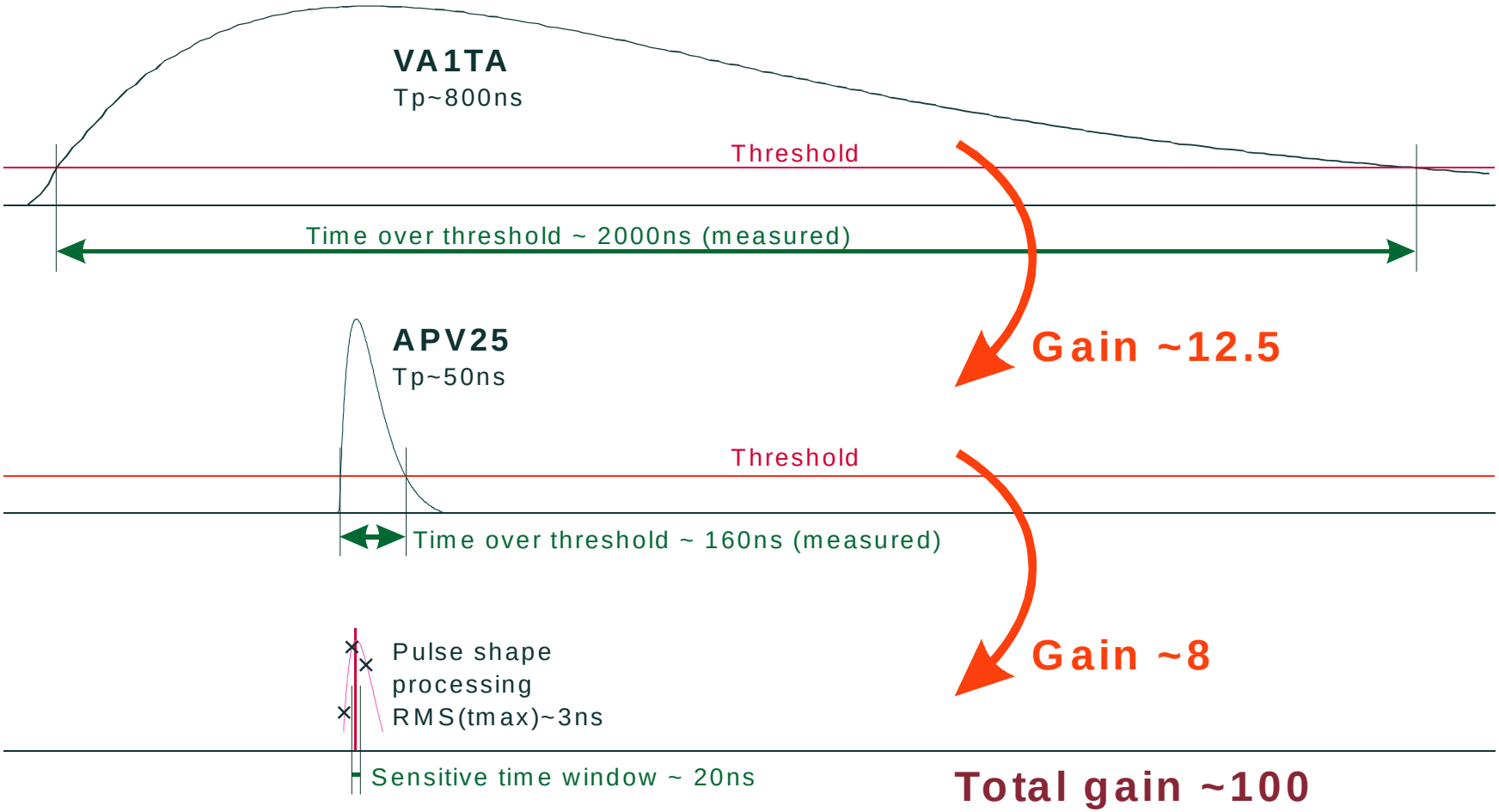
- Reconstruction of **peak time** (and amplitude) by waveform fit

- Will be used to **remove off-time background** hits

Measurement

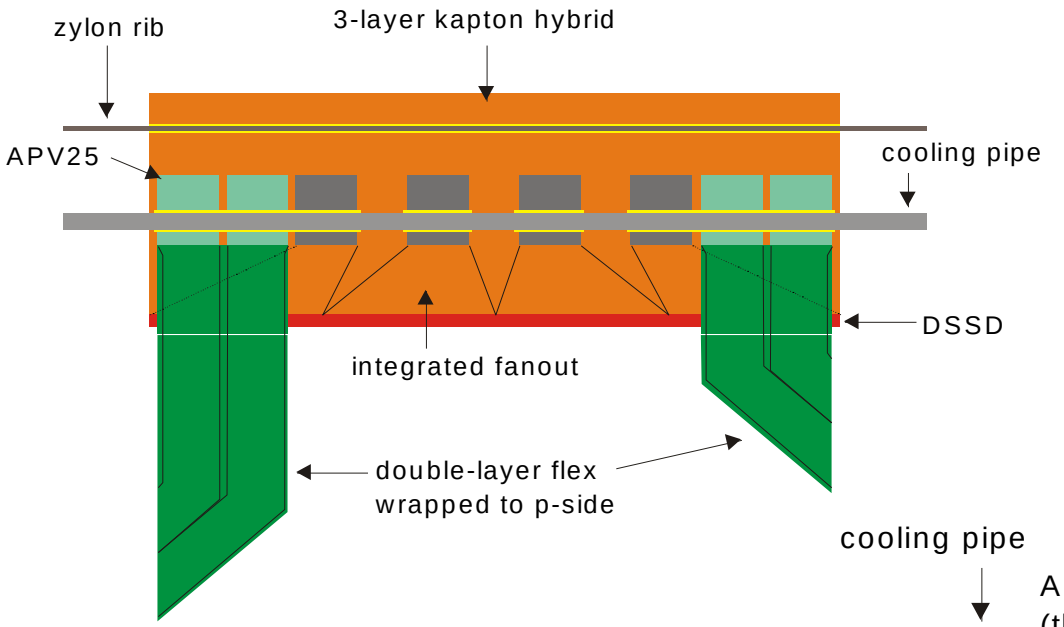


Occupancy Reduction

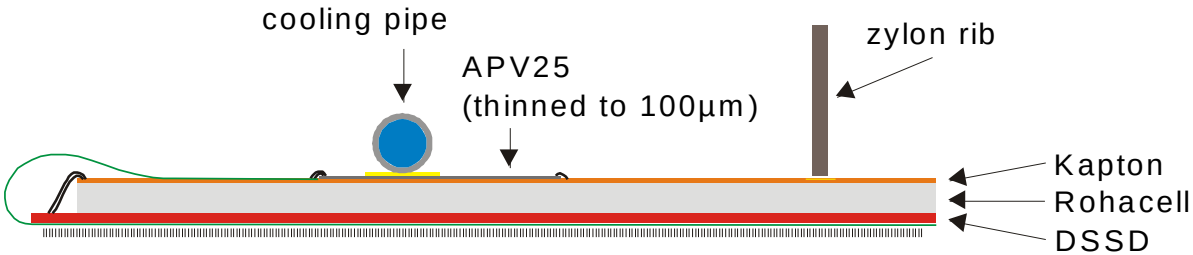


Origami – Chip-on-Sensor Concept

- **Chip-on-sensor** concept for **double-sided readout**
- **Flex fan-out** pieces **wrapped** to opposite side (hence "Origami")
- All chips aligned on one side → **single cooling pipe**

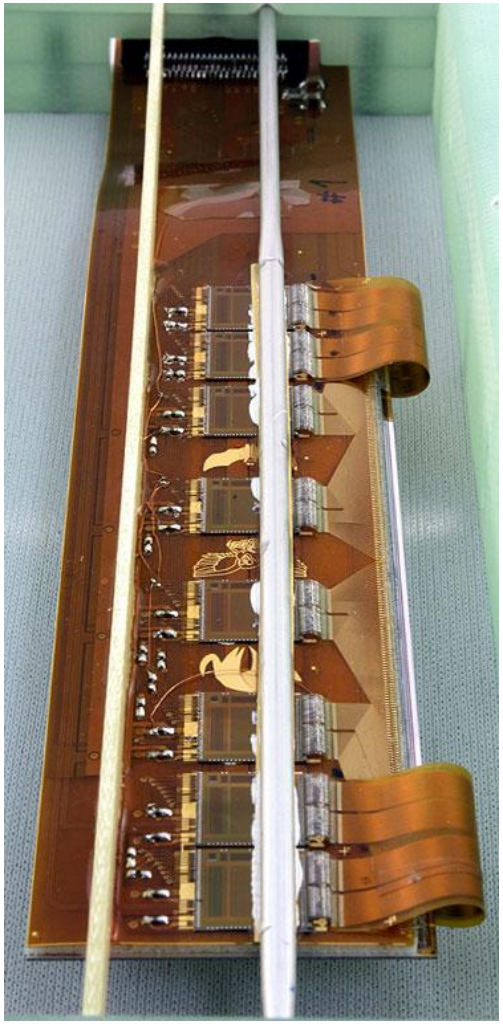


Side View (below)

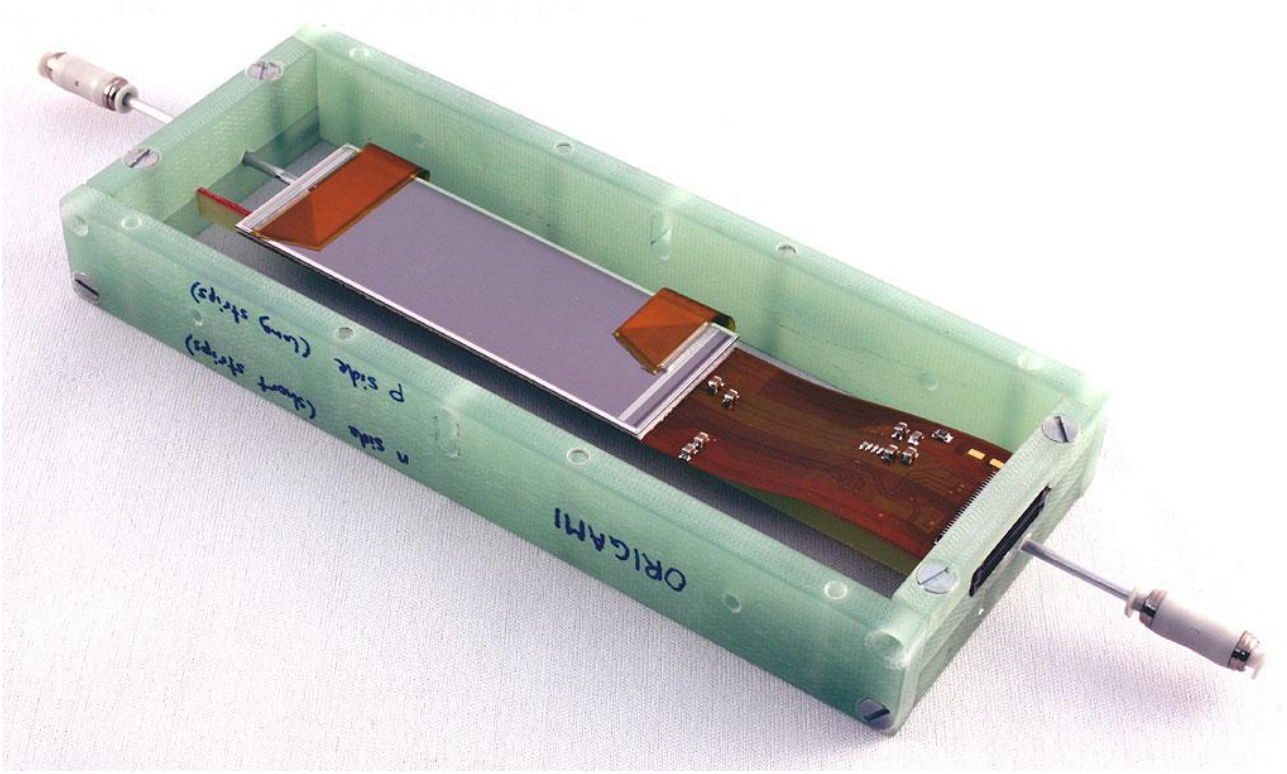


Prototype for 4" DSSD (later with 6" sensors)

First Origami Module (2009)

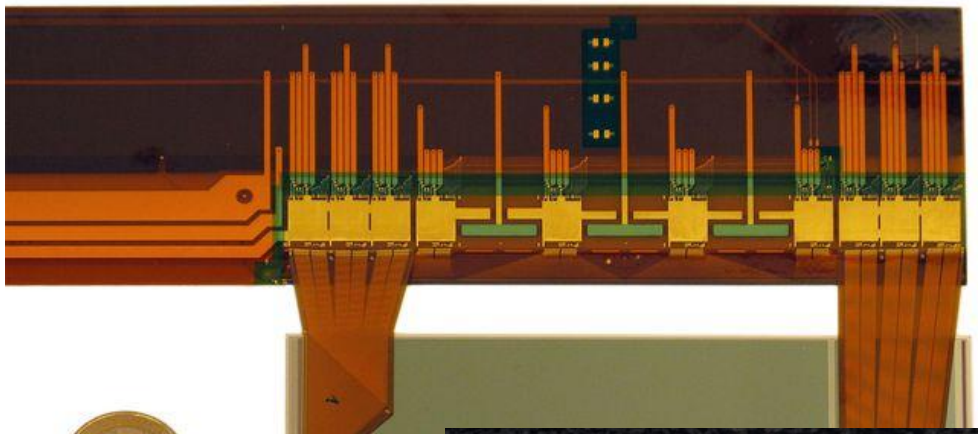


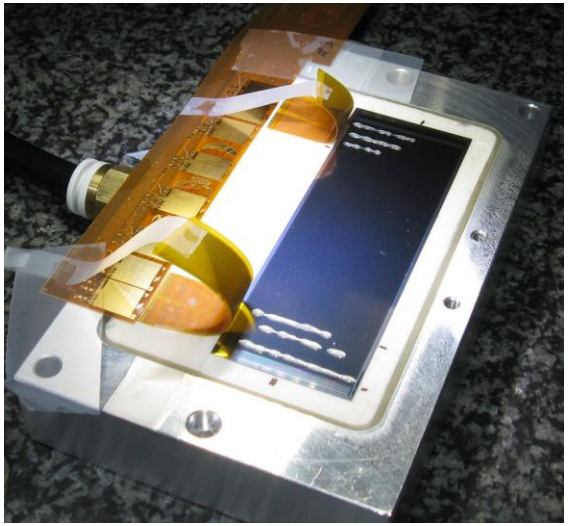
- Top and bottom side Origami concept (4” sensor)
- Prototype completed in August 2009
- Successfully evaluated in lab and beam tests
- Currently building module based on 6” sensor

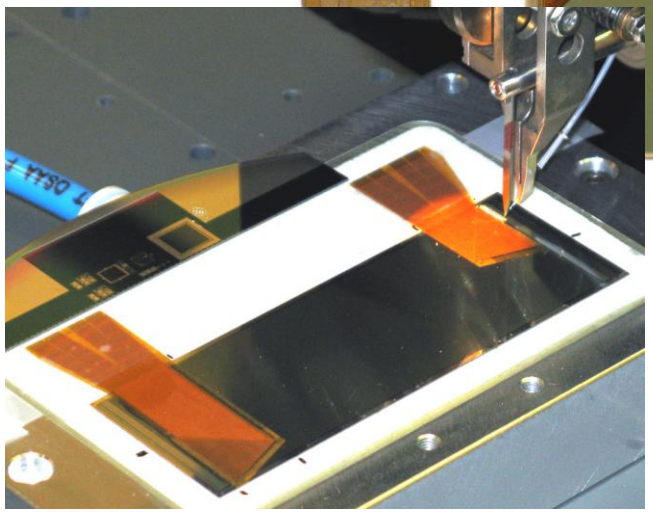


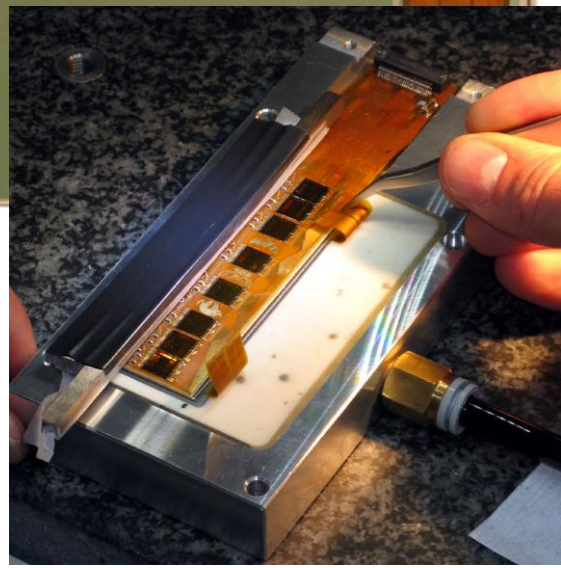
Second Origami Module (2010)

- Now using new 6 inch sensors
- Kapton PCB and pitch-adapters ordered by Japanese company
  - Currently under test in Vienna
- Followed by complicated assembly procedure



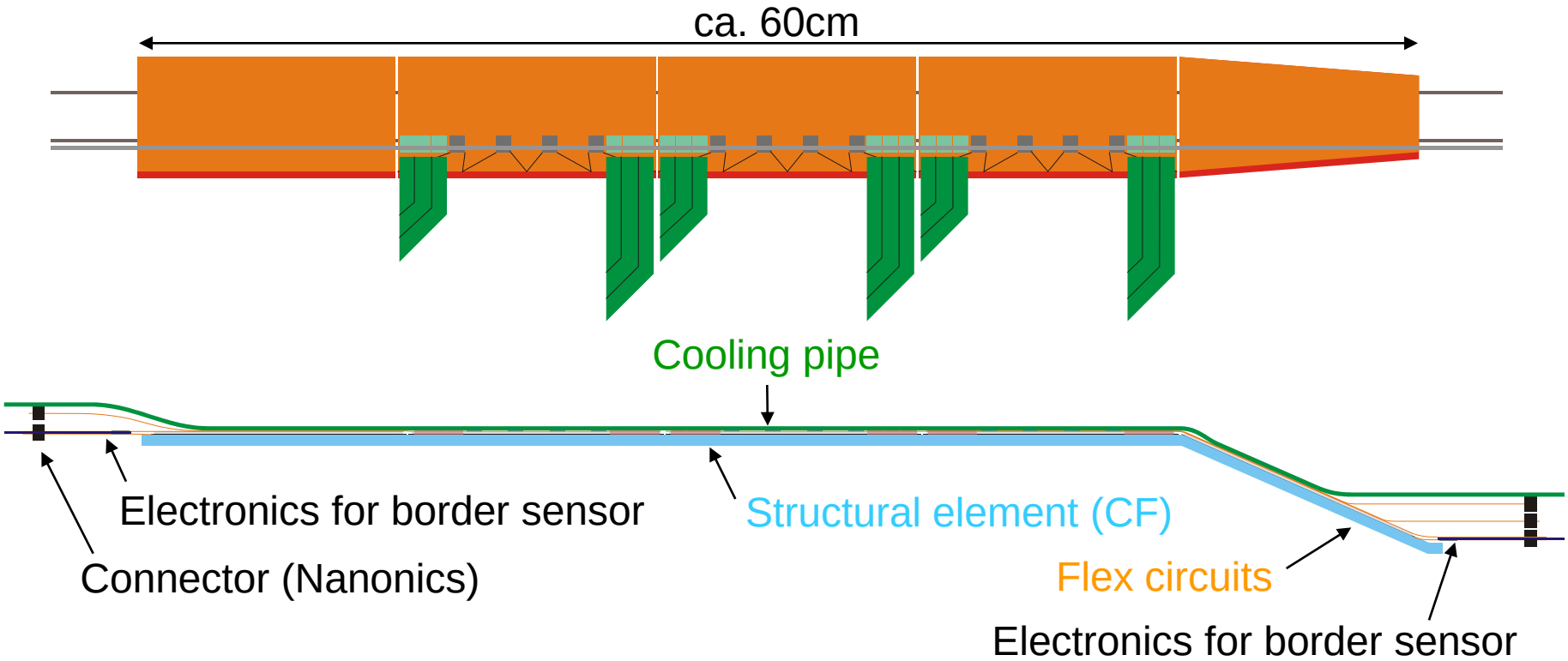




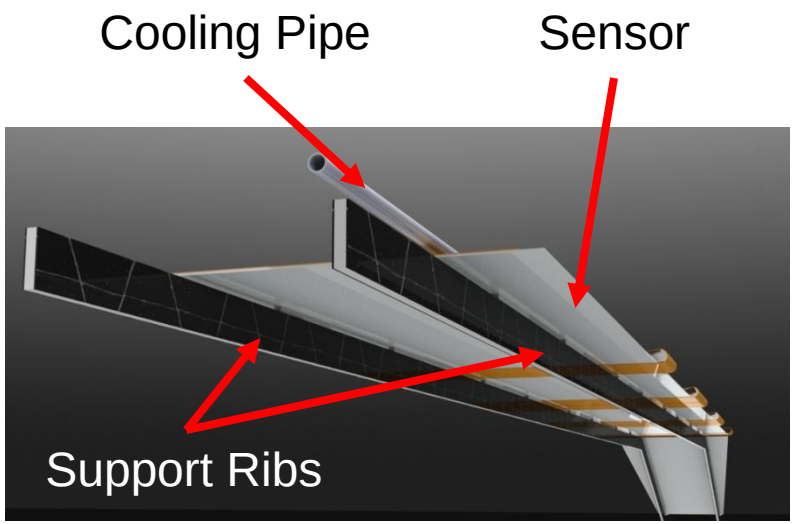


Sketch of the Outermost Ladder (Layer 6)

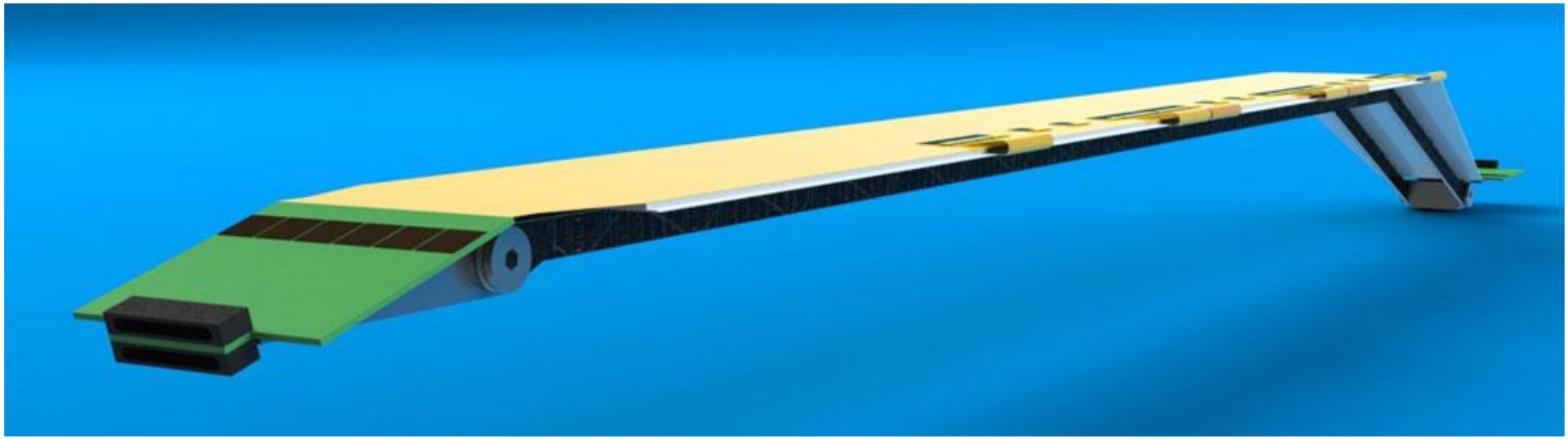
- Composed of 5 x 6” double-sided sensors
- Center sensors have Origami structure
- Border sensors are conventionally read out from sides

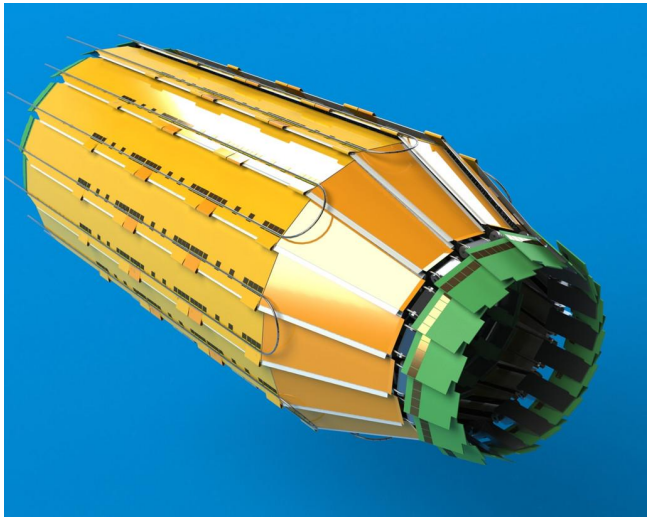


Ladder Mechanics (preliminary)



- Carried by ribs made of carbon fiber and Rohacell
- Averaged material budget: 0.58% X_0
- Cooling options under study
  - Conventional liquid cooling
  - CO_2 cooling

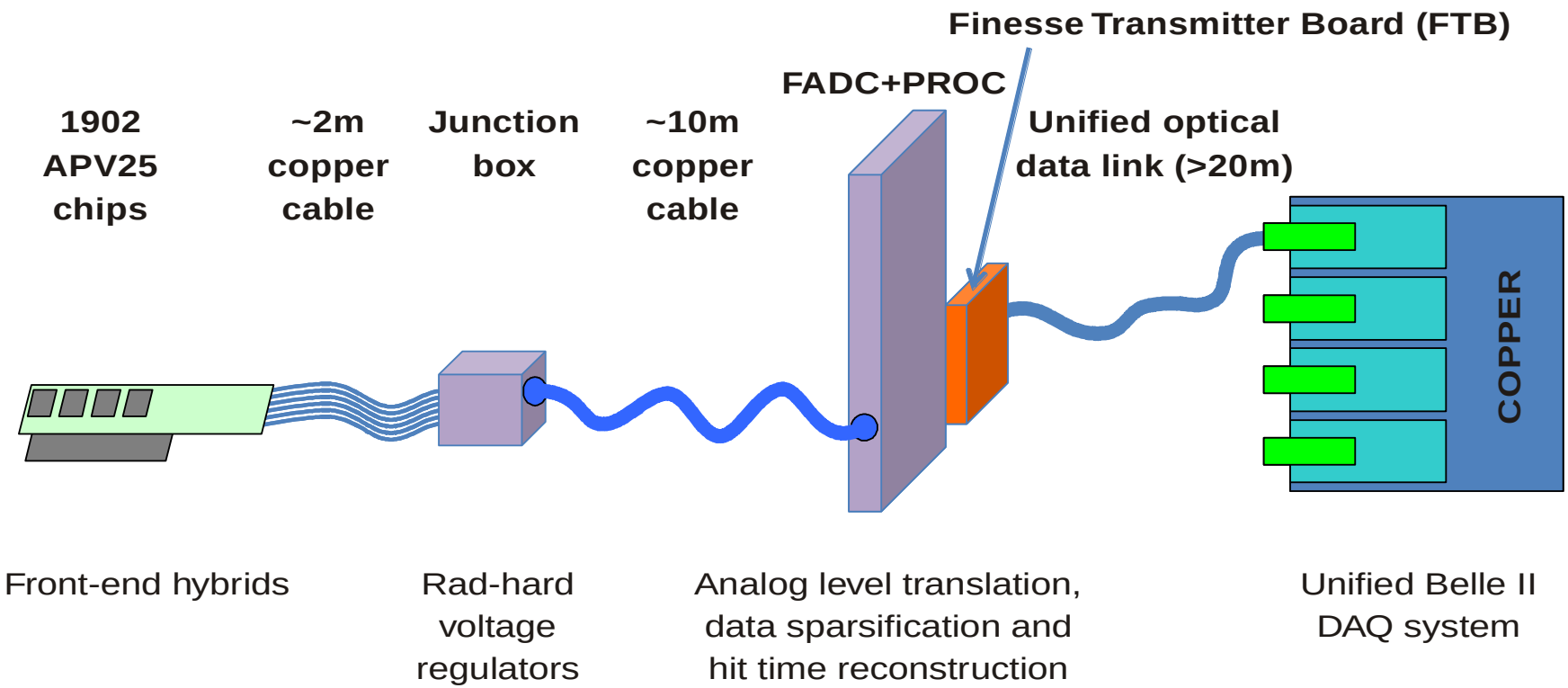




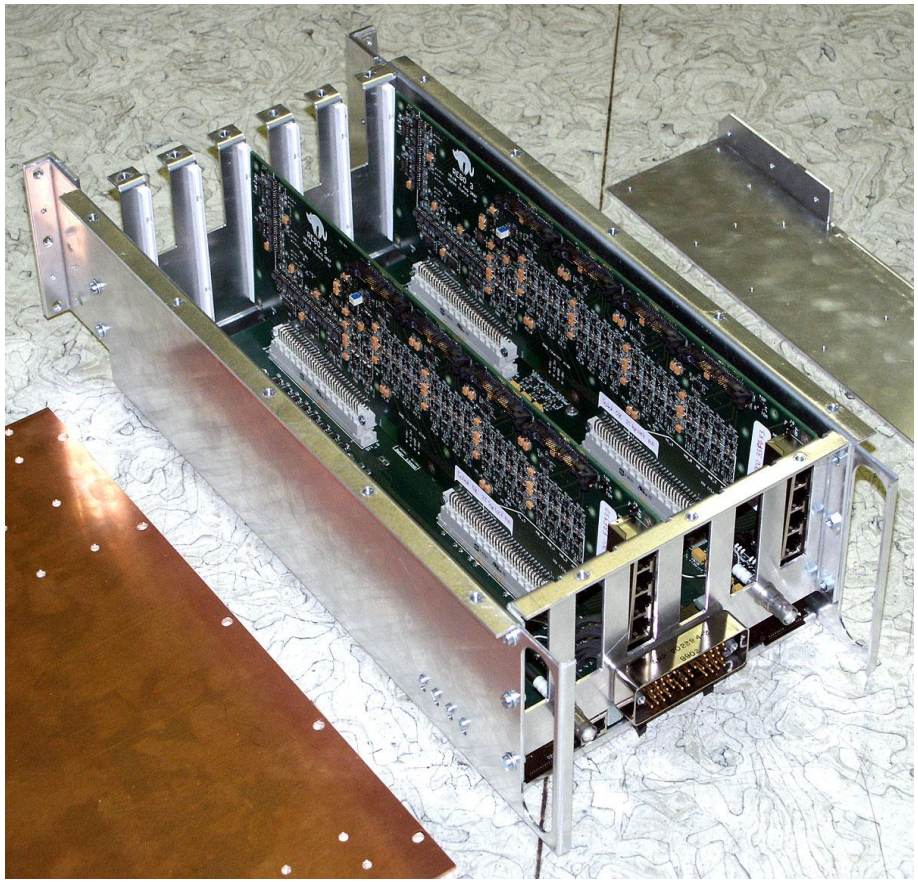
Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary

Readout System

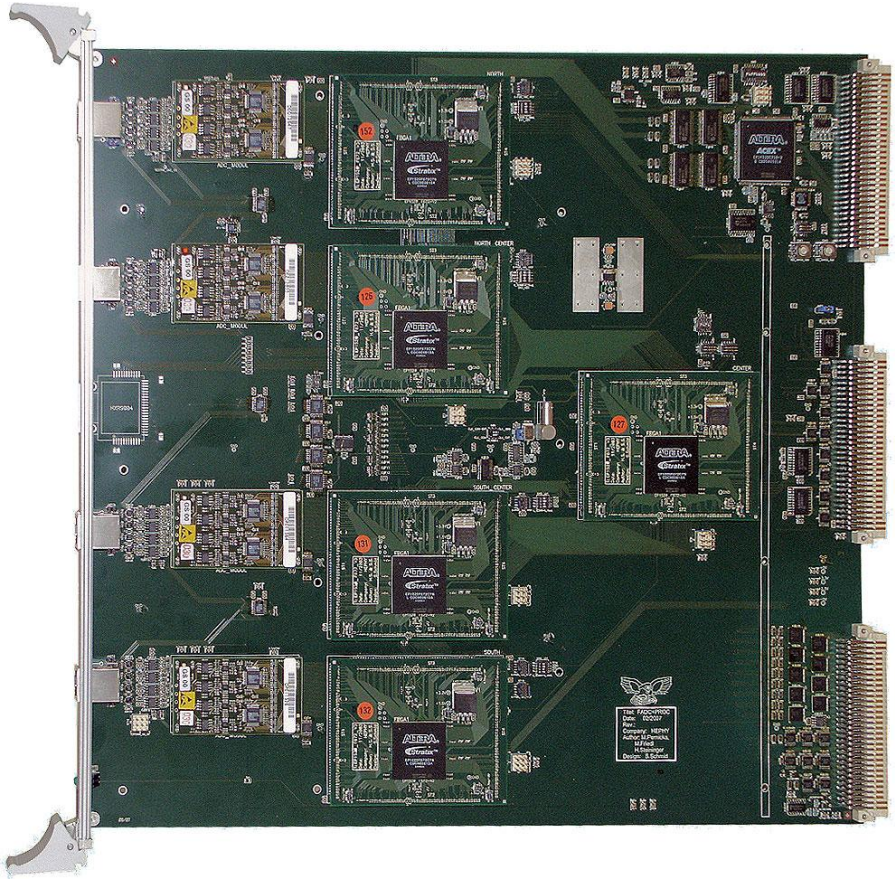
- Prototype **readout system exists**
- **Verified** in several **beam tests**
- Basis for future SVD system shown below



Prototype Readout System



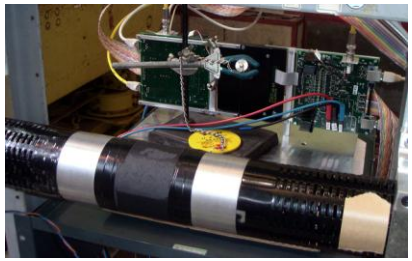
Repeater Box
Level translation, buffering



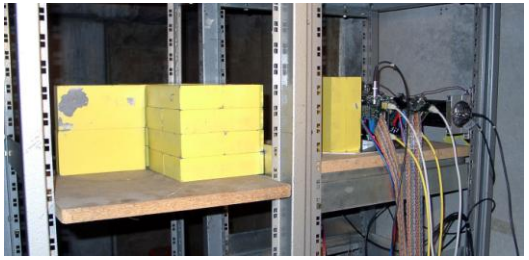
FADC+PROC (9U VME)
Digitization, zero-suppression,
hit time reconstruction

Beam Tests

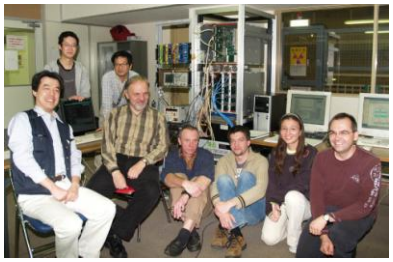
KEK (Apr 2005)



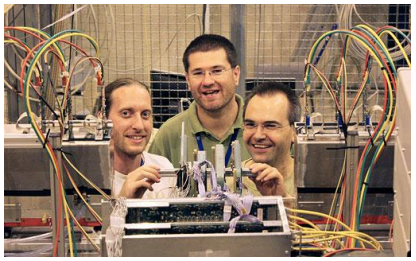
PSI (Aug 2005, Aug 2006)

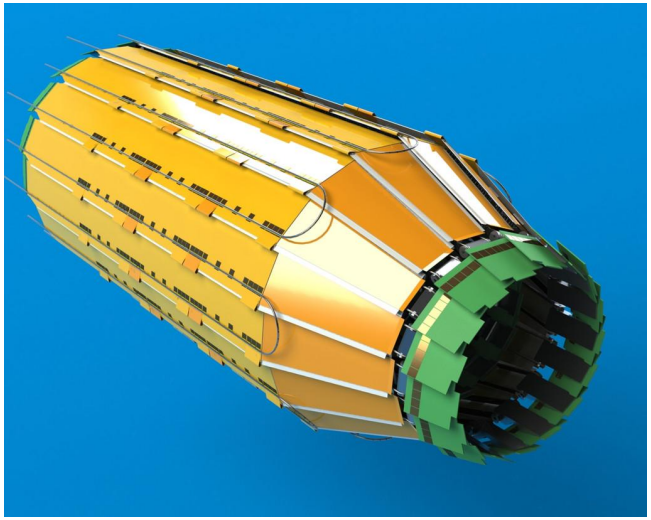


KEK (Nov 2007, Nov 2008)



CERN (June 2008, September 2009)

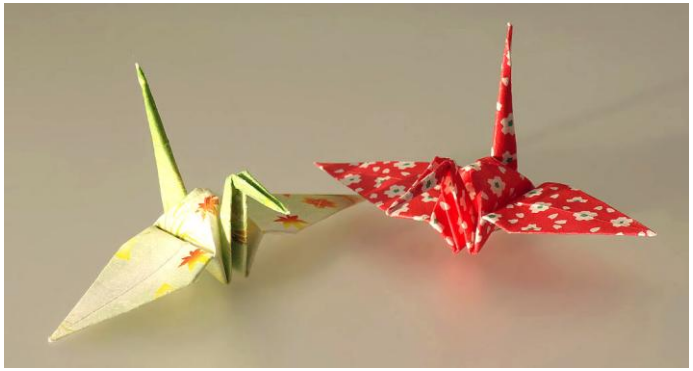


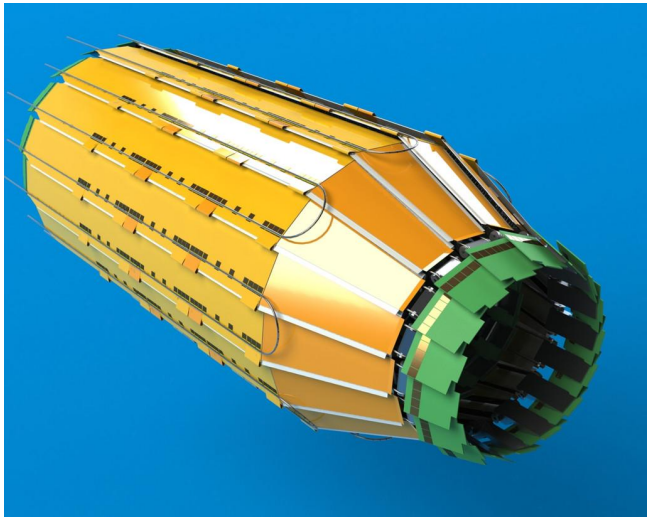


Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary

Summary

- **KEKB** is the **highest luminosity** machine in the world
- **Upgrade** of KEKB and Belle (2010-2014)
  - 40-fold increase in **luminosity**
  - Needs upgrades of all subdetectors
- New, enlarged **Silicon Vertex Detector**
  - **DEPFET** pixel double-layer
  - Four **strip** layers
- Strip Detector **R&D**
  - **New 6" Double Sided Strip Detectors** by HPK
  - **Origami** chip-on-sensor concept for low-mass DSSD readout
  - Readout with **hit time reconstruction** for improved background tolerance (up to 100x occupancy reduction w.r.t. now)



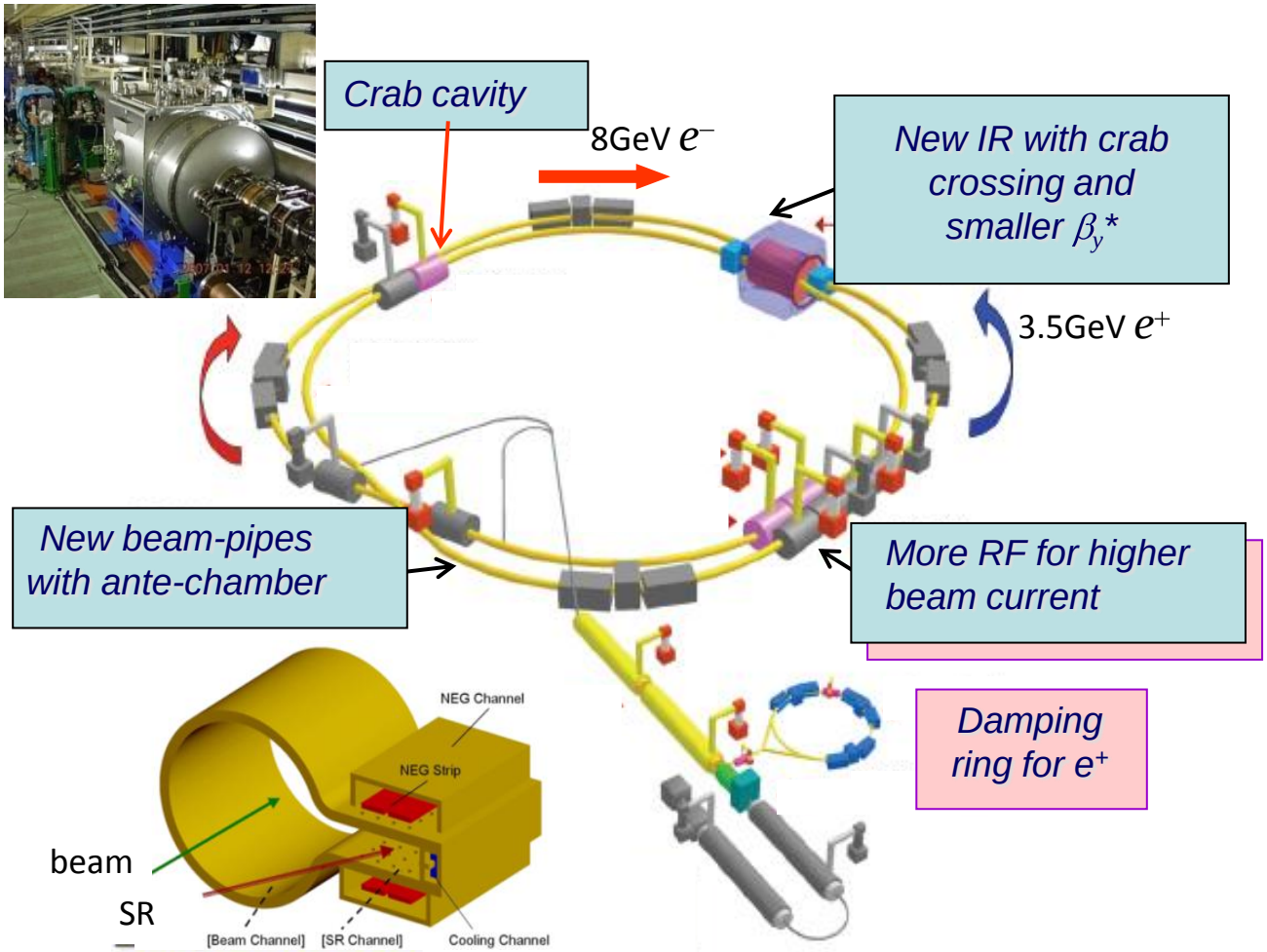


Backup Slides

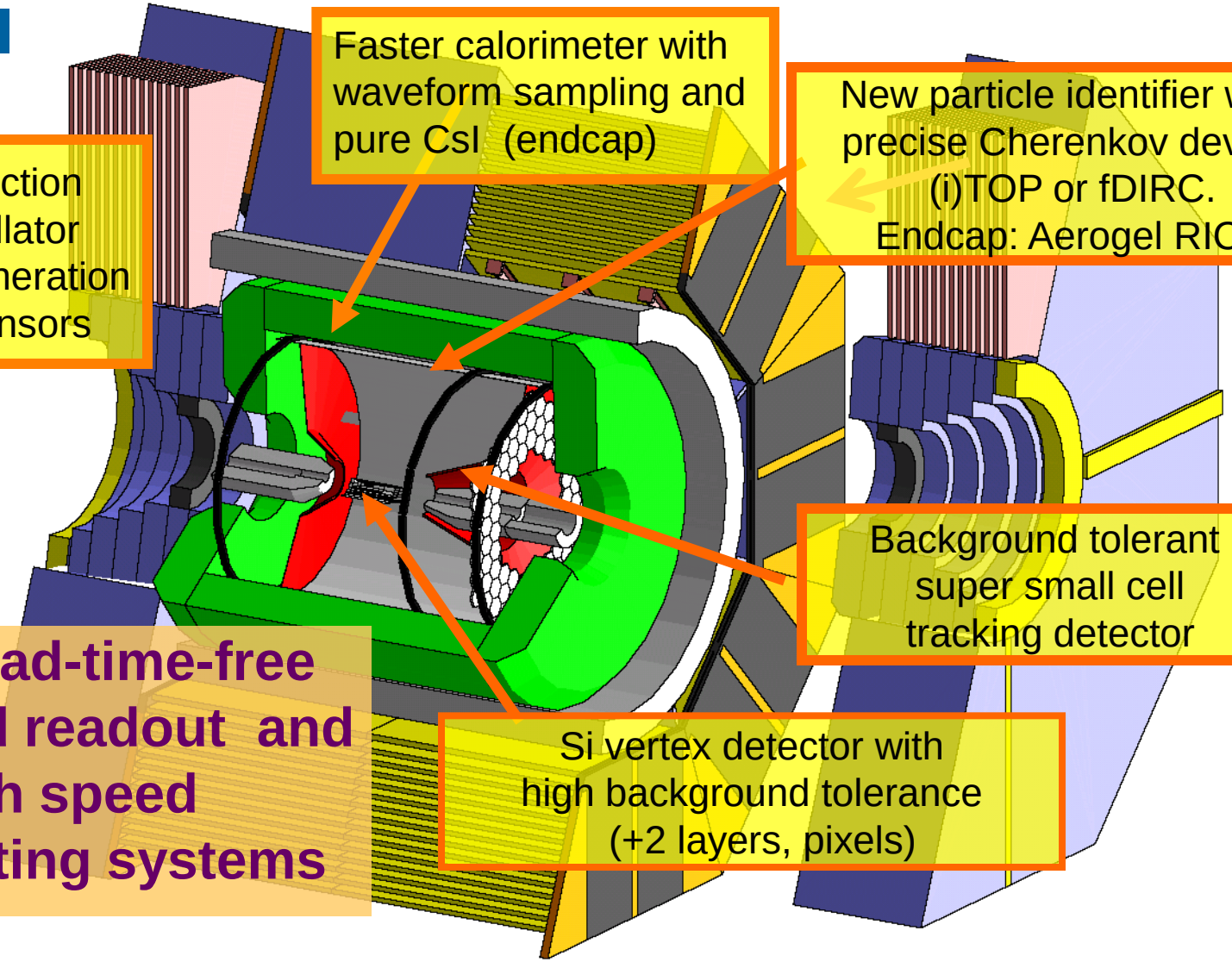
Beam Parameters

	KEKB Design	KEKB Achieved : with crab	SuperKEKB High-Current	SuperKEKB Nano-Beam
Energy (GeV) (LER/HER)	3.5/8.0	3.5/8.0	3.5/8.0	4.0/7.0
β_y^* (mm)	10/10	5.9/5.9	3/6	0.27/0.42
ε_x (nm)	18/18	18/24	24/18	3.2/2.4
σ_y(μm)	1.9	0.94	0.85/0.73	0.059
ξ_y	0.052	0.129/0.090	0.3/0.51	0.09/0.09
σ_z (mm)	4	~ 6	5/3	6/5
I_{beam} (A)	2.6/1.1	1.64/1.19	9.4/4.1	3.6/2.6
$N_{bunches}$	5000	1584	5000	2503
Luminosity (10^{34} cm^{-2} s^{-1})	1	2.11	53	80

KEKB accelerator upgrade



Belle-II



Faster calorimeter with waveform sampling and pure CsI (endcap)

New particle identifier with precise Cherenkov device: (i)TOP or fDIRC. Endcap: Aerogel RICH

KL/μ detection with scintillator and next generation photon sensors

Background tolerant super small cell tracking detector

New dead-time-free pipelined readout and high speed computing systems

Si vertex detector with high background tolerance (+2 layers, pixels)

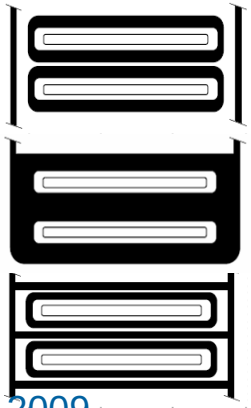
Micron Wafer Layout

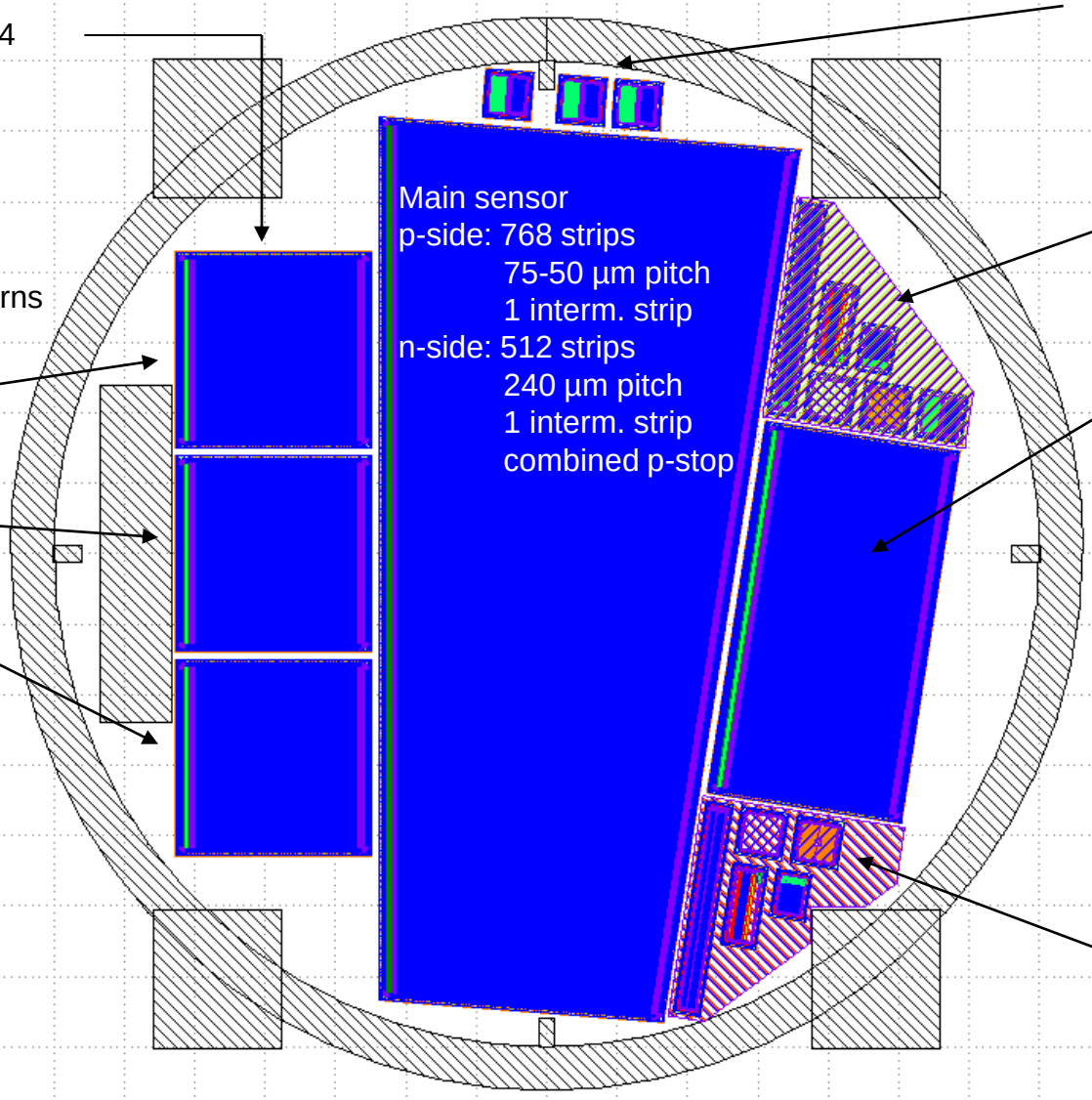
Quadratic baby sensors 2,3,4
p-side: 512 strips
50 µm pitch
1 interm. strip
n-side: 256 strips
100 µm pitch
0 interm. strip
different p-stop patterns

1) atoll p-stop
varying distance from strip

2) conventional p-stop
varying width

3) combined p-stop
varying distance from strip





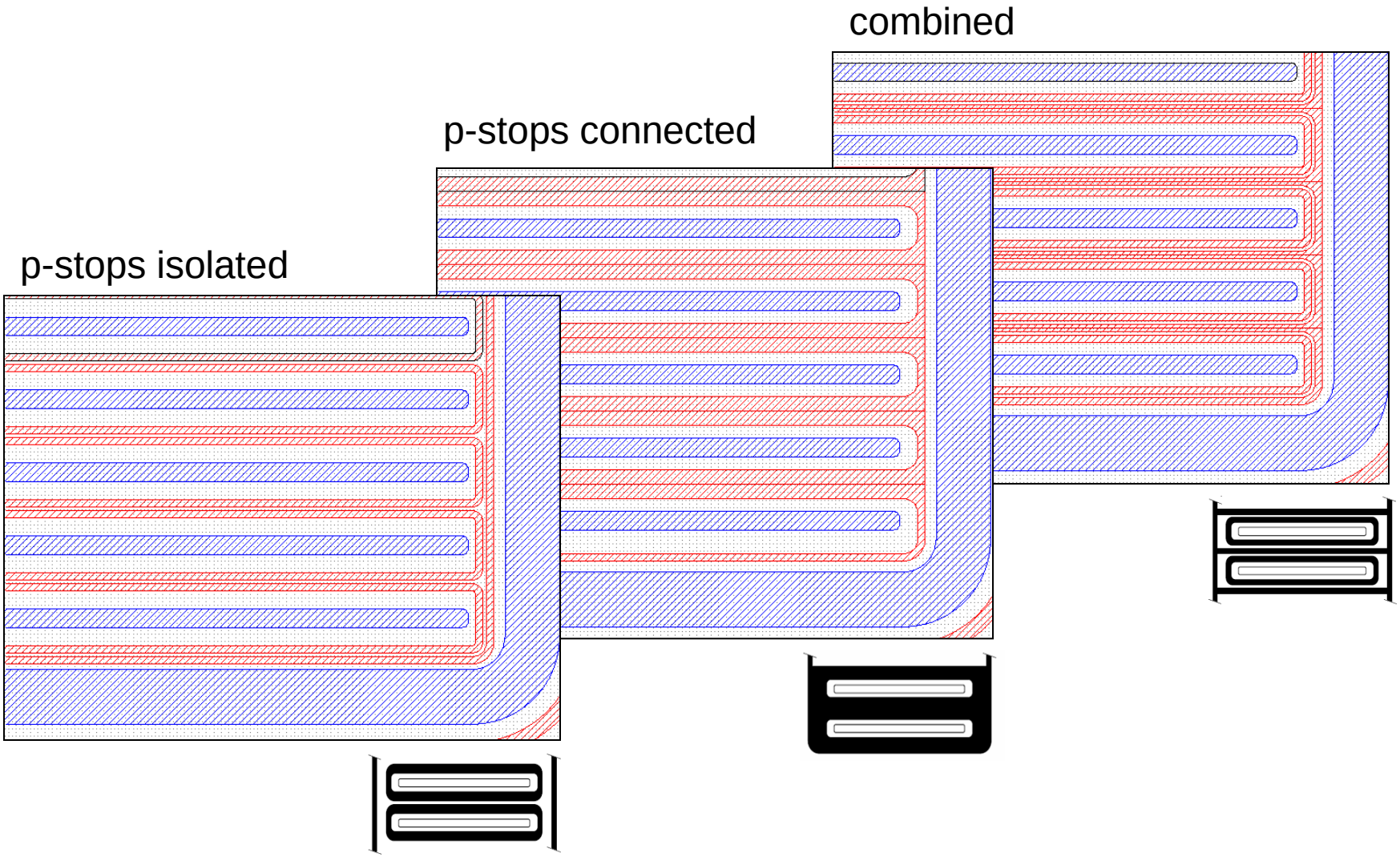
3 different GCDs
for the n-side

Teststructures
for p-side

Baby sensor 1
p-side: 512 strips
50 µm pitch
1 interm. strip
n-side: 512 strips
100 µm pitch
1 interm. strip
atoll p-stop

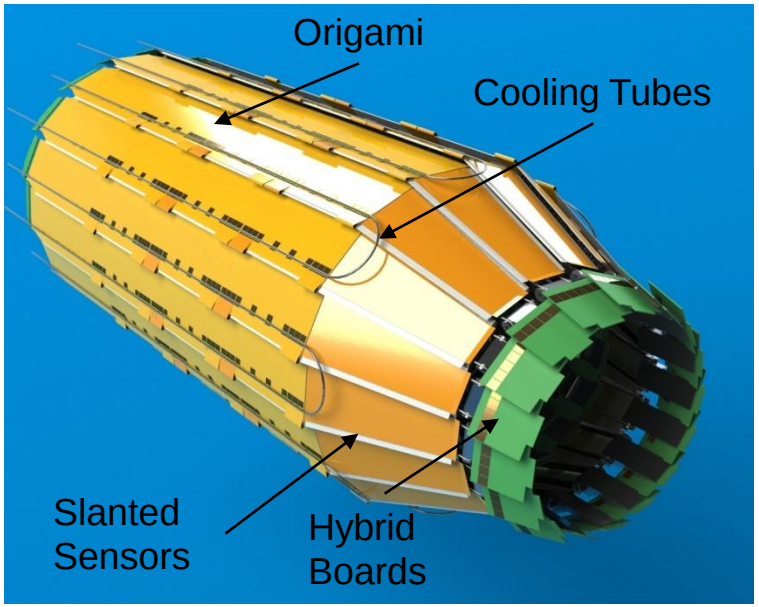
Teststructures
for n-side
(no GCD)

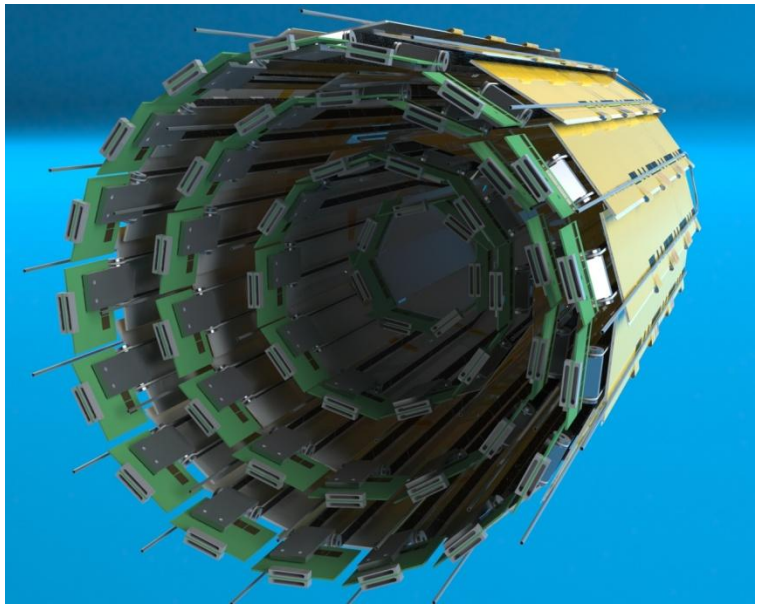
Micron: p-stop layout



Current Barrel Layout

Layer	Sensors/ Ladder	Origamis/ Ladder	Ladders	Length [mm]	Radius [mm]	Slant Angle [°]
3	2	0	7/8	262	38	0
4	3	1	10	390	80	11.9
5	4	2	14	515	115	17.2
6	5	3	17	645	140	21.1





Comparison VA1TA – APV25

VA1TA (SVD)

- Commercial product (IDEAS)
- Tp = 800ns (300 ns – 1000 ns)
- no pipeline
- <10 MHz readout
- 20 Mrad radiation tolerance
- noise: ENC = 180 e + 7.5 e/pF
- time over threshold: ~2000 ns
- single sample per trigger

APV25 (Belle-II SVD)

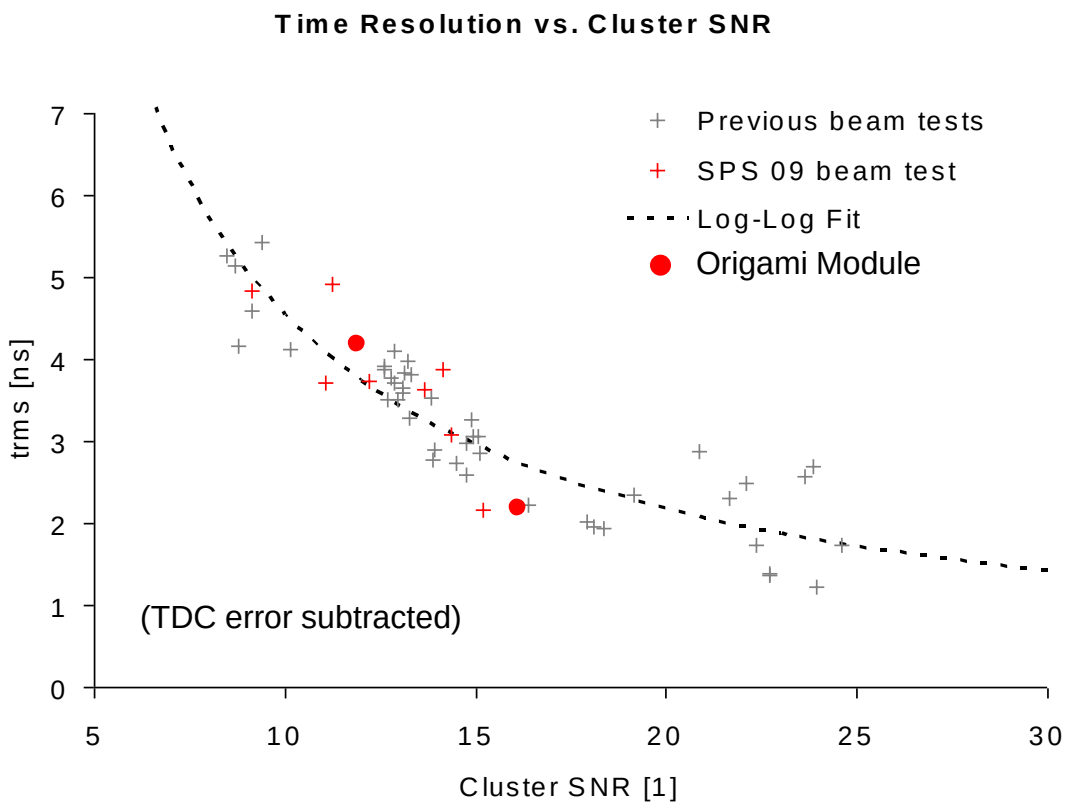
- Developed for CMS by IC London and RAL
- Tp = 50 ns (30 ns – 200 ns)
- 192 cells analog pipeline
- 40 MHz readout
- >100 Mrad radiation tolerance
- noise: ENC = 250 e + 36 e/pF
- time over threshold: ~160 ns
- multiple samples per trigger possible (Multi-Peak-Mode)

Measured Hit Time Precision

- Results achieved in **beam tests** with several different types of Belle DSSD prototype modules (covering a broad range of SNR)

- **2...3 ns RMS** accuracy at typical cluster SNR (15...25)

- Working on implementation in **FPGA** (using lookup tables) – simulation successful



Origami Material Budget

- X_0 comparison between conventional and chip-on-sensor (4” sensors):

Conventional (double layer kapton)

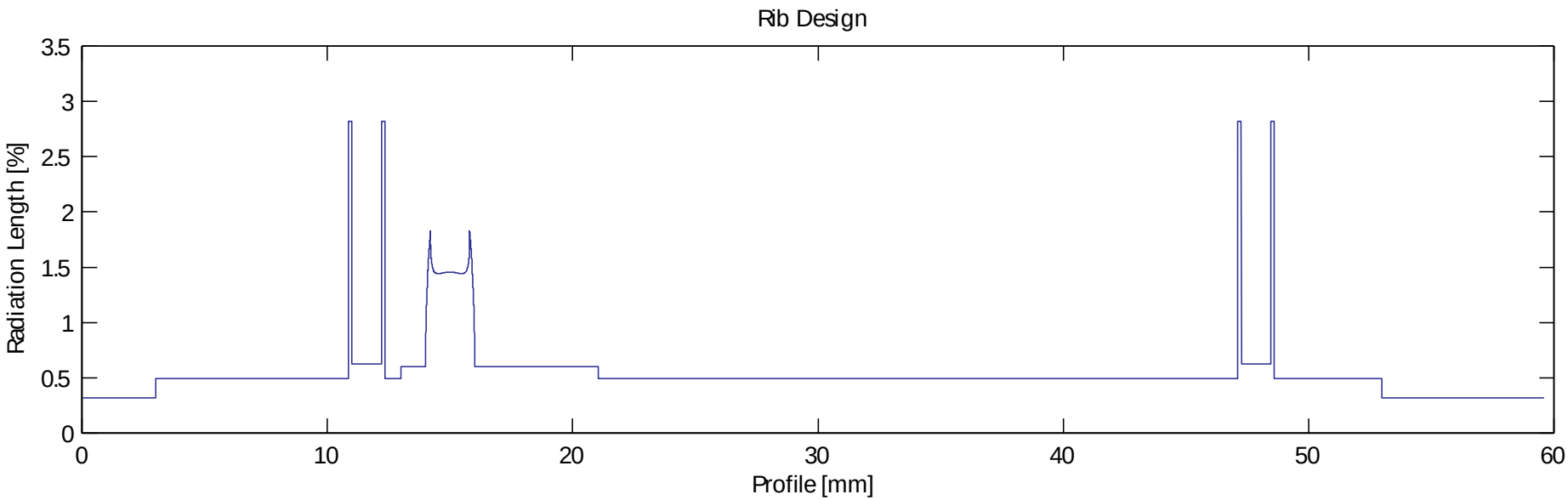
Layer	Material	X0 [mm]	Thickness [mm]	Percentage	Area coverage	Averaged Percentage
Sensor	Silicon	93.7	0.3	0.32%	100.0%	0.320%
Fanout	Polyimide (2 layer of 50um each)	300.0	0.1	0.03%	96.3%	0.032%
	Copper (10um)	14.0	0.01	0.07%	50.0%	0.036%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	50.0%	0.005%
	Gold (top: 0.8um)	3.4	0.0008	0.02%	50.0%	0.012%
Ribs	Zylon (0.5mm wide)	300.0	5	1.67%	3.7%	0.062%
Glue	Araldite 2011 / Double sided tape	335.0	0.05	0.01%	96.3%	0.014%
					Total	**0.480%**

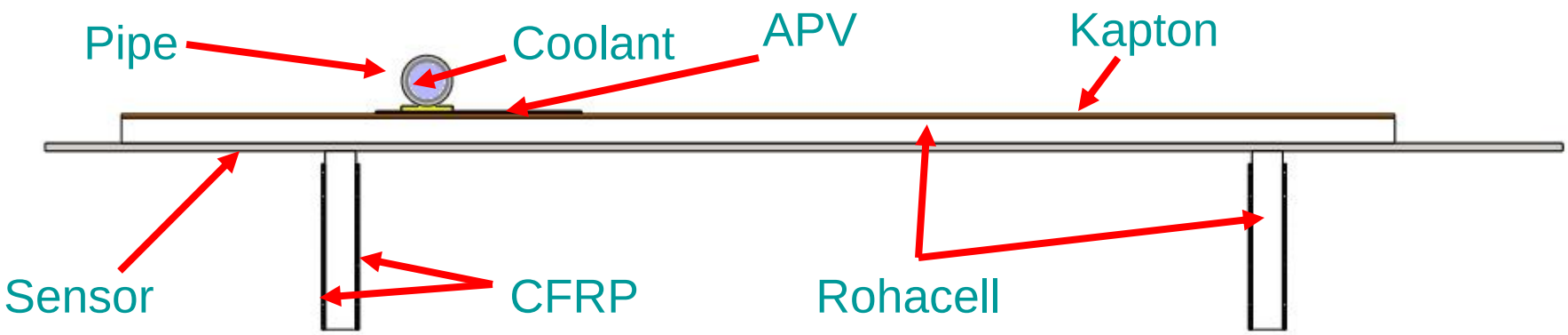
DSSD Chip-on-Sensor (4-layer kapton)

Layer	Material	X0 [mm]	Thickness [mm]	Percentage	Area coverage	Averaged Percentage
Sensor	Silicon	93.7	0.3	0.32%	100.0%	0.320%
Isolation	Rohacell (Degussa)	5450.0	1	0.02%	96.3%	0.018%
Hybrid	Polyimide (4 layers of 50um each)	300.0	0.2	0.07%	96.3%	0.064%
	Copper (4 layers of 5um each)	14.0	0.02	0.14%	64.7%	0.092%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	64.7%	0.006%
	Flash Gold (top: 0.4um)	3.4	0.0004	0.01%	64.7%	0.008%
Flexes	Polyimide (1 layer of 25um)	300.0	0.025	0.01%	56.3%	0.005%
	Copper (1 layer of 5um)	14.0	0.005	0.04%	28.1%	0.010%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	28.1%	0.003%
	Flash Gold (top: 0.4um)	3.4	0.0004	0.01%	28.1%	0.003%
8 * APV25	Silicon	93.7	0.1	0.11%	21.4%	0.023%
SMDs	SMD	50.0	0.4	0.80%	0.8%	0.007%
Sil-Pad	Sil-Pad 800 (Bergquist)	200.0	0.127	0.06%	11%	0.007%
Pipe	Aluminum (D=2.0mm, wall=0.2mm)	89.0	0.56	0.63%	7%	0.047%
Rib	Zylon (0.5mm wide)	300.0	5	1.67%	1.9%	0.031%
Glue	Araldite 2011	335.0	0.2	0.06%	50%	0.030%
Cooling	Water	360.5	1.26	0.35%	13%	0.047%
					Total	**0.719%**

- **+50%** increase in **material**, but also **huge** improvement in **SNR**
- **Trade-off** between material budget and SNR
- According to simulation, additional material is prohibitive in 2 innermost layers, but **no problem for layers 3-5** → OK with layout

Maximum Radiation Length Distribution





Cooling Boundary Conditions

- Power dissipation/APV: 0.4 W
- 1 Origami sensor features 10 APVs

	Origamis/ Ladder	Ladders	APVs Origami	APVs Hybrid
Layer 6	3	17	510	340
Layer 5	2	14	280	280
Layer 4	1	10	100	200
Layer 3	0	8	0	192

- Total Origami power dissipation: 356 W
- 404 W dissipated at the hybridboards
- Total SVD power dissipation: 760 W