The Silicon Vertex Detector of the Belle II Experiment

Thomas Bergauer (HEPHY Vienna)
Introduction
Belle II: The Future
Double Sided Sensors
SVD-II Components
Readout System
Summary
KEKB and Belle @ KEK

- **Asymmetric** machine: 8 GeV $e^-$ on 3.5 GeV $e^+$
- Center of mass **energy**: $Y(4S)$ (10.58 GeV)
- **High intensity** beams (1.6 A & 1.3 A)
- Integrated luminosity 1 ab$^{-1}$ recorded by end of 2009

About 60km northeast of Tokyo

~1 km in diameter

Mt. Tsukuba

KEKB

Belle

Linac
The Silicon Vertex Detector
of the Belle II Experiment


µ / K

14/15 lyr. RPC+Fe

CsI(Tl)

Si vertex detector

4 lyr. DSSD

SC solenoid 1.5 T

8 GeV e−

3.5 GeV e+ + Aerogel Cherenkov counter

n=1.015~1.030

Central Drift Chamber small cell +He/C

TOF counter


T. Bergauer
The Present SVD – Overview

- **4 layers** (6/12/18/18 ladders), $r = 2.0 \ldots 8.8$ cm
- **17°…150°** polar angle coverage
- **246 double sided** silicon detectors (DSSDs), $0.5 \text{ m}^2$ overall active area
- **VA1TA** readout chip (Viking variant; 800ns shaping time)
- **110592** channels in total
Introduction

Belle II: The Future

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KEKB/Belle upgrade (2010–2014)

- Aim: super-high luminosity $\sim 8 \times 10^{35} \text{cm}^{-2}\text{s}^{-1} \rightarrow 1 \times 10^{10} \text{B} \bar{\text{B}} / \text{year}$
- LoI published in 2004; TDR was written in spring this year and is presently under review
- Refurbishment of accelerator and detector required

http://belle2.kek.jp
Belle II SVD Upgrade (2010–2014)

- Ultimately **40-fold increase in luminosity** (~$8 \times 10^{35}$ cm$^{-2}$s$^{-1}$)
- Present SVD limitations are
  - **occupancy** (currently ~10% in innermost layer) → need faster shaping
  - **dead time** (currently ~3%) → need faster readout and pipeline
- Needs Detector with
  - high **background tolerance**
  - **pipelined** readout
  - **robust tracking**
  - **low material budget** in active volume (low energy machine)
- Ultimately **40-fold increase in luminosity** (~$8 \times 10^{35}$ cm$^{-2}$s$^{-1}$)
- Present SVD limitations are
  - **occupancy** (currently ~10% in innermost layer) → need faster shaping
  - **dead time** (currently ~3%) → need faster readout and pipeline
- Needs Detector with
  - high **background tolerance**
  - **pipelined** readout
  - **robust tracking**
  - **low material budget** in active volume (low energy machine)

Current SVD is not suitable for Belle II

**10 June 2010 T. Bergauer**
The Silicon Vertex Detector
of the Belle II Experiment

Present SVD Layout (until 2010)

- 4 straight layers of 4" double-sided silicon detectors (DSSDs)
- Outer radius of r~8.8 cm
- Up to 3 sensors are ganged and read out by one hybrid located outside of acceptance
• Geometry optimization is underway
• New central pixel double-layer using **DEPFET**
• Strip layers extend to *r*~14 cm
• Every sensor is **read out individually** (no ganging) to maintain good S/N
  → chip-on-sensor concept
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Vendors for 6” DSSD

• Aim is to use double sided silicon detectors with AC-coupled readout and poly-silicon resistor biasing from 6 inch wafer.

• Hamamatsu decided in the past to abandon the production of double sided sensors.

• Thus, negotiations with Canberra, SINTEF and Micron started.

• Finally HPK could be convinced to restart DSSD production on 6” wafers.

• 6” prototypes ordered from
  – Hamamatsu (rectangular): First batch delivered in April
  – Micron (trapezoidal): First batch in July.
The Silicon Vertex Detector of the Belle II Experiment

SVD Layout

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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</tr>
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<tbody>
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<td>6</td>
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<td>0</td>
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<td>17</td>
<td>850</td>
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<td>0</td>
<td>20</td>
<td>10</td>
<td>300</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>16</td>
<td>0</td>
<td>0</td>
<td>192</td>
</tr>
<tr>
<td>Sum:</td>
<td>49</td>
<td>16</td>
<td>130</td>
<td>41</td>
<td>1902</td>
</tr>
</tbody>
</table>

Thomas Bergauer (HEPHY Vienna)

First batch from HPK

- First 20 pieces of 6” sensors have been delivered in April 2010
- Technical details:
  - Dimensions: 59.6 x 124.88 mm
  - p-side:
    - Readout pitch: 75 µm
    - 768 strips
  - n-side:
    - Readout pitch: 240 µm
    - 512 readout strips n-side
    - P-stop scheme

10 June 2010

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First Batch of 6” DSSD from HPK

• Electrical Characterization
  – IV, CV
  – Stripscan (p- and n-side)
  – Longterm stability vs. temperature and humidity
  – Inter-strip resistance and capacitance currently under investigation

• Pull-tests to show bondability ok
Trapezoidal Sensors (Micron)

- Full wafer designed using self-developed framework
- Including test structures and mini sensors to test different p-stop designs
- Delivery due July 2010

Sensor “programming language”

// Sensor
extern SensorPitch=50;
extern SensorSizeX=100000;
extern SensorSizeY=100000;
extern SensorCutMargin=100;
extern SensorGuardSpacing=50;
extern SensorGuardBiasSpacing=100;
extern SensorBiasStripSpacing=50;

// GuardRing
extern GuardNRings=10;
extern GuardWidth=100;
extern GuardCornerRadius=30;
extern GuardCornerPoints=20;

// BiasRing
extern BiasWidth=100;
extern BiasCornerRadius=30;
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APV25 Readout Chip

- Developed for **CMS** (LHC) by IC London and RAL (70k chips installed)
- 0.25 µm CMOS process (>100 MRad tolerant)
- **40 MHz clock** (adjustable), 128 channels
- **192 cell analog pipeline** → no dead time
- **50 ns shaping time** → low occupancy
- **Noise**: 250 e + 36 e/pF → must minimize capacitive load!!!
- **Multi-peak mode** (read out several samples along shaping curve)
- **Thinning** to 100µm successful
APV25 – Hit Time Reconstruction

- Possibility of recording **multiple samples** (x) along shaped waveform (feature of APV25)

- Reconstruction of **peak time** (and amplitude) by waveform fit

- Will be used to **remove off-time background** hits
Occupancy Reduction

- VA1TA
  - $T_p \approx 800\text{ns}$
  - Time over threshold $\sim 2000\text{ns}$ (measured)

- APV25
  - $T_p \approx 50\text{ns}$
  - Time over threshold $\sim 160\text{ns}$ (measured)
  - Gain $\sim 12.5$
  - Gain $\sim 8$
  - Total gain $\sim 100$

- Pulse shape processing
  - RMS ($t_{\text{max}}$) $\sim 3\text{ns}$

- Sensitive time window $\sim 20\text{ns}$
Origami – Chip-on-Sensor Concept

- **Chip-on-sensor** concept for **double-sided readout**
- **Flex fan-out** pieces **wrapped** to opposite side (hence “Origami“)
- All chips aligned on one side → **single cooling pipe**

Prototype for 4” DSSD (later with 6” sensors)
First Origami Module (2009)

- Top and bottom side Origami concept (4” sensor)
- Prototype completed in August 2009
- Successfully evaluated in lab and beam tests
- Currently building module based on 6” sensor
Second Origami Module (2010)

- Now using new 6 inch sensors
- Kapton PCB and pitch-adapters ordered by Japanese company
  - Currently under test in Vienna
- Followed by complicated assembly procedure
Sketch of the Outermost Ladder (Layer 6)

- Composed of 5 x 6” double-sided sensors
- Center sensors have Origami structure
- Border sensors are conventionally read out from sides
Ladder Mechanics (preliminary)

- Carried by ribs made of carbon fiber and Rohacell
- Averaged material budget: 0.58% $X_0$
- Cooling options under study
  - Conventional liquid cooling
  - $CO_2$ cooling
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Readout System

- Prototype **readout system exists**
- **Verified** in several **beam tests**
- Basis for future SVD system shown below

1902 APV25 chips

~2m copper cable

Junction box

~10m copper cable

FADC+PROC

Unified optical data link (>20m)

Finesse Transmitter Board (FTB)

Front-end hybrids

Rad-hard voltage regulators

Analog level translation, data sparsification and hit time reconstruction

Unified Belle II DAQ system
Prototype Readout System

Repeater Box
Level translation, buffering

FADC+PROC (9U VME)
Digitization, zero-suppression, hit time reconstruction
Beam Tests

KEK (Apr 2005)


KEK (Nov 2007, Nov 2008)

CERN (June 2008, September 2009)
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Summary

- **KEKB** is the **highest luminosity** machine in the world
- **Upgrade** of KEKB and Belle (2010-2014)
  - 40-fold increase in **luminosity**
  - Needs upgrades of all subdetectors
- New, enlarged **Silicon Vertex Detector**
  - **DEPFET** pixel double-layer
  - Four **strip** layers
- **Strip Detector R&D**
  - **New 6” Double Sided Strip Detectors** by HPK
  - **Origami** chip-on-sensor concept for low-mass DSSD readout
  - Readout with **hit time reconstruction** for improved background tolerance (up to 100x occupancy reduction w.r.t. now)
# Beam Parameters

<table>
<thead>
<tr>
<th></th>
<th>KEKB Design</th>
<th>KEKB Achieved: with crab</th>
<th>SuperKEKB High-Current</th>
<th>SuperKEKB Nano-Beam</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy (GeV) (LER/HER)</td>
<td>3.5/8.0</td>
<td>3.5/8.0</td>
<td>3.5/8.0</td>
<td>4.0/7.0</td>
</tr>
<tr>
<td>( \beta_y^* ) (mm)</td>
<td>10/10</td>
<td>5.9/5.9</td>
<td>3/6</td>
<td>0.27/0.42</td>
</tr>
<tr>
<td>( \varepsilon_x ) (nm)</td>
<td>18/18</td>
<td>18/24</td>
<td>24/18</td>
<td>3.2/2.4</td>
</tr>
<tr>
<td>( \sigma_y ) (\mu m)</td>
<td>1.9</td>
<td>0.94</td>
<td>0.85/0.73</td>
<td>0.059</td>
</tr>
<tr>
<td>( \xi_y )</td>
<td>0.052</td>
<td>0.129/0.090</td>
<td>0.3/0.51</td>
<td>0.09/0.09</td>
</tr>
<tr>
<td>( \sigma_z ) (mm)</td>
<td>4</td>
<td>\sim 6</td>
<td>5/3</td>
<td>6/5</td>
</tr>
<tr>
<td>( I_{\text{beam}} ) (A)</td>
<td>2.6/1.1</td>
<td>1.64/1.19</td>
<td>9.4/4.1</td>
<td>3.6/2.6</td>
</tr>
<tr>
<td>( N_{\text{bunches}} )</td>
<td>5000</td>
<td>1584</td>
<td>5000</td>
<td>2503</td>
</tr>
<tr>
<td>Luminosity ((10^{34} \text{ cm}^{-2} \text{ s}^{-1}))</td>
<td>1</td>
<td>2.11</td>
<td>53</td>
<td>80</td>
</tr>
</tbody>
</table>
KEKB accelerator upgrade

- Crab cavity
- 8 GeV $e^-$
- New IR with crab crossing and smaller $\beta_y^*$
- New beam-pipes with ante-chamber
- More RF for higher beam current
- Damping ring for $e^+$

KEKB accelerator upgrade
The Silicon Vertex Detector of the Belle II Experiment

Faster calorimeter with waveform sampling and pure CsI (endcap)

New particle identifier with precise Cherenkov device: (i)TOP or fDIRC. Endcap: Aerogel RICH

Background tolerant super small cell tracking detector

Si vertex detector with high background tolerance (+2 layers, pixels)

KL/µ detection with scintillator and next generation photon sensors

New dead-time-free pipelined readout and high speed computing systems

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The Silicon Vertex Detector of the Belle II Experiment

Micron Wafer Layout

- Quadratic baby sensors 2, 3, 4
  - p-side: 512 strips
  - 50 µm pitch
  - 1 interm. strip
  - n-side: 256 strips
  - 100 µm pitch
  - 0 interm. strip
  - different p-stop patterns

- Baby sensor 1
  - p-side: 512 strips
  - 50 µm pitch
  - 1 interm. strip
  - n-side: 512 strips
  - 100 µm pitch
  - 1 interm. strip
  - atoll p-stop

- Main sensor
  - p-side: 768 strips
  - 75-50 µm pitch
  - 1 interm. strip
  - n-side: 512 strips
  - 240 µm pitch
  - 1 interm. strip
  - combined p-stop

- Baby sensor 2, 3, 4
  - p-side: 512 strips
  - 50 µm pitch
  - 1 interm. strip
  - n-side: 256 strips
  - 100 µm pitch
  - 0 interm. strip
  - different p-stop patterns

  1) atoll p-stop
     varying distance from strip
  2) conventional p-stop
     varying width
  3) combined p-stop
     varying distance from strip

3 different GCDs for the n-side

Teststructures for p-side

Teststructures for n-side (no GCD)

Micron: p-stop layout

- p-stops connected
- p-stops isolated
- combined
## Current Barrel Layout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sensors/Ladder</th>
<th>Origamis/Ladder</th>
<th>Ladders</th>
<th>Length [mm]</th>
<th>Radius [mm]</th>
<th>Slant Angle [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>0</td>
<td>7/8</td>
<td>262</td>
<td>38</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>1</td>
<td>10</td>
<td>390</td>
<td>80</td>
<td>11.9</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>2</td>
<td>14</td>
<td>515</td>
<td>115</td>
<td>17.2</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>3</td>
<td>17</td>
<td>645</td>
<td>140</td>
<td>21.1</td>
</tr>
</tbody>
</table>

- **Origami**
- **Cooling Tubes**
- **Slanted Sensors**
- **Hybrid Boards**
Comparison VA1TA – APV25

VA1TA (SVD)
- Commercial product (IDEAS)
- $T_p = 800\,\text{ns} \ (300 \,\text{ns} - 1000 \,\text{ns})$
- no pipeline
- $<10 \,\text{MHz}$ readout
- 20 Mrad radiation tolerance
- noise: $\text{ENC} = 180 \,\text{e} + 7.5 \,\text{e/pF}$
- time over threshold: $\sim 2000 \,\text{ns}$
- single sample per trigger

APV25 (Belle-II SVD)
- Developed for CMS by IC London and RAL
- $T_p = 50 \,\text{ns} \ (30 \,\text{ns} - 200 \,\text{ns})$
- 192 cells analog pipeline
- $40 \,\text{MHz}$ readout
- $>100 \,\text{Mrad}$ radiation tolerance
- noise: $\text{ENC} = 250 \,\text{e} + 36 \,\text{e/pF}$
- time over threshold: $\sim 160 \,\text{ns}$
- multiple samples per trigger possible (Multi-Peak-Mode)
Measured Hit Time Precision

- Results achieved in **beam tests** with several different types of Belle DSSD prototype modules (covering a broad range of SNR).

- **2...3 ns RMS** accuracy at typical cluster SNR (15...25)

- Working on implementation in **FPGA** (using lookup tables) – simulation successful.

![Time Resolution vs. Cluster SNR](image)
### Origami Material Budget

**X₀ comparison between conventional and chip-on-sensor (4” sensors):**

#### Conventional (double layer kapton)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>X₀ (mm)</th>
<th>Thickness (mm)</th>
<th>Percentage</th>
<th>Area coverage</th>
<th>Averaged Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor</td>
<td>Silicon</td>
<td>93.7</td>
<td>0.3</td>
<td>0.32%</td>
<td>100.0%</td>
<td>0.320%</td>
</tr>
<tr>
<td>Fanout</td>
<td>Polyimide (2 layer of 50um each)</td>
<td>300.0</td>
<td>0.1</td>
<td>0.03%</td>
<td>96.3%</td>
<td>0.032%</td>
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<tr>
<td>Copper</td>
<td>(10um)</td>
<td>14.0</td>
<td>0.01</td>
<td>0.07%</td>
<td>50.0%</td>
<td>0.036%</td>
</tr>
<tr>
<td>Nickel</td>
<td>(top: 1.3um)</td>
<td>14.3</td>
<td>0.0013</td>
<td>0.01%</td>
<td>50.0%</td>
<td>0.005%</td>
</tr>
<tr>
<td>Gold</td>
<td>(top: 0.8um)</td>
<td>3.4</td>
<td>0.0006</td>
<td>0.02%</td>
<td>50.0%</td>
<td>0.012%</td>
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<tr>
<td>Ribs</td>
<td>Zylon (0.5mm wide)</td>
<td>300.0</td>
<td>5</td>
<td>1.67%</td>
<td>3.7%</td>
<td>0.062%</td>
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<tr>
<td>Glue</td>
<td>Araldite 2011 / Double sided tape</td>
<td>335.0</td>
<td>0.05</td>
<td>0.01%</td>
<td>96.3%</td>
<td>0.014%</td>
</tr>
</tbody>
</table>

**Total** 0.480%

#### DSSD Chip-on-Sensor (4-layer kapton)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>X₀ (mm)</th>
<th>Thickness (mm)</th>
<th>Percentage</th>
<th>Area coverage</th>
<th>Averaged Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor</td>
<td>Silicon</td>
<td>93.7</td>
<td>0.3</td>
<td>0.32%</td>
<td>100.0%</td>
<td>0.320%</td>
</tr>
<tr>
<td>Isolation</td>
<td>Rohacell (Degussa)</td>
<td>5450.0</td>
<td>1</td>
<td>0.02%</td>
<td>96.3%</td>
<td>0.018%</td>
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<tr>
<td>Hybrid</td>
<td>Polyimide (4 layers of 50um each)</td>
<td>300.0</td>
<td>0.2</td>
<td>0.07%</td>
<td>96.3%</td>
<td>0.064%</td>
</tr>
<tr>
<td>Copper</td>
<td>(4 layers of 5um each)</td>
<td>14.0</td>
<td>0.02</td>
<td>0.14%</td>
<td>64.7%</td>
<td>0.092%</td>
</tr>
<tr>
<td>Nickel</td>
<td>(top: 1.3um)</td>
<td>14.3</td>
<td>0.0013</td>
<td>0.01%</td>
<td>64.7%</td>
<td>0.006%</td>
</tr>
<tr>
<td>Flash Gold</td>
<td>(top: 0.4um)</td>
<td>3.4</td>
<td>0.0004</td>
<td>0.01%</td>
<td>64.7%</td>
<td>0.008%</td>
</tr>
<tr>
<td>Flexes</td>
<td>Polyimide (1 layer of 25um)</td>
<td>300.0</td>
<td>0.025</td>
<td>0.01%</td>
<td>56.3%</td>
<td>0.005%</td>
</tr>
<tr>
<td>Copper</td>
<td>(1 layer of 5um)</td>
<td>14.0</td>
<td>0.005</td>
<td>0.04%</td>
<td>28.1%</td>
<td>0.010%</td>
</tr>
<tr>
<td>Nickel</td>
<td>(top: 1.3um)</td>
<td>14.3</td>
<td>0.0013</td>
<td>0.01%</td>
<td>28.1%</td>
<td>0.003%</td>
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<tr>
<td>Flash Gold</td>
<td>(top: 0.4um)</td>
<td>3.4</td>
<td>0.0004</td>
<td>0.01%</td>
<td>28.1%</td>
<td>0.003%</td>
</tr>
<tr>
<td>8 * APV25</td>
<td>Silicon</td>
<td>93.7</td>
<td>0.1</td>
<td>0.11%</td>
<td>21.4%</td>
<td>0.023%</td>
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<td>SMDs</td>
<td>SMD</td>
<td>50.0</td>
<td>0.4</td>
<td>0.80%</td>
<td>8.0%</td>
<td>0.007%</td>
</tr>
<tr>
<td>Si-Pad</td>
<td>Si-Pad 800 (Bergquist)</td>
<td>200.0</td>
<td>0.127</td>
<td>0.06%</td>
<td>11%</td>
<td>0.007%</td>
</tr>
<tr>
<td>Pipe</td>
<td>Aluminum (D=2.0mm, wall=0.2mm)</td>
<td>89.0</td>
<td>0.56</td>
<td>0.63%</td>
<td>7%</td>
<td>0.047%</td>
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<tr>
<td>Rib</td>
<td>Zylon (0.5mm wide)</td>
<td>300.0</td>
<td>5</td>
<td>1.67%</td>
<td>1.9%</td>
<td>0.031%</td>
</tr>
<tr>
<td>Glue</td>
<td>Araldite 2011</td>
<td>335.0</td>
<td>0.2</td>
<td>0.06%</td>
<td>50%</td>
<td>0.030%</td>
</tr>
<tr>
<td>Cooling</td>
<td>Water</td>
<td>360.5</td>
<td>1.26</td>
<td>0.35%</td>
<td>13%</td>
<td>0.047%</td>
</tr>
</tbody>
</table>

**Total** 0.719%

- **+50%** increase in material, but also **huge** improvement in SNR
- **Trade-off** between material budget and SNR
- According to simulation, additional material is prohibitive in 2 innermost layers, but **no problem for layers 3-5** → OK with layout
Maximum Radiation Length Distribution

![Graph showing radiation length distribution for different materials.]

- **Profile [mm]**
- **Radiation Length [%]**
- **Rib Design**

Materials:
- CFRP
- Rohacell
- Pipe
- Coolant
- APV
- Kapton
- Sensor
- Rohacell

10 June 2010

T. Bergauer
Cooling Boundary Conditions

- Power dissipation/APV: 0.4 W
- 1 Origami sensor features 10 APVs

<table>
<thead>
<tr>
<th>Origamis/Ladder</th>
<th>Ladders</th>
<th>APVs Origami</th>
<th>APVs Hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 6</td>
<td>3</td>
<td>17</td>
<td>510</td>
</tr>
<tr>
<td>Layer 5</td>
<td>2</td>
<td>14</td>
<td>280</td>
</tr>
<tr>
<td>Layer 4</td>
<td>1</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>Layer 3</td>
<td>0</td>
<td>8</td>
<td>0</td>
</tr>
</tbody>
</table>

- Total Origami power dissipation: 356 W
- 404 W dissipated at the hybridboards
- Total SVD power dissipation: 760 W