The NA62 Gigatracker

presented by A. Kluge

CERN/PH-ESE

June 10, 2010

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[a] CERN, Geneva Switzerland, [b] INFN Torino, Italy, [c] INFN Ferrara, Italy, [d] UCL Louvain la Neuve, Belgium, [d] EPFL Lausanne Switzerland

Outline

- NA62, introduction, challenge
- GigaTracker
  - specifications, module, beam/data rate
  - electronics architecture
  - demonstrator ASICs
  - cooling
- Summary

NA62 - Introduction

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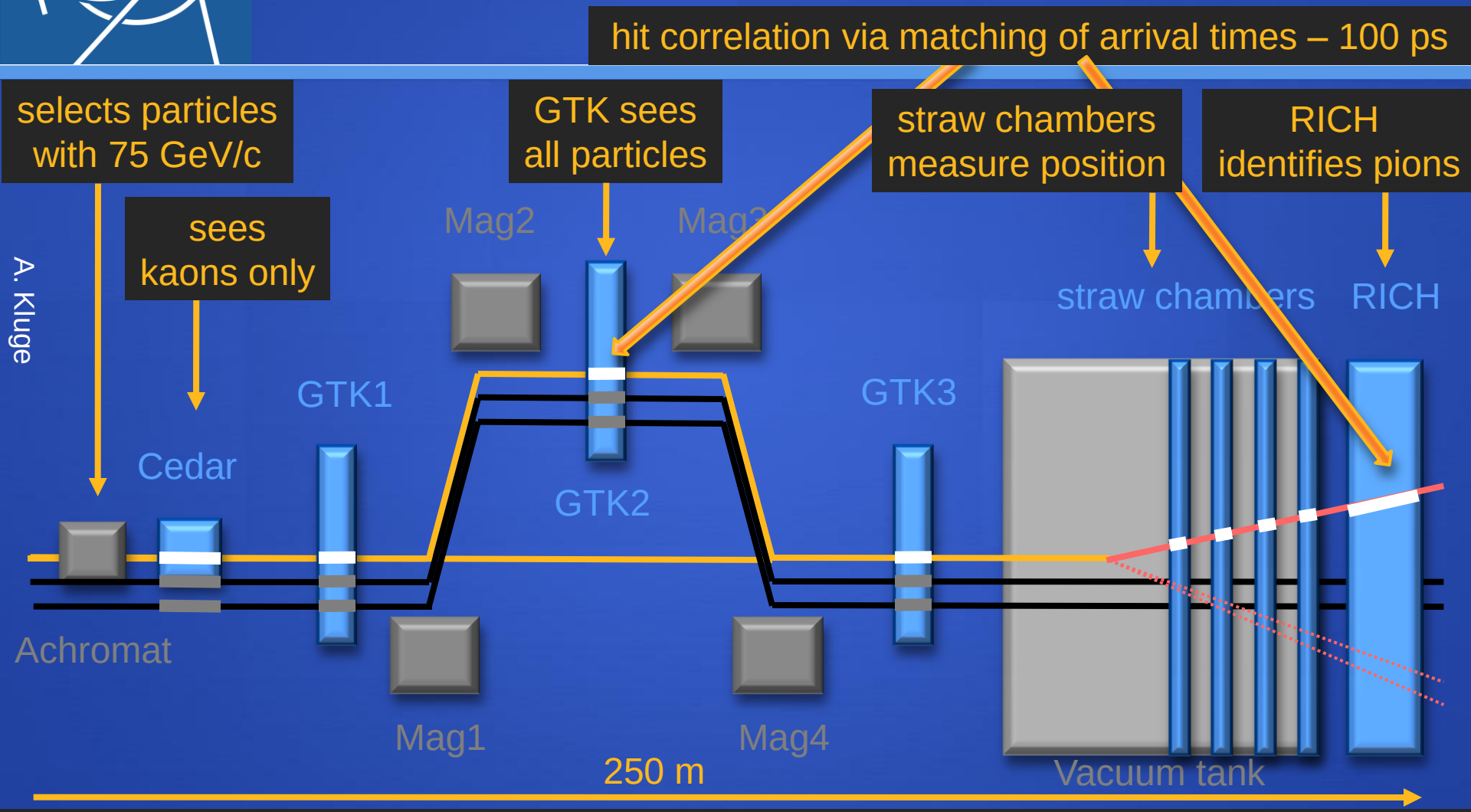
Experimental setup- NA62



beam: hadrons, only 6% kaons-> only 20% of charged kaon decay in the vacuum tank
-> out of which only 10^{-11} decays are of interest (pion-neutrino-antineutrino)

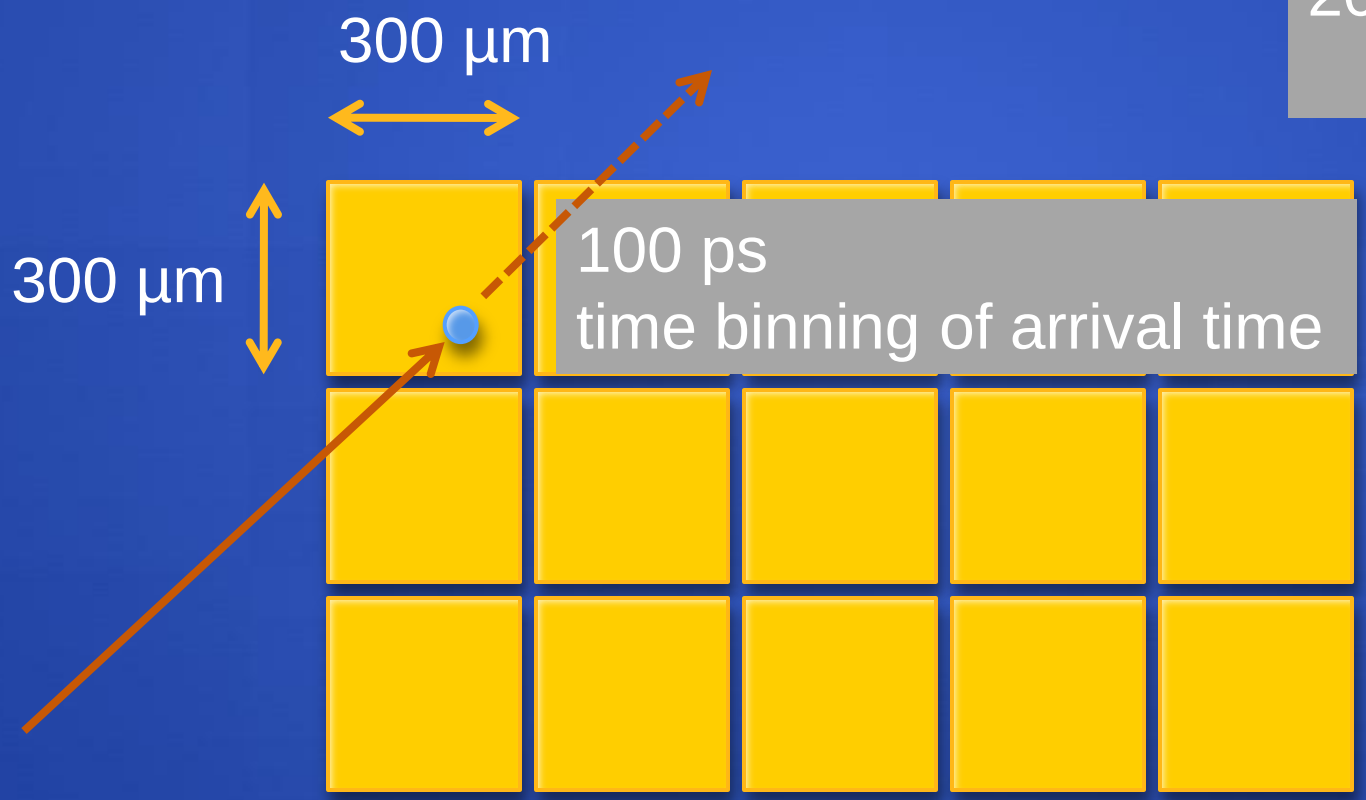
Experimental setup- NA62

beam: hadrons, only 6% kaons ->	0.06
only 20% of charged kaon decay in the vacuum tank ->	0.20
out of which only 10^{-11} decays are of interest -> decay into one pion, one neutrino and one anti-neutrino	10^{-11}
total probability	1.2×10^{-13}

- **100 events of kaon -> pion/neutrino/antineutrino**
  any deviation from standard model -> new physics

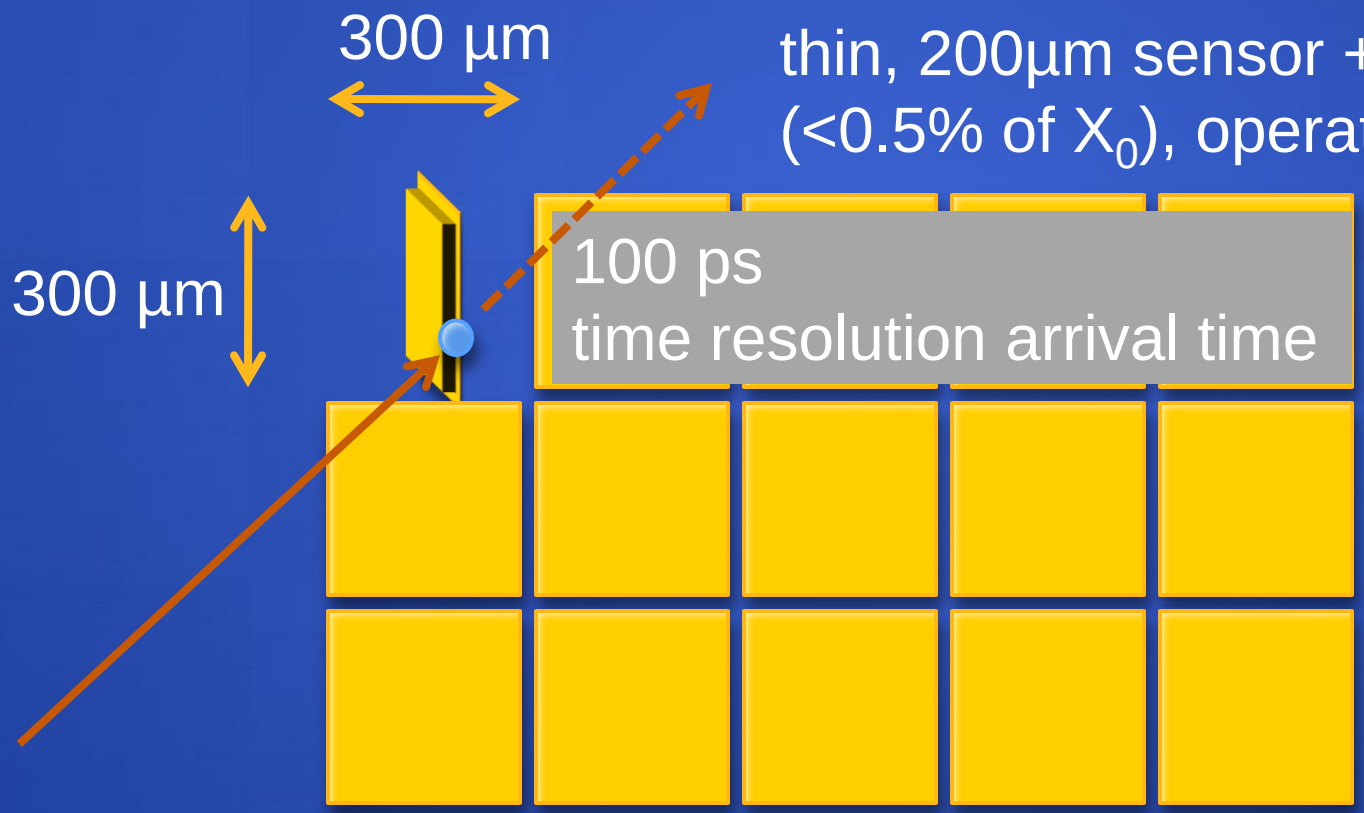
Experimental setup: GTK specifications

200 ps per station



800 MHz particle rate

Experimental setup: GTK specifications



thin, 200µm sensor + 100 µm chip
(<0.5% of X_0), operated in vacuum

Beam & detector configuration

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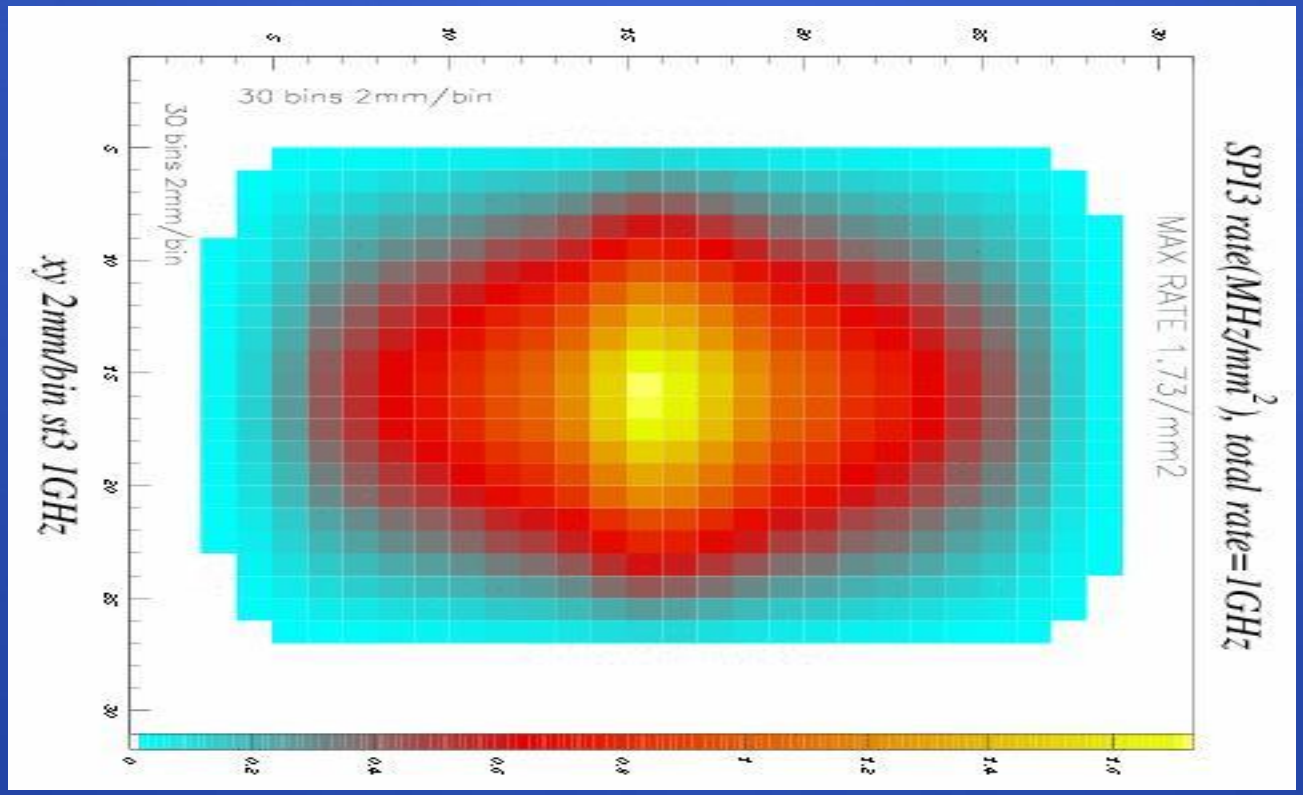
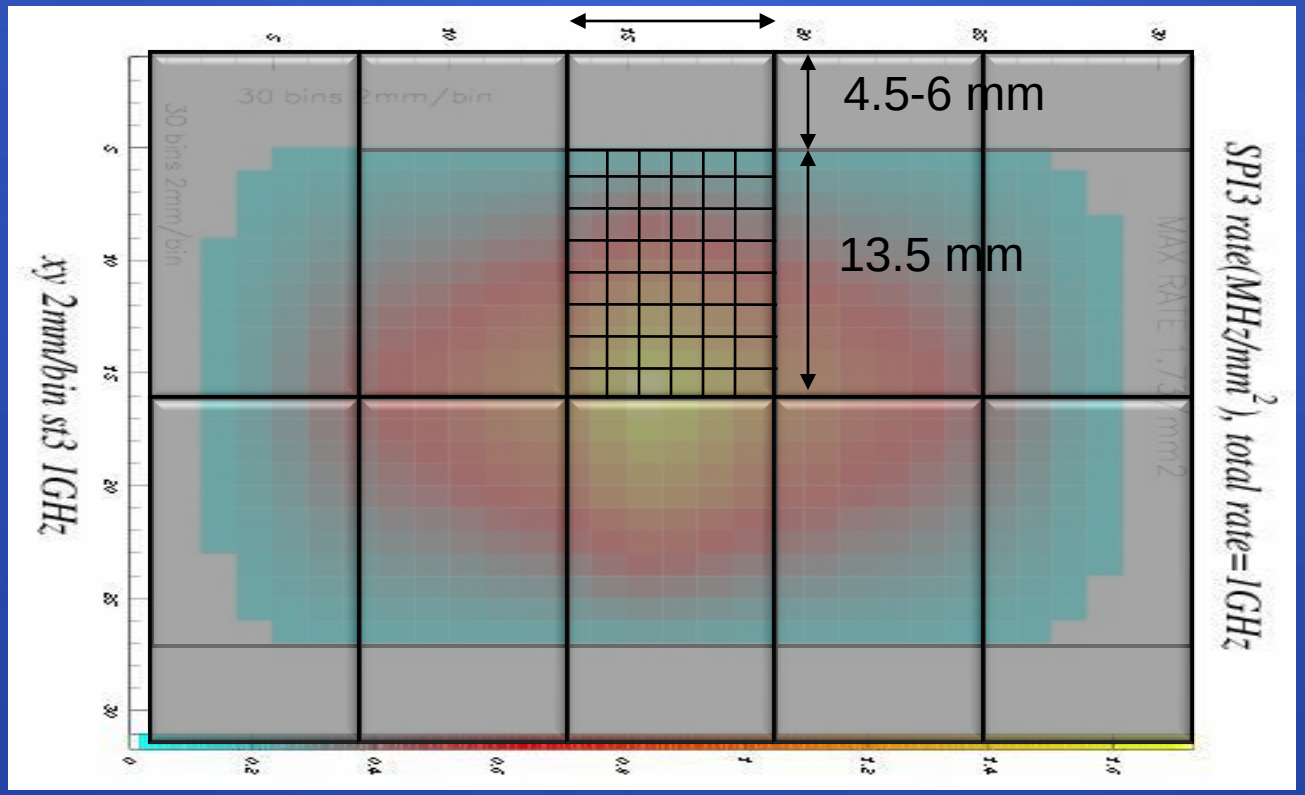
Beam profile

60 mm



27 mm

ASIC covering beam



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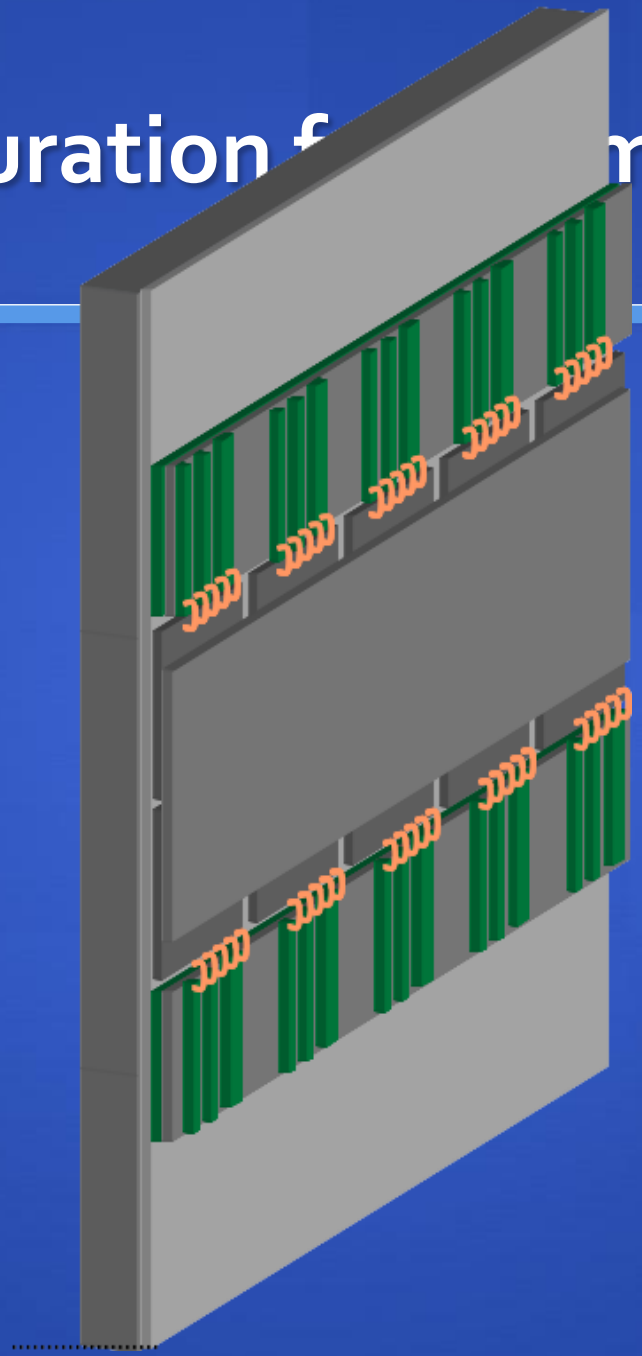
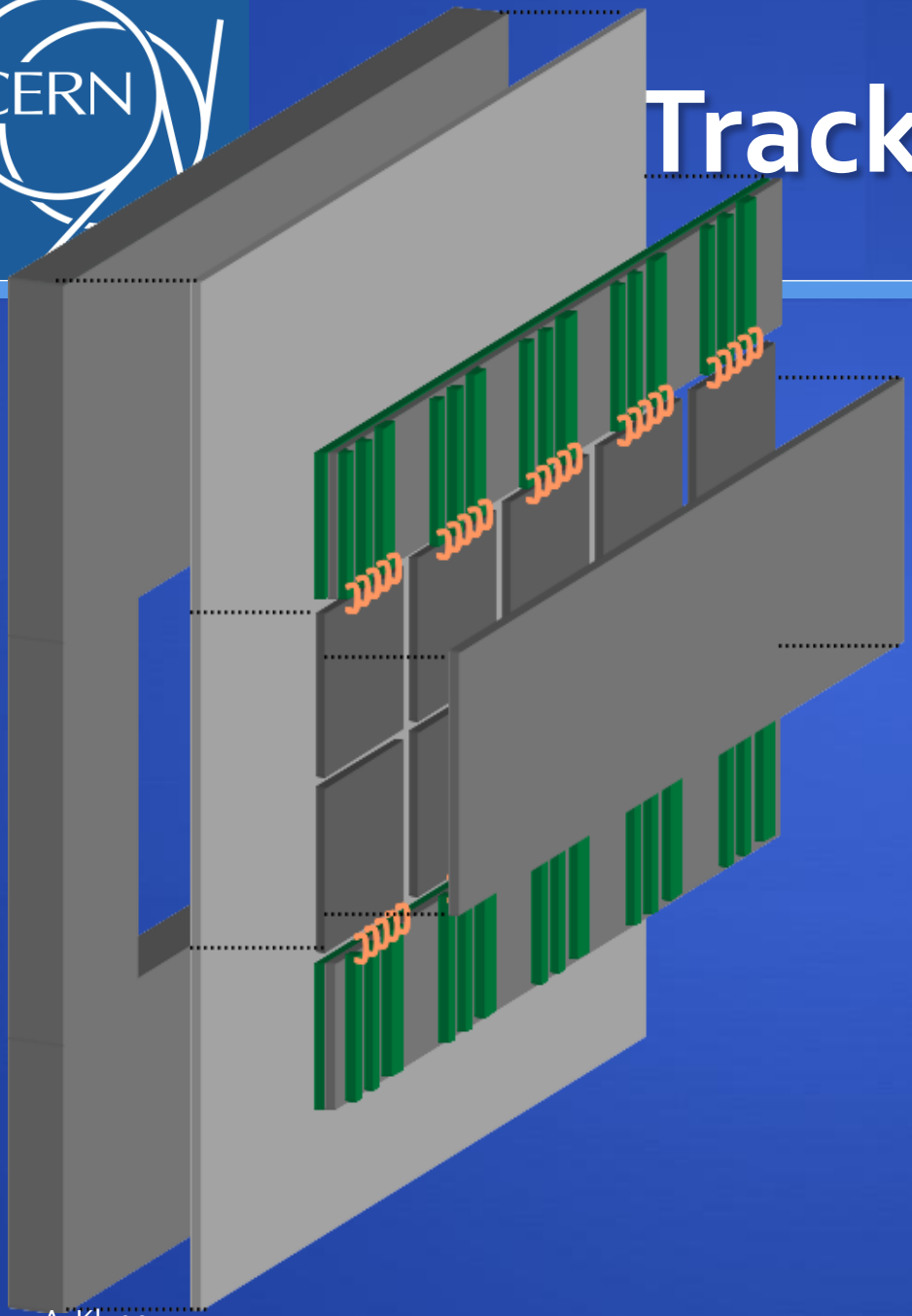
45 rows times 40 columns per chip = 1800 pixels per chip

Configuration f m 27-60



Tracker setup



- Sensor&bonds: 0.24% X_0 (200 µm Silicon)
- RO chip: 0.11% X_0 (100 µm Silicon)
- Structure: 0.10% X_0 (100 µm Carbon or silicon)
- Total: 0.45% X_0 uniform

The electronics specification

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General: System Specifications

Number of pixels per chip	1800 = 45 x 40
Size of pixels	300 µm x 300 µm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
Chip design time resolution	100 ps (rms)
Thickness of sensor	200 µm
Type of sensor	p in n
Thickness of read-out chip	100 µm
Dynamic input range	5000 – 60000 electrons

General: System Specifications

Design particle rate per chip	130 MHz
Rate of center pixel	140 kHz
Rate of center column	~ 3.3 MHz or 0.82 MHz/mm^2
Average rate per pixel	73 kHz
Maximum dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	~ 10^5 Gy
Neutron flux in 100 days	2 x 10^{14} 1 MeV neutron equivalent cm^{-2}
Material budget/thickness	0.5 % X_0 per station

The ASIC architecture

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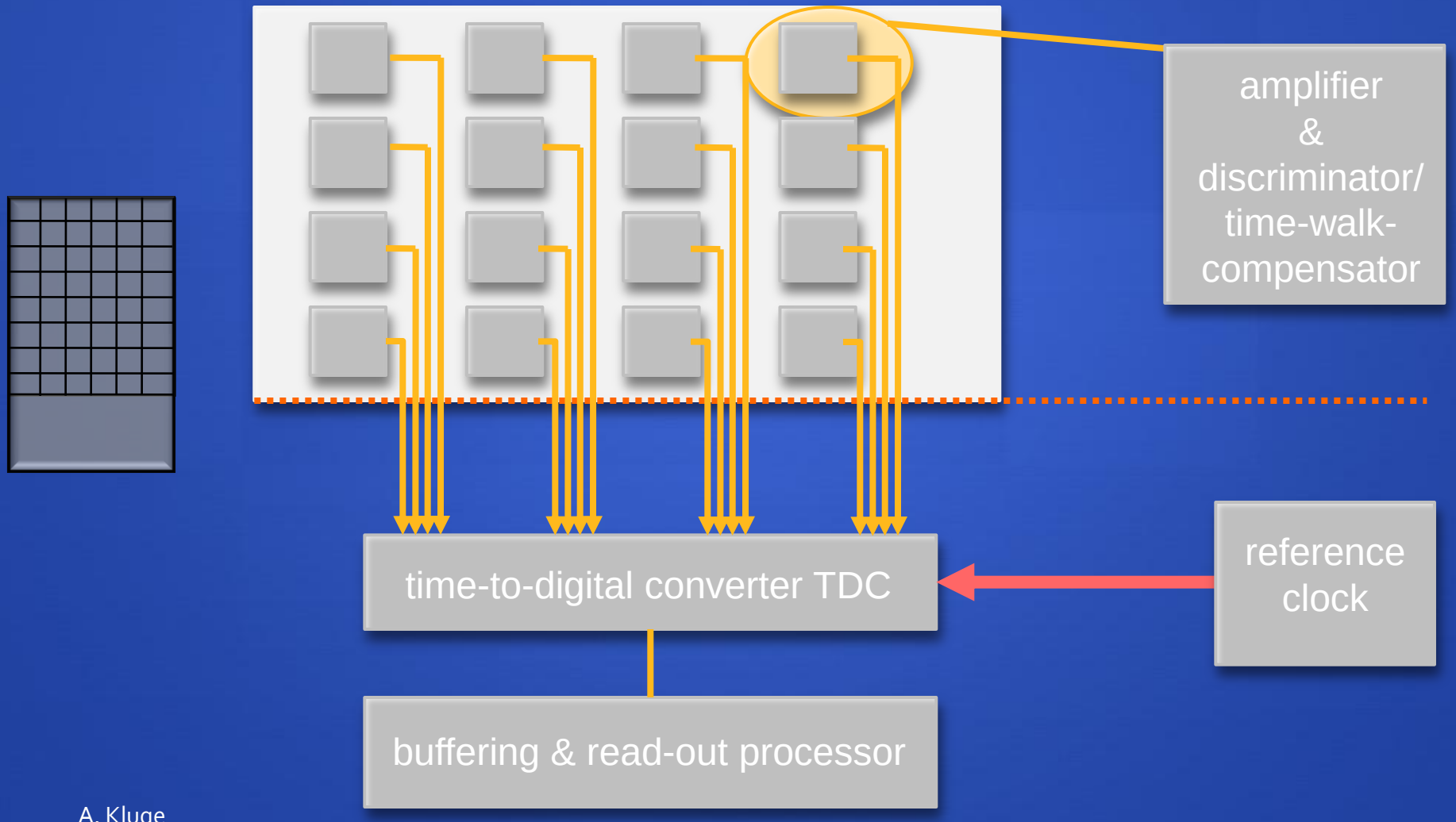
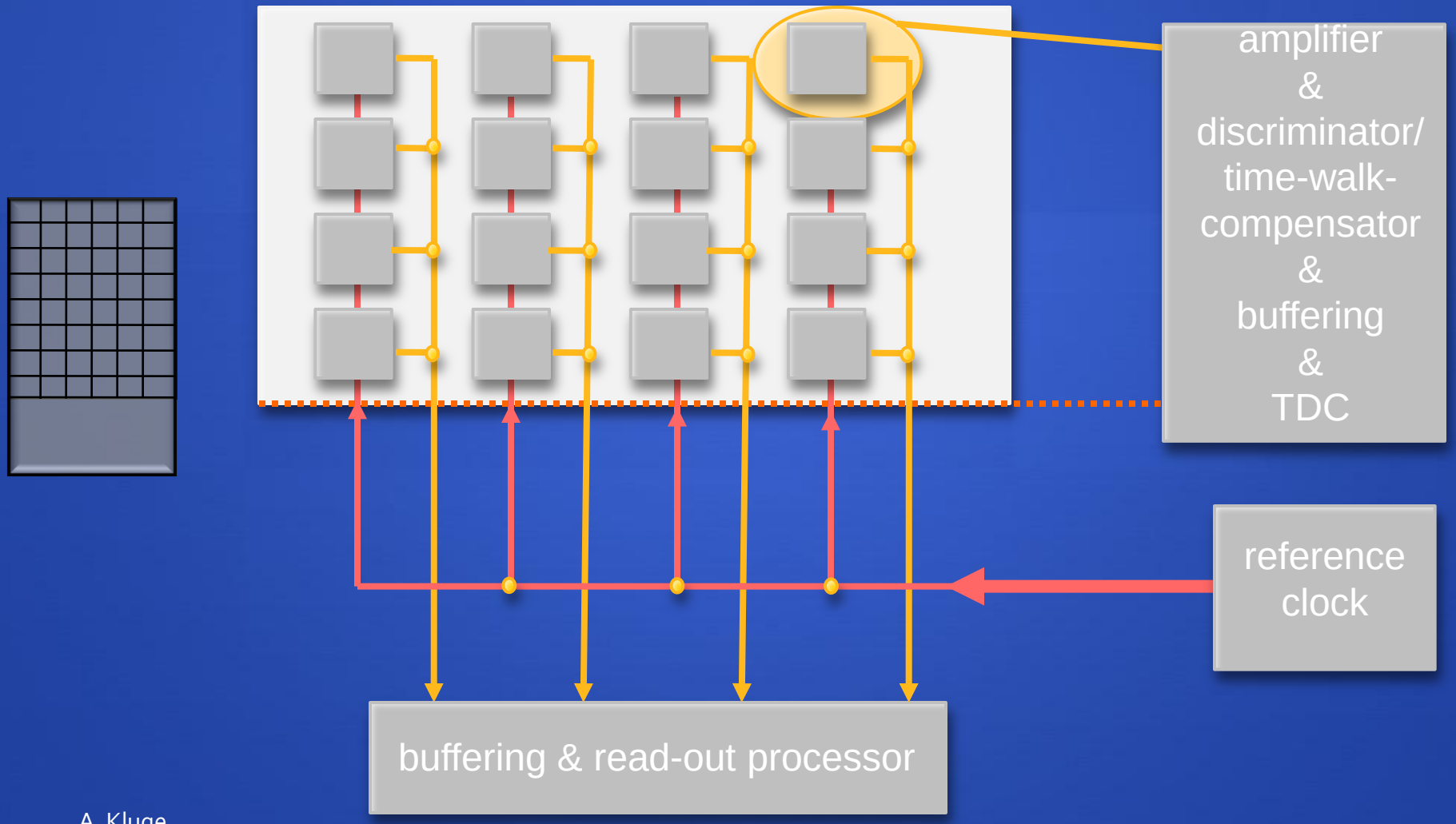
Jitter-free pixel signal to TDC in EOC



Precise clock signal to all pixels



TDC per pixel architecture

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The time-to-digital conversion
Dual slope TDC

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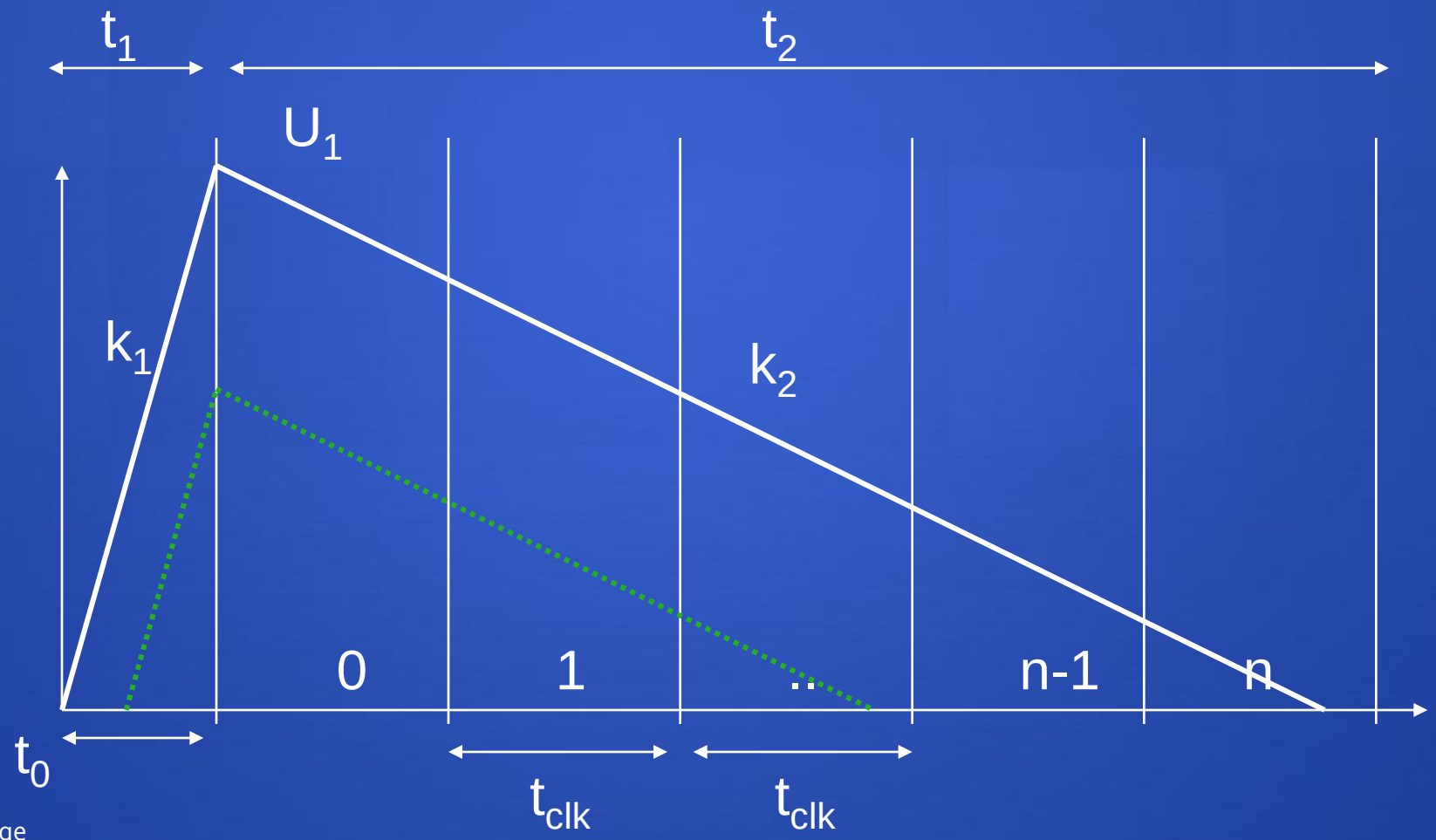
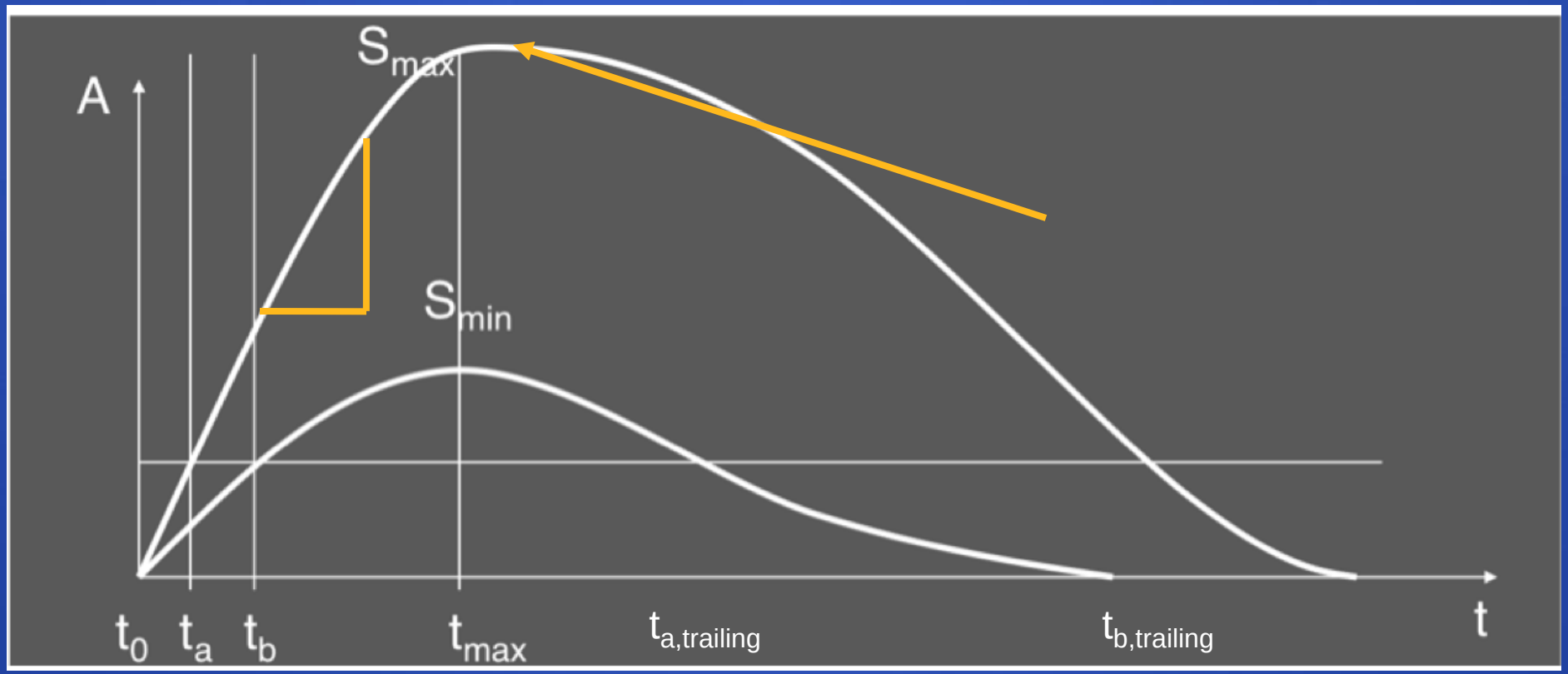
TDC Wilkinson (dual slope)

$t_o = n\, t_{clk}\, k_2 / k_1$



time walk

Constant fraction discriminator



End-of-column architecture

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The time-to-digital conversion
Delay locked loop based TDC

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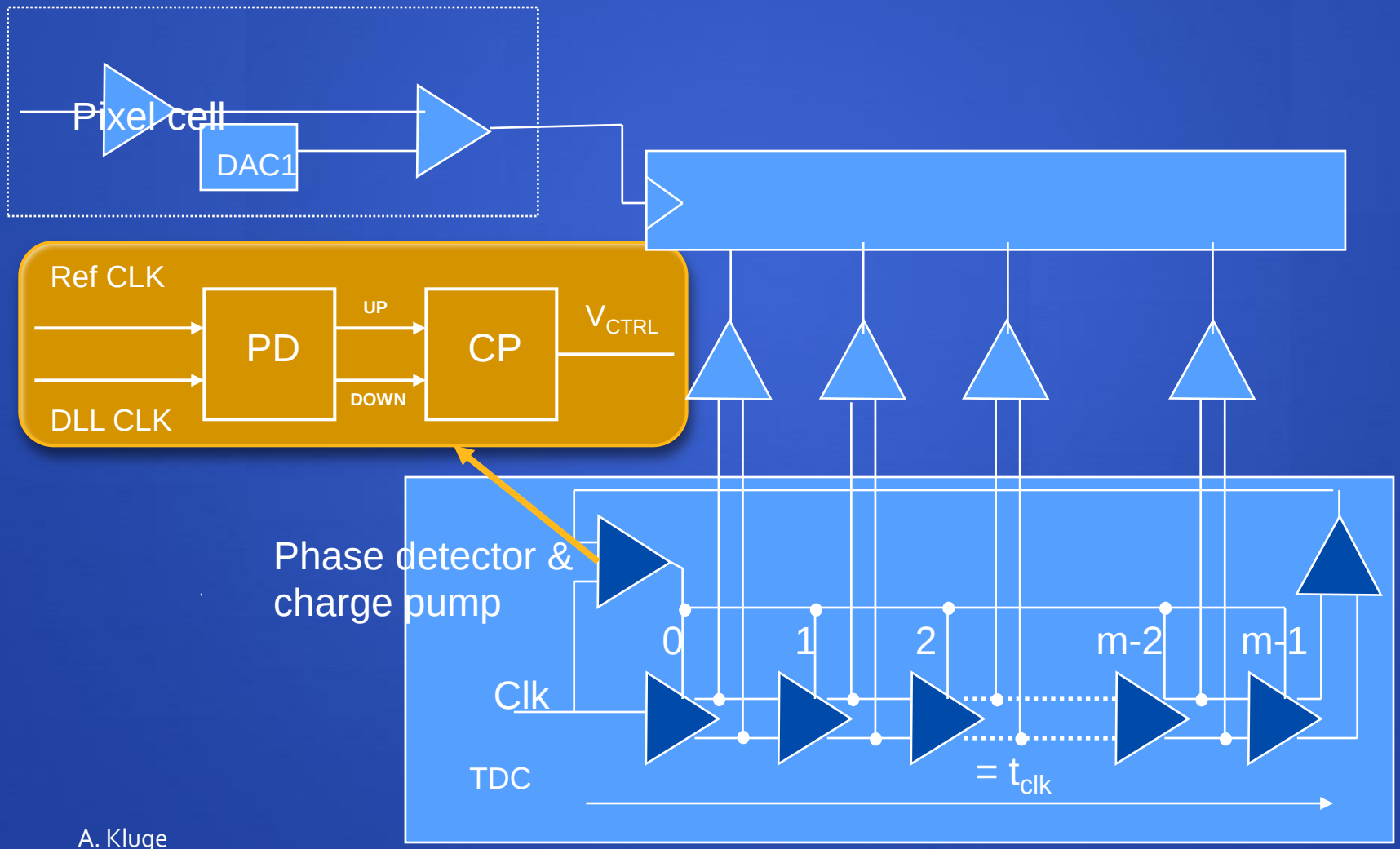
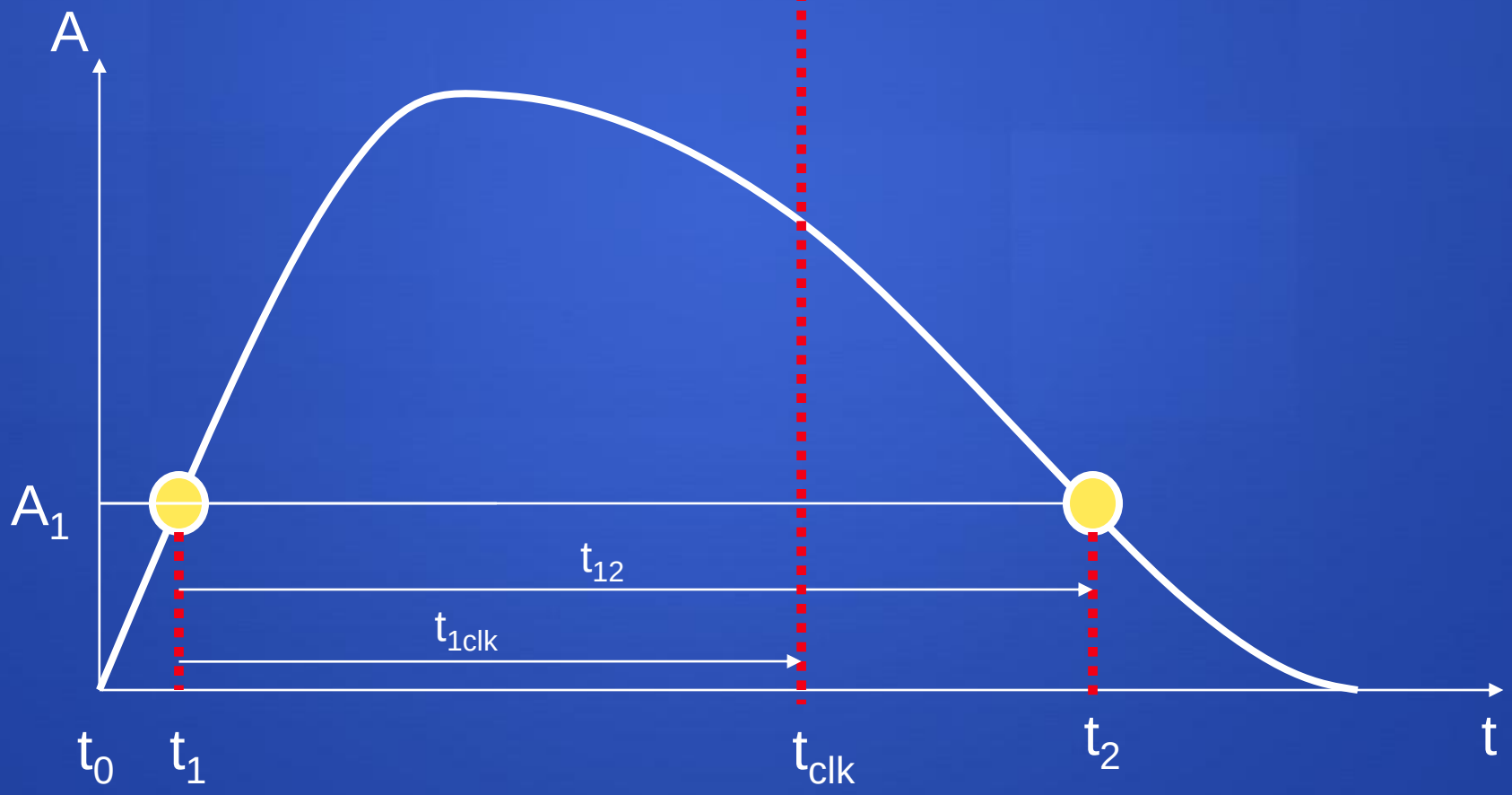
DLL based TDC

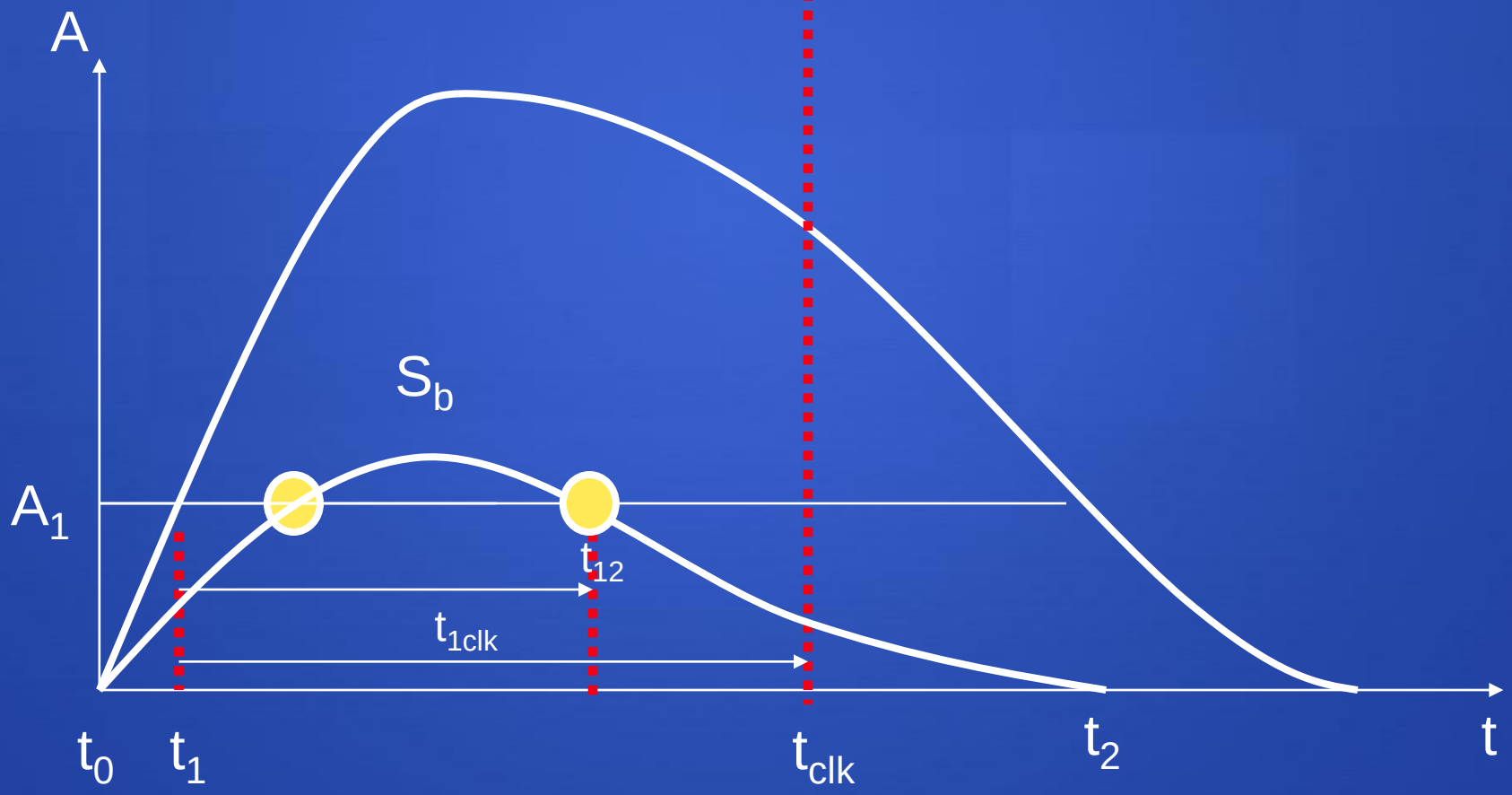


time walk

time-over-threshold



Time-over-threshold



Demonstrator

Demonstrator

- On-pixel
  dual slope TDC with CFD time walk compensation
- End-of-column
  DLL based TDC with time-over-threshold compensation
- 2 demonstrator ASICs
  - 45 pixel - folded column with full frontend
  - complete TDC system
  - reduced read-out and formatting functionality

TDC per pixel architecture

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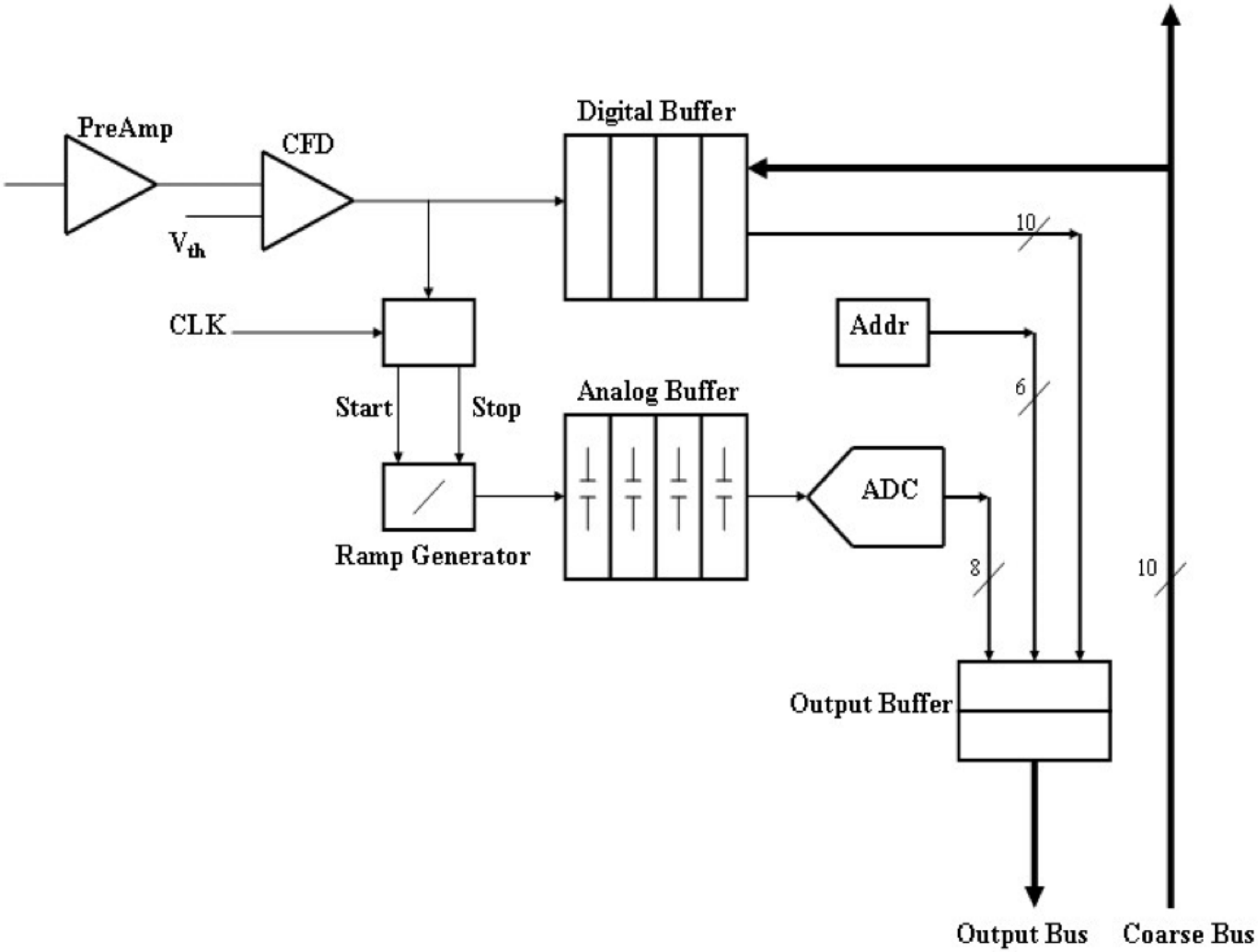
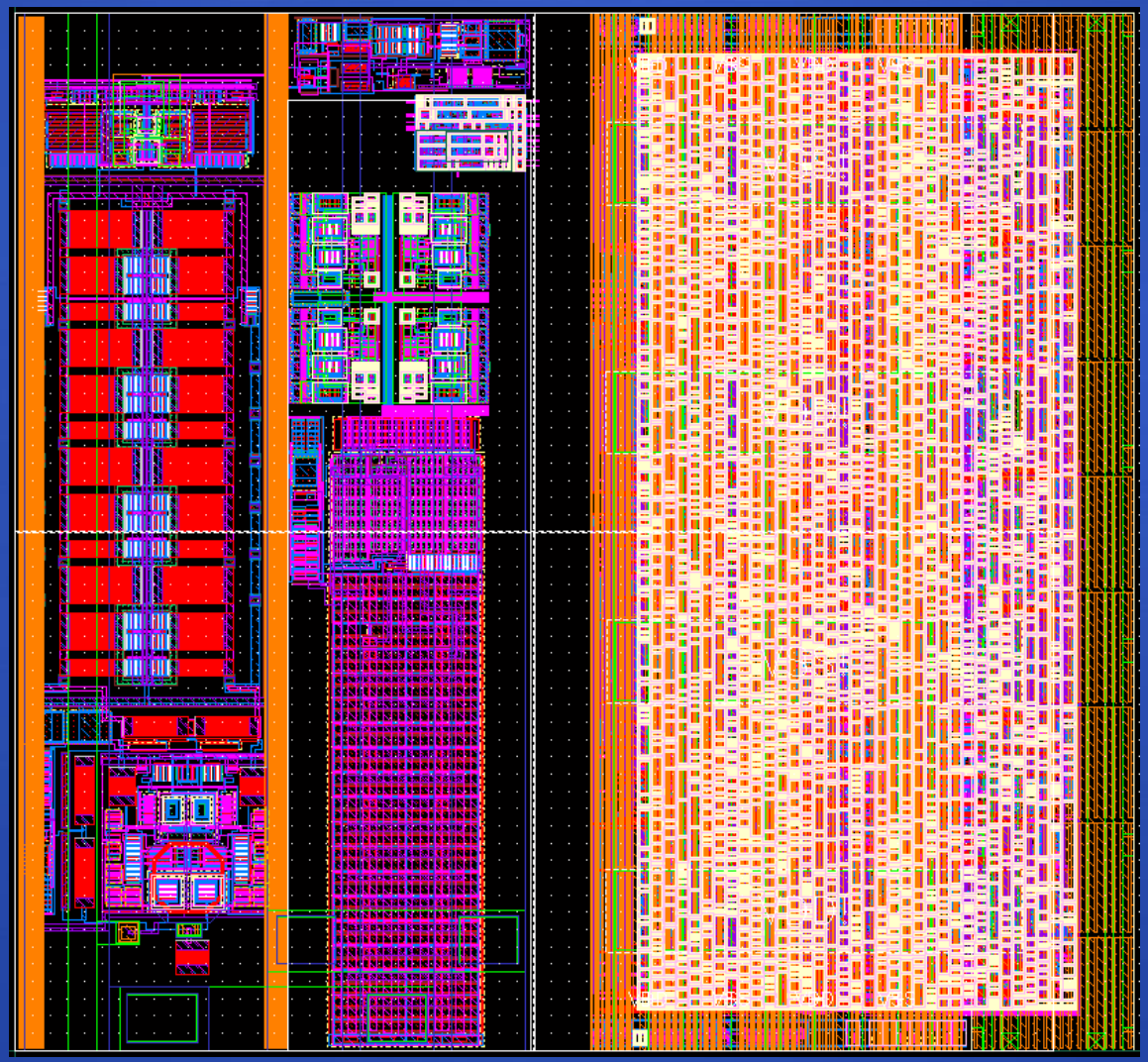
On pixel cell TDC



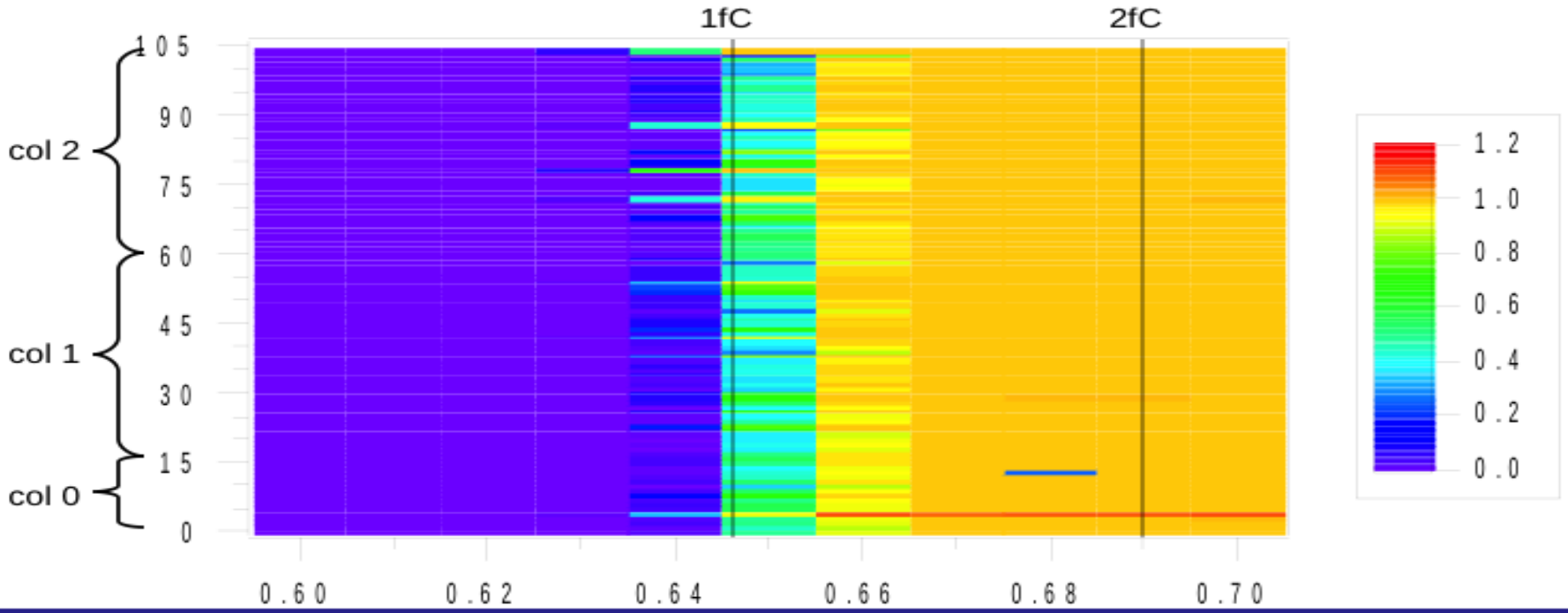
Layout – on pixel TDC 130µm



Efficiency and calibration

Efficiency (2)

- First equalization: full efficiency at 1.45fC

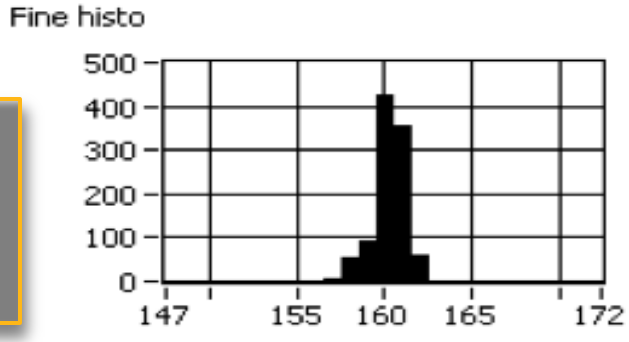


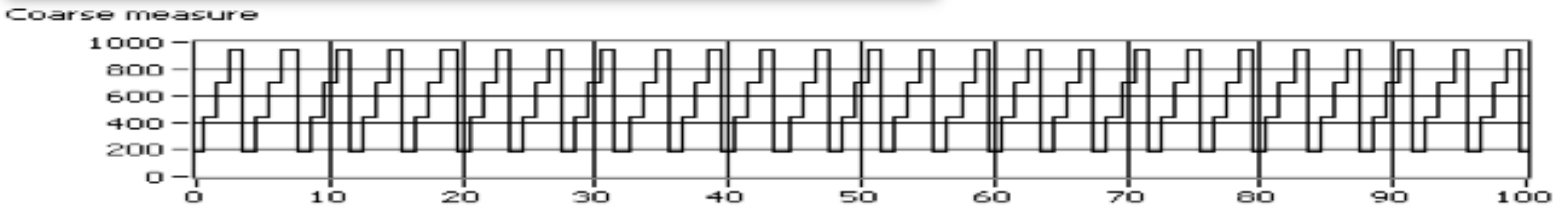
Preliminary pTDC jitter

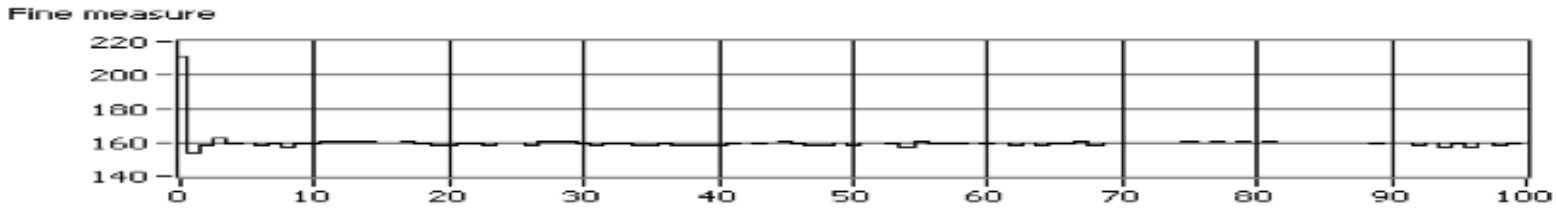
Preliminary time measures (2)

- Synchronous Test Pulse

Promising test results







EOC column architecture

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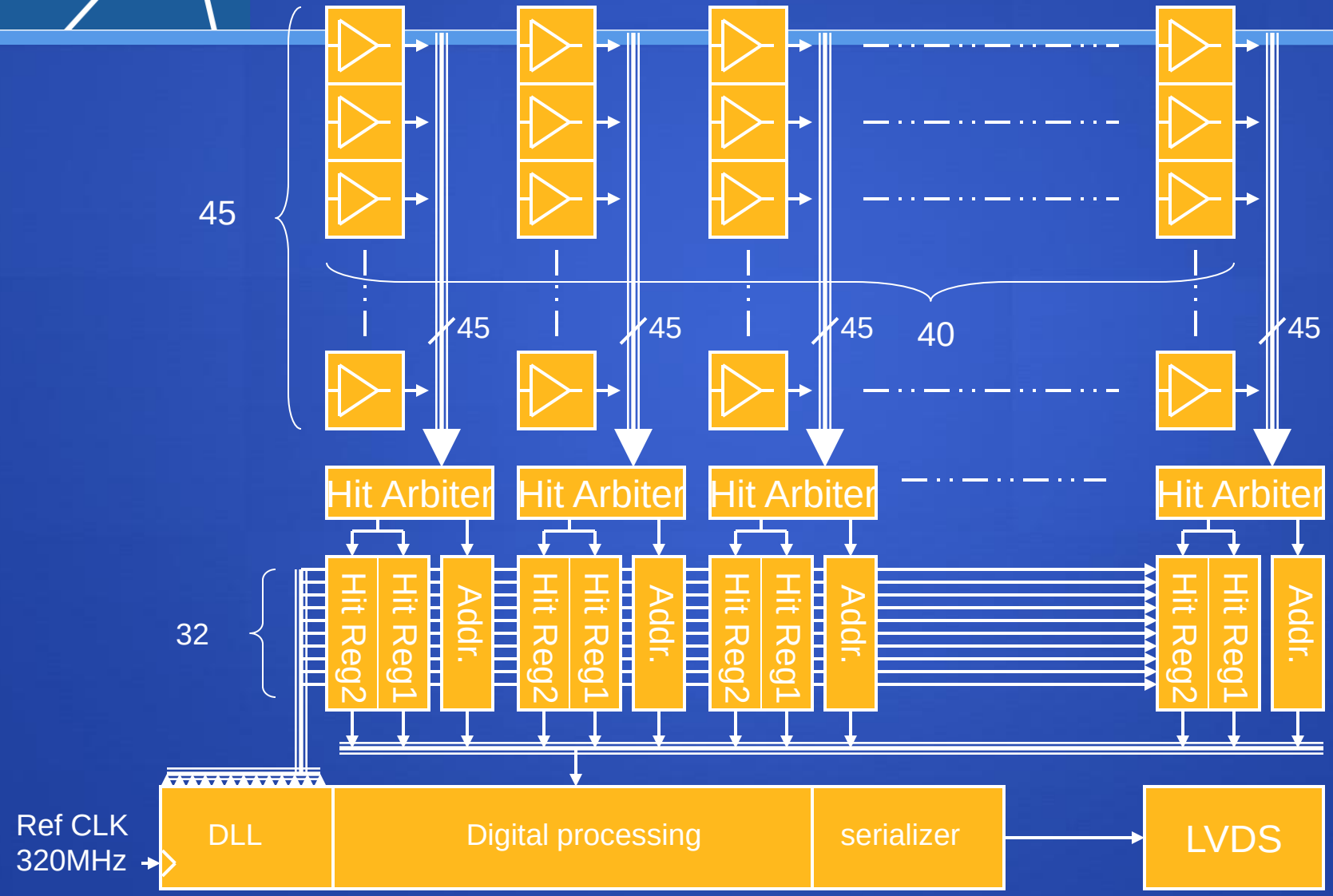
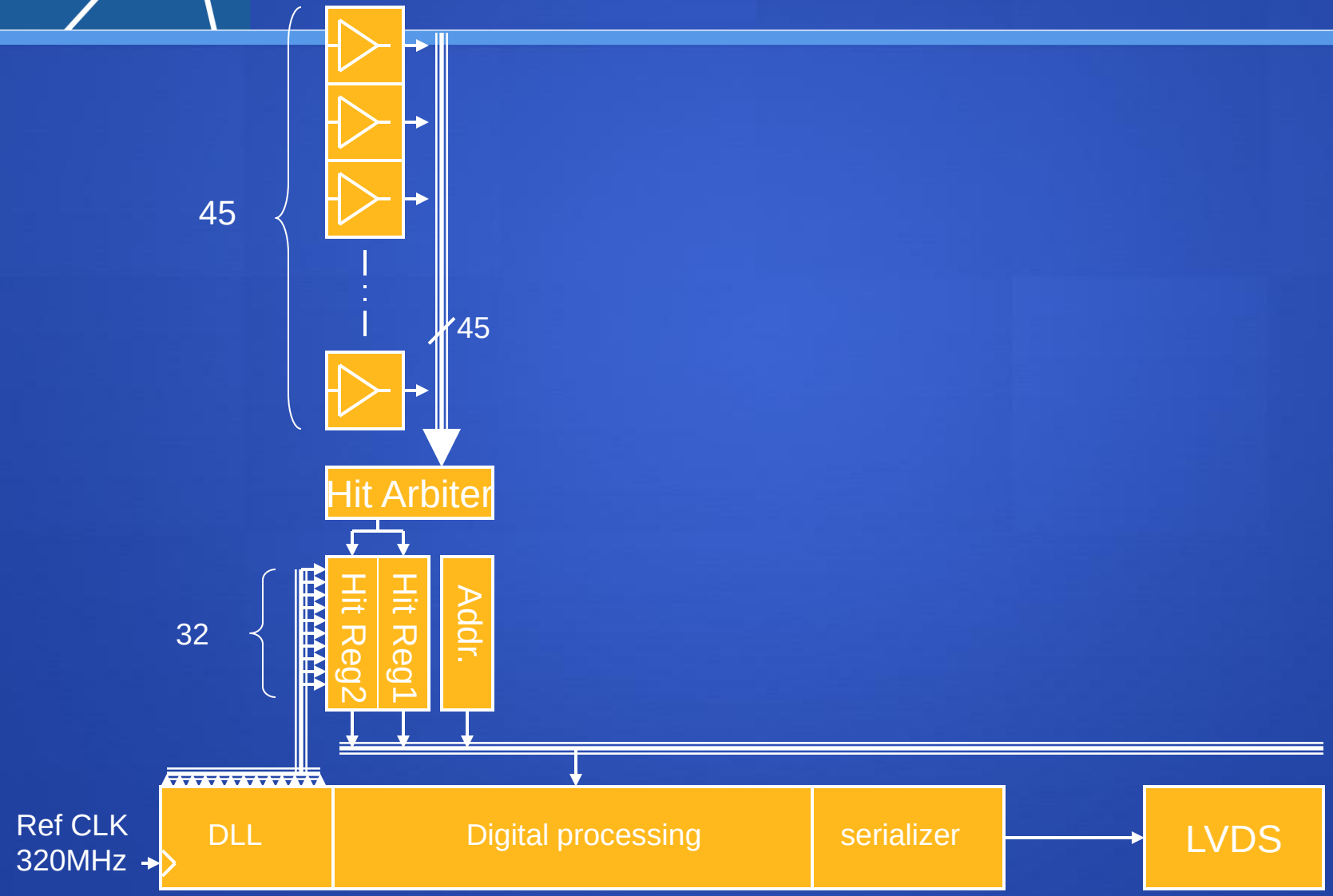
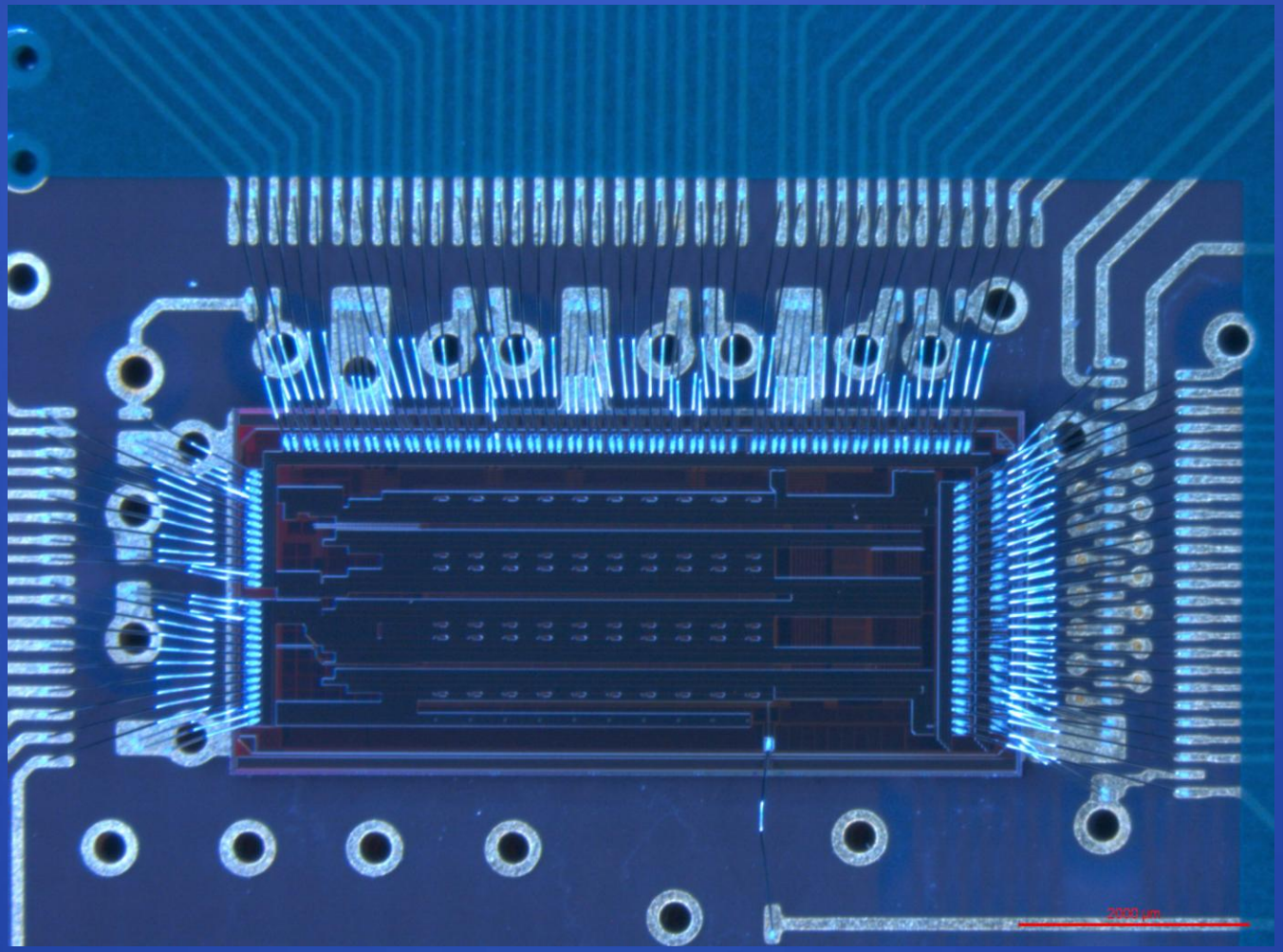
45 x 40 pixel final chip



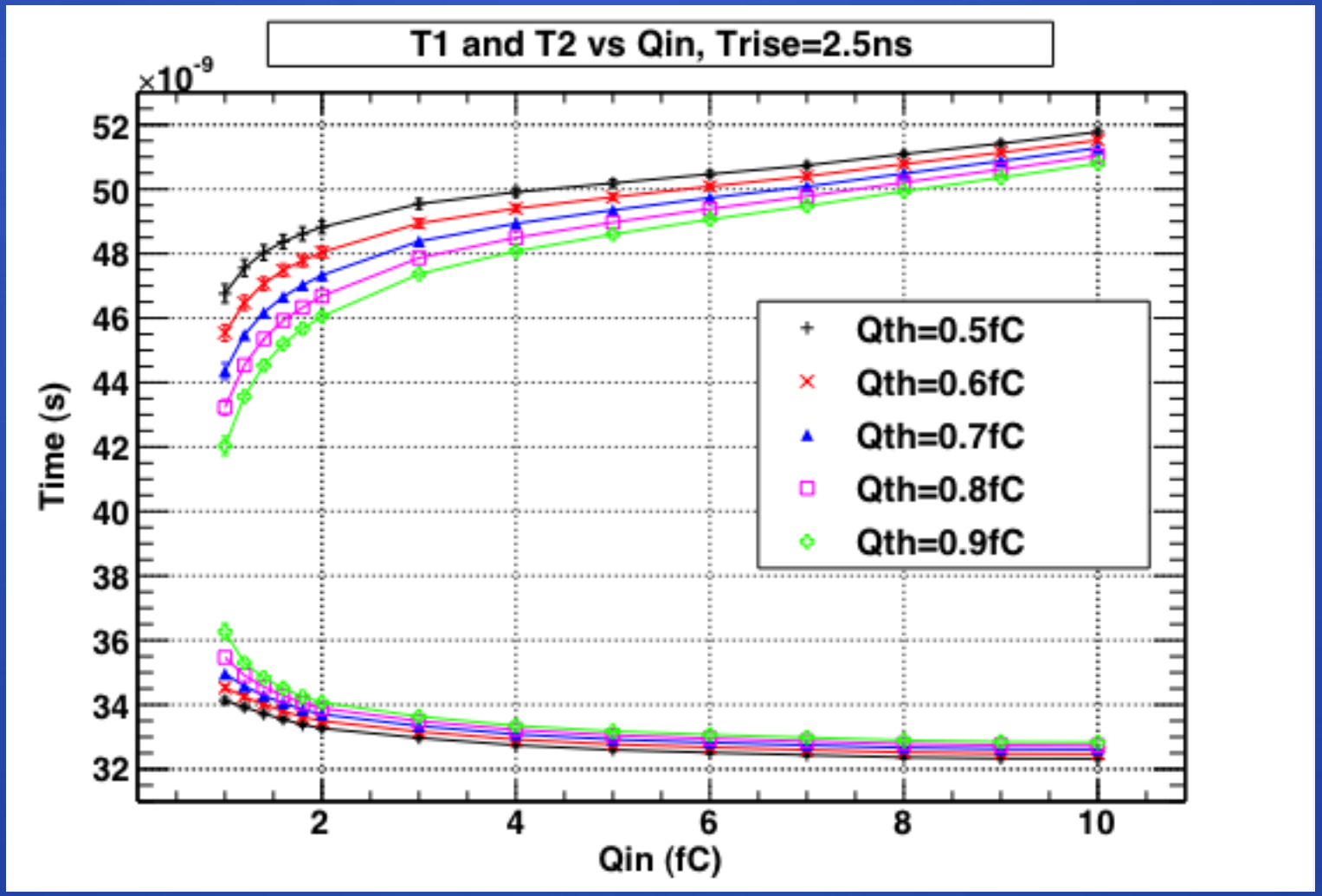
45 x 1 demonstrator



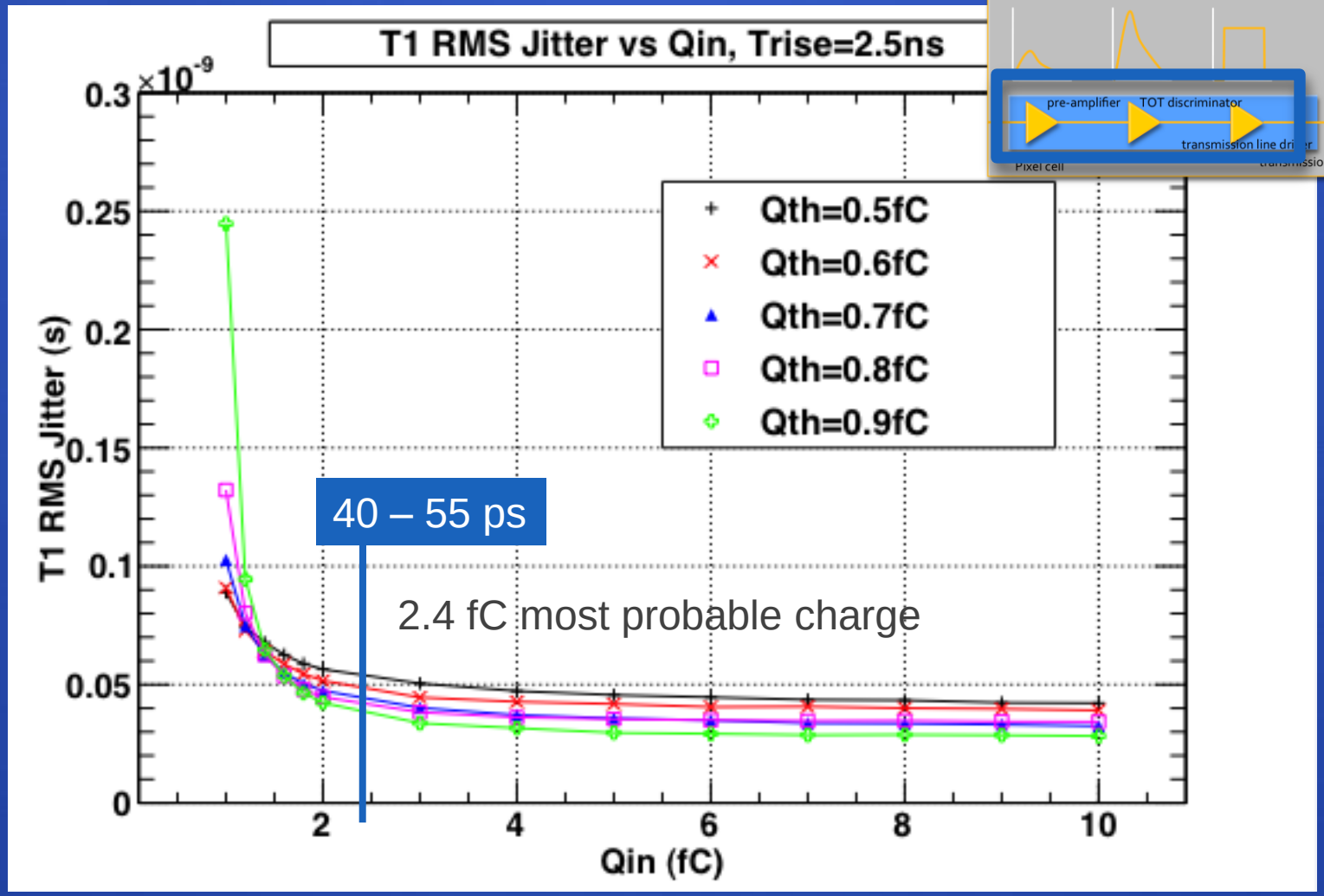
GTK demonstrator ASIC



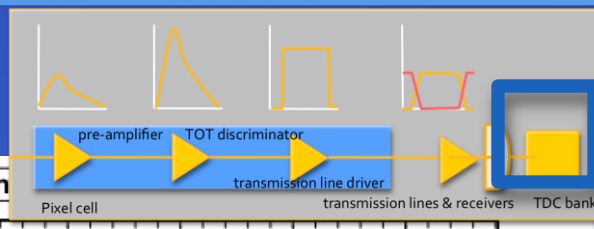
T1, T2 versus input charge

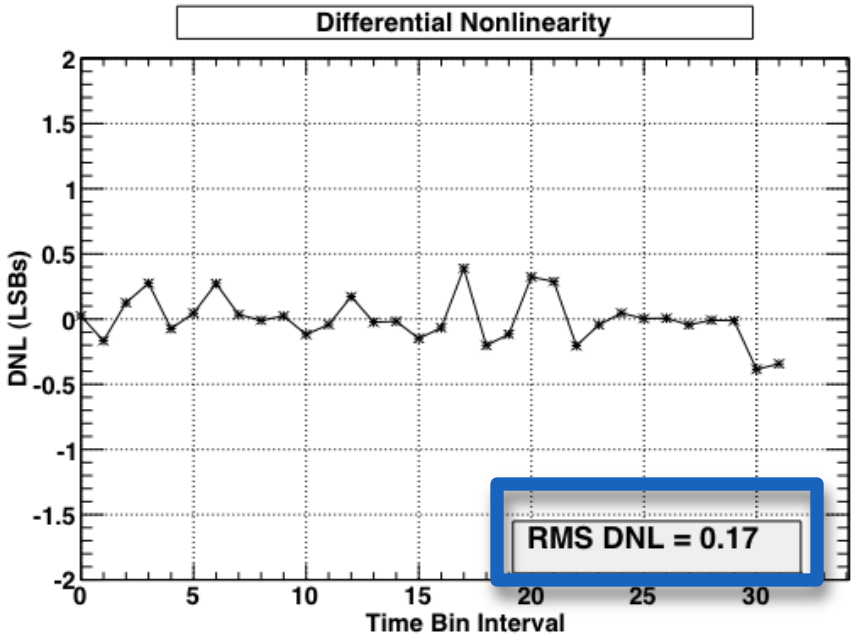


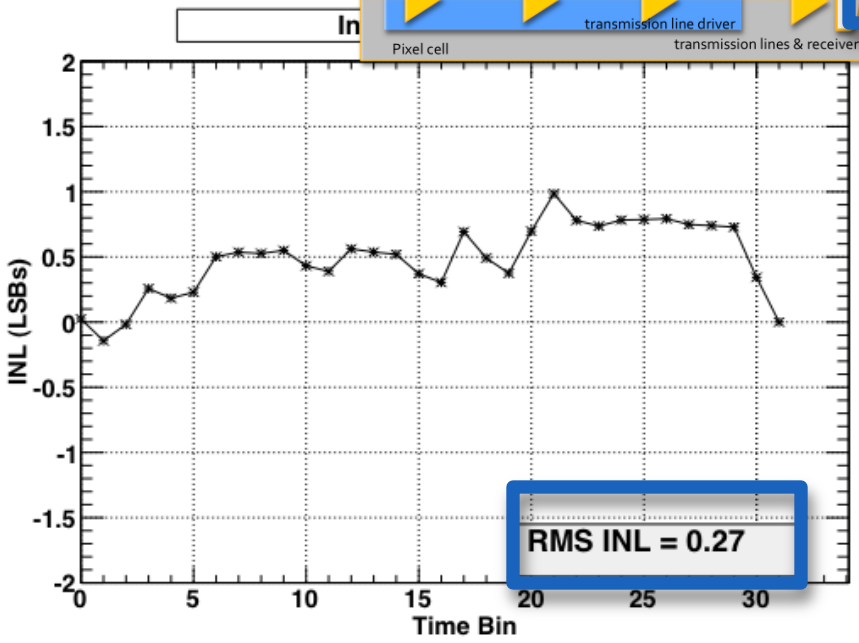
T1 jitter over input charge



TDC differential/integral non-linearity

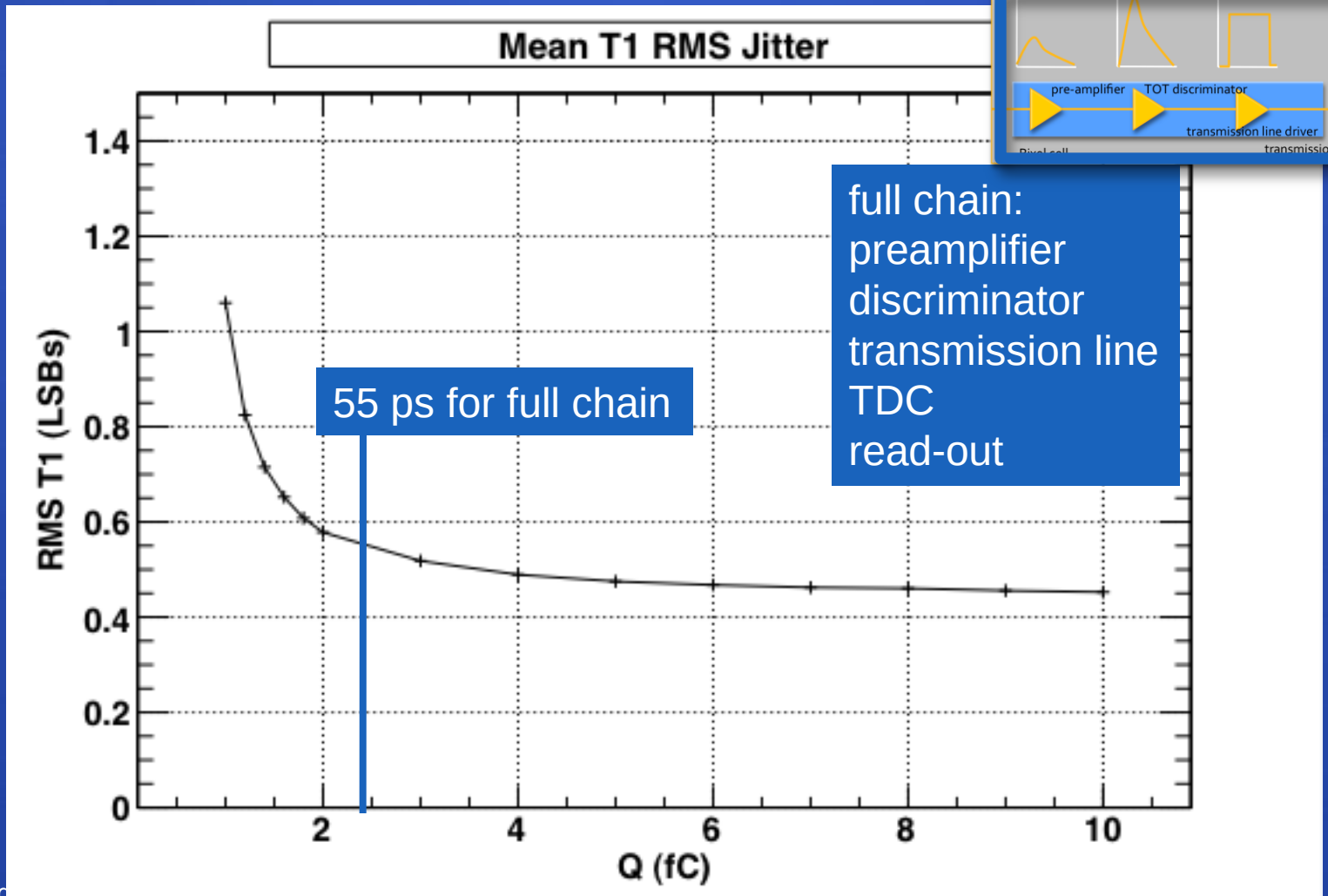




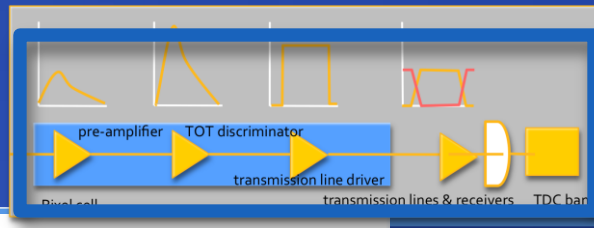


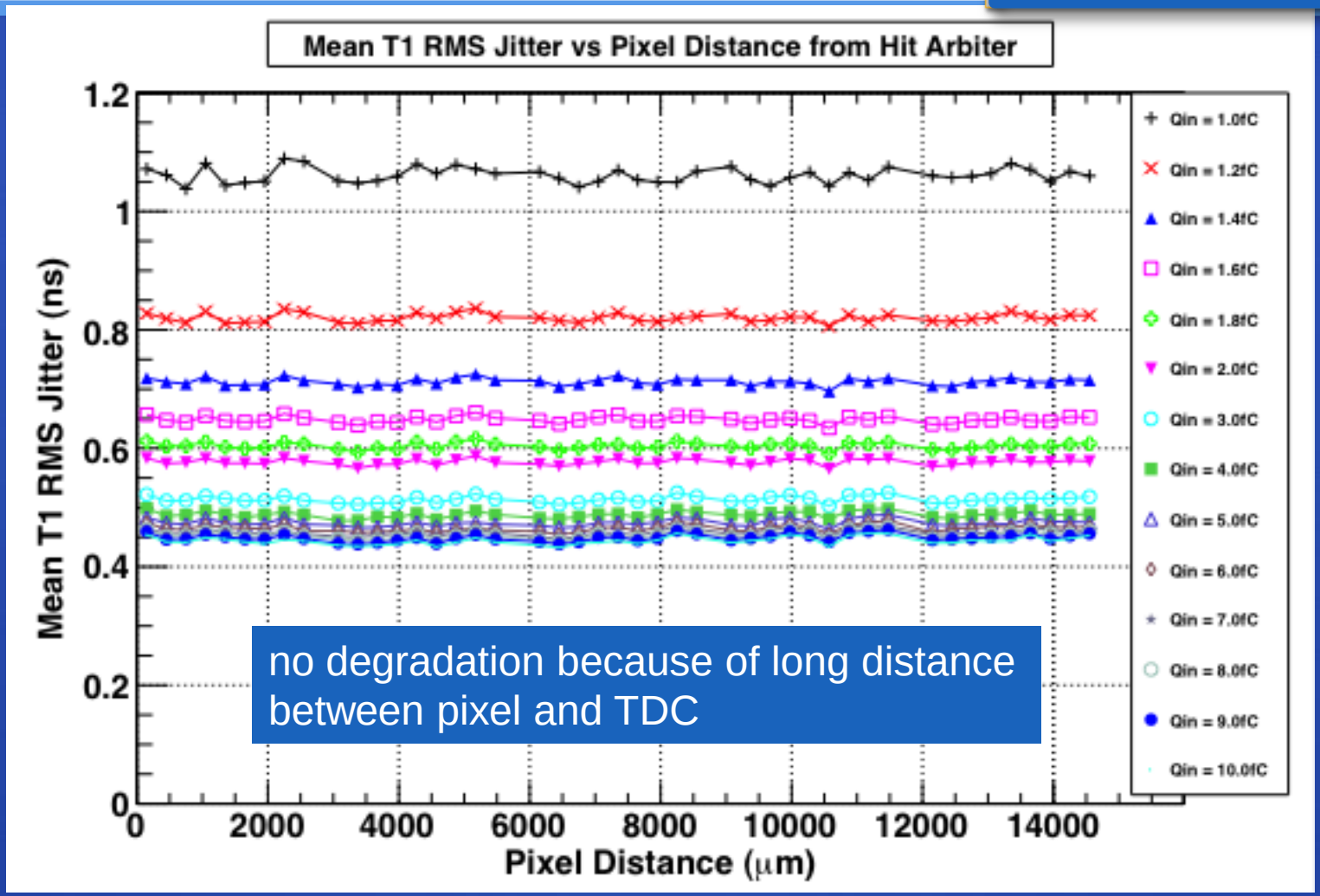
jitter on TDC 7 ps

Full chain T1 jitter over input charge @ 0.7 fC threshold



Full chain T1 rms jitter over pixel position





GTK cooling & electro-mechanical integration

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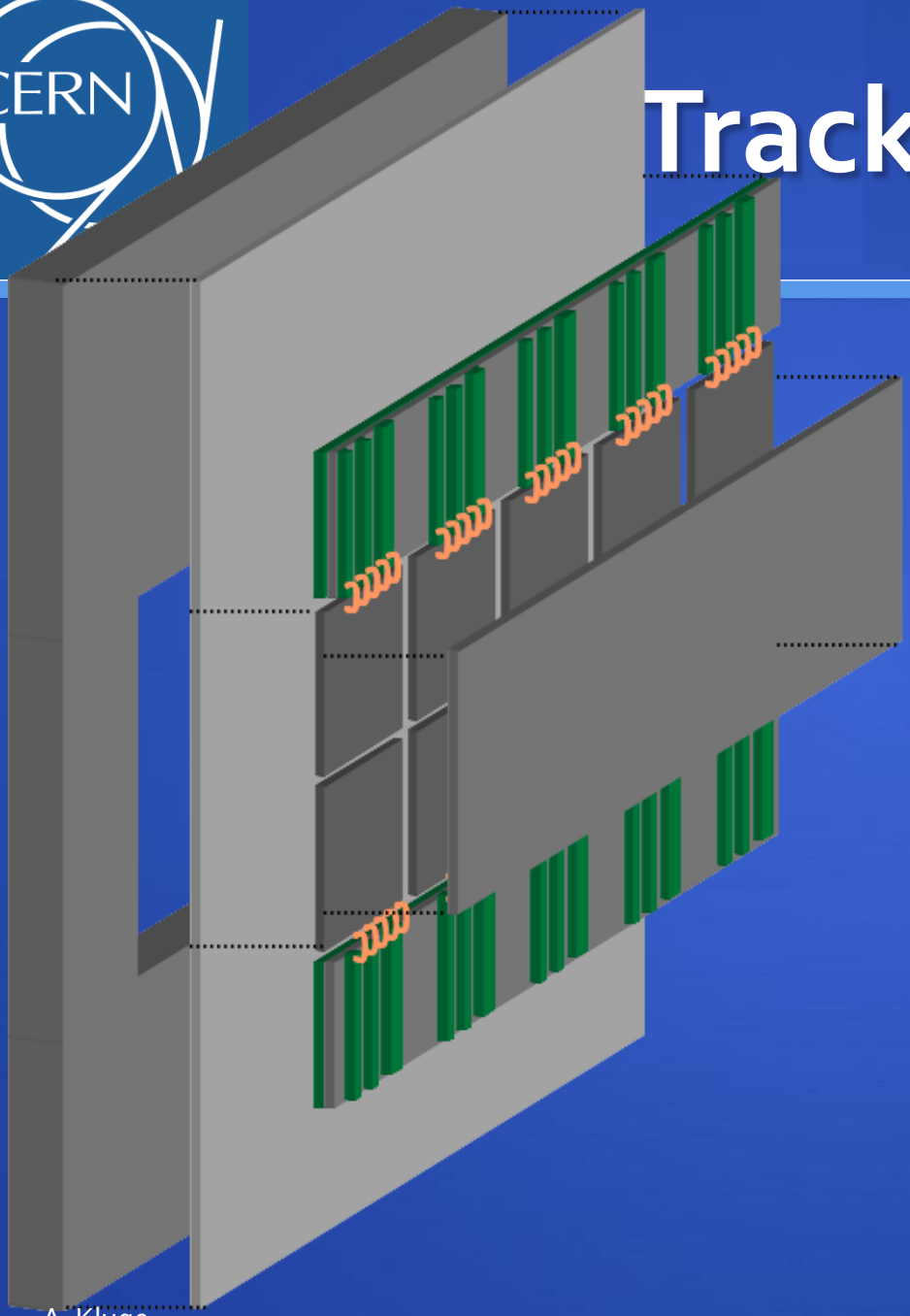
Tracker setup

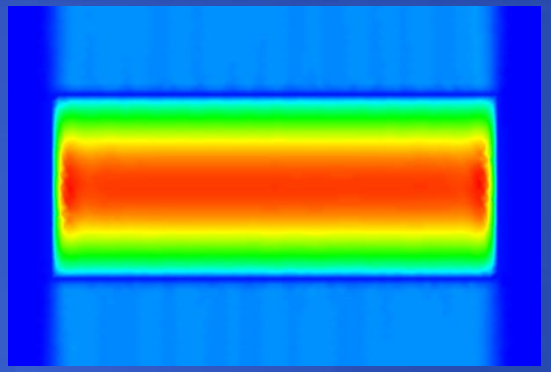


- Sensor&bonds: 0.24% X_0 (200 µm Silicon)
- RO chip: 0.11% X_0 (100 µm Silicon)
- Structure: 0.10% X_0 (100 µm Carbon fiber)
- Total: 0.45% X_0 uniform

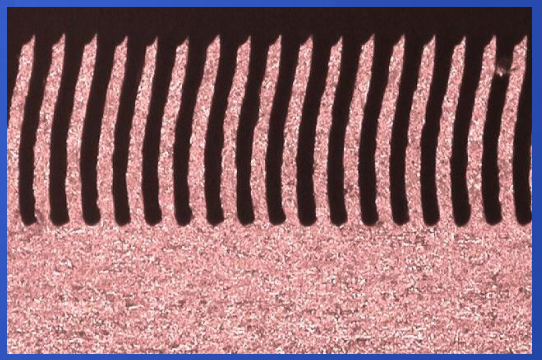
- Readout chip (12 x 20 mm), power < 3.2W per chip (2 W/cm^2)
- Vaccuum
- Radiation
- max. Temperature: 5 degree C, aiming for -20 degree C

Cooling systems under investigation

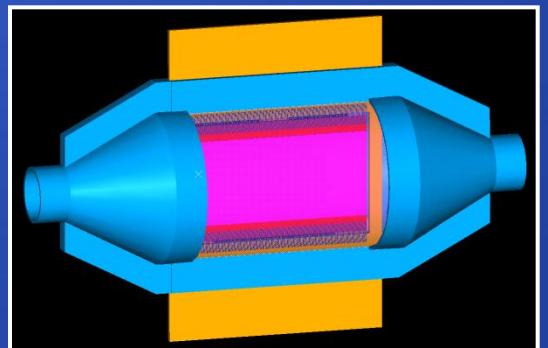
- carbon plate, conductive cooling



- micro channels



- convective cooling in a vessel



μ channel cooling

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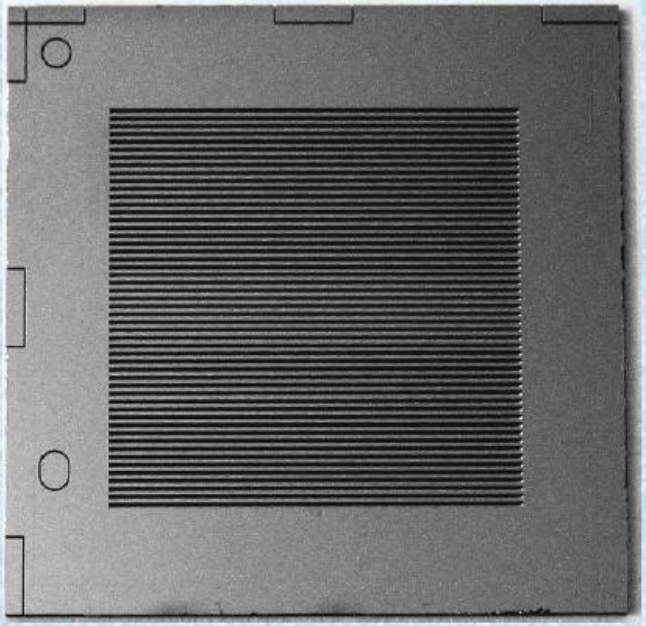
Micro channel cooling

ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE

LTCM/IBM Boiling Study: Microchannel Silicon Heat Sink

View of One Silicon Test Section Investigated with Refrigerants



Si: 31 x 31 x 1 mm^3
surface roughness 160 nm
134 parallel channels:
l = 20 mm, w = 67 µm, h = 680 µm,
separation 92 µm

255 W/cm^2

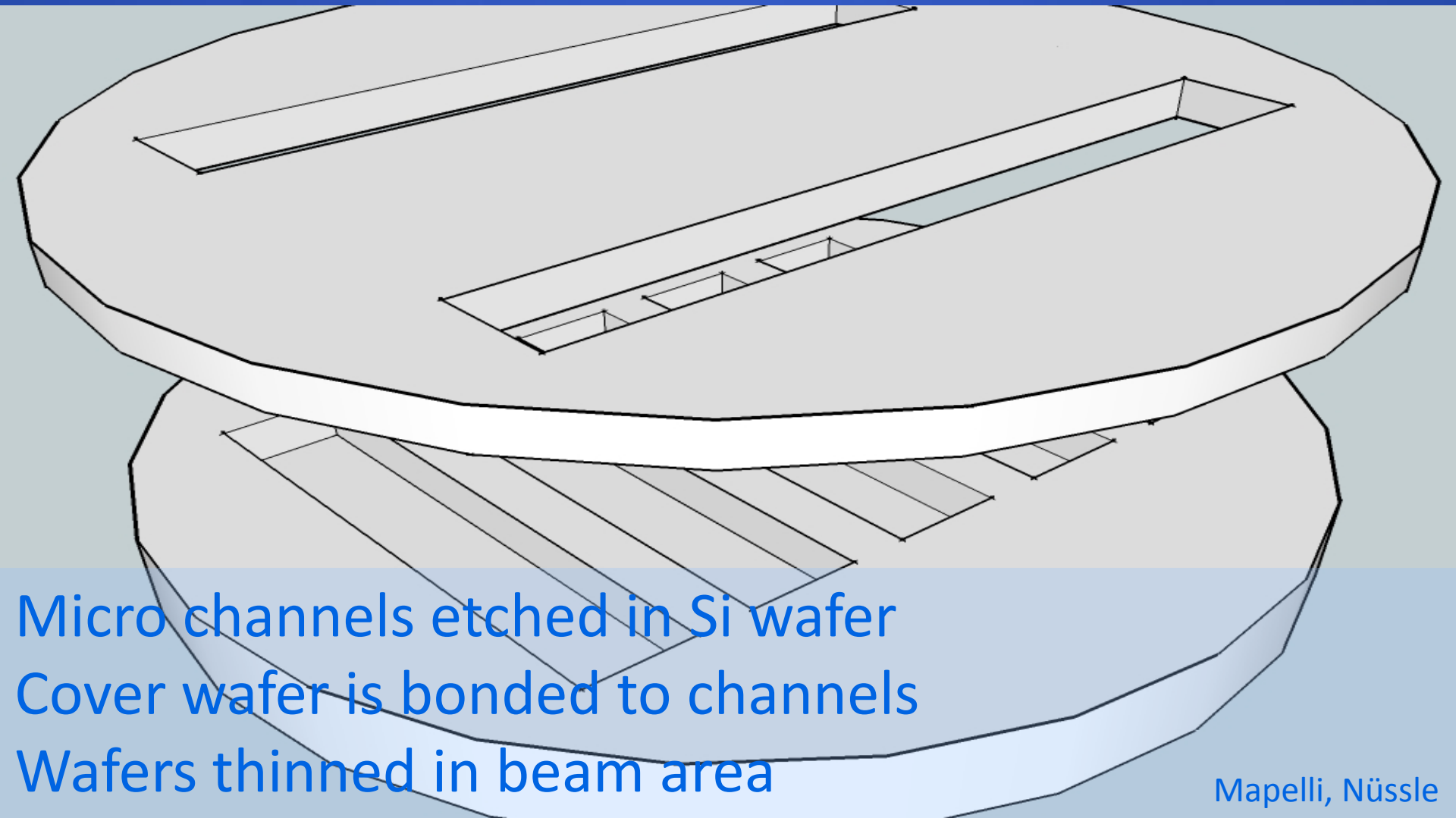
Top Side: Microchannels in Silicon **Bottom Side: Heater and Temp. Sensors**

Agostini et al.:To be published in Int. J. Heat Mass Transfer, in press.

Brief Introduction to Two-Phase Flow and Boiling in Microchannels

Prof. John R. Thome and Lorenzo Consolini
Laboratory of Heat and Mass Transfer
Faculty of Engineering Science
Ecole Polytechnique Fédérale de Lausanne
Lausanne, Switzerland

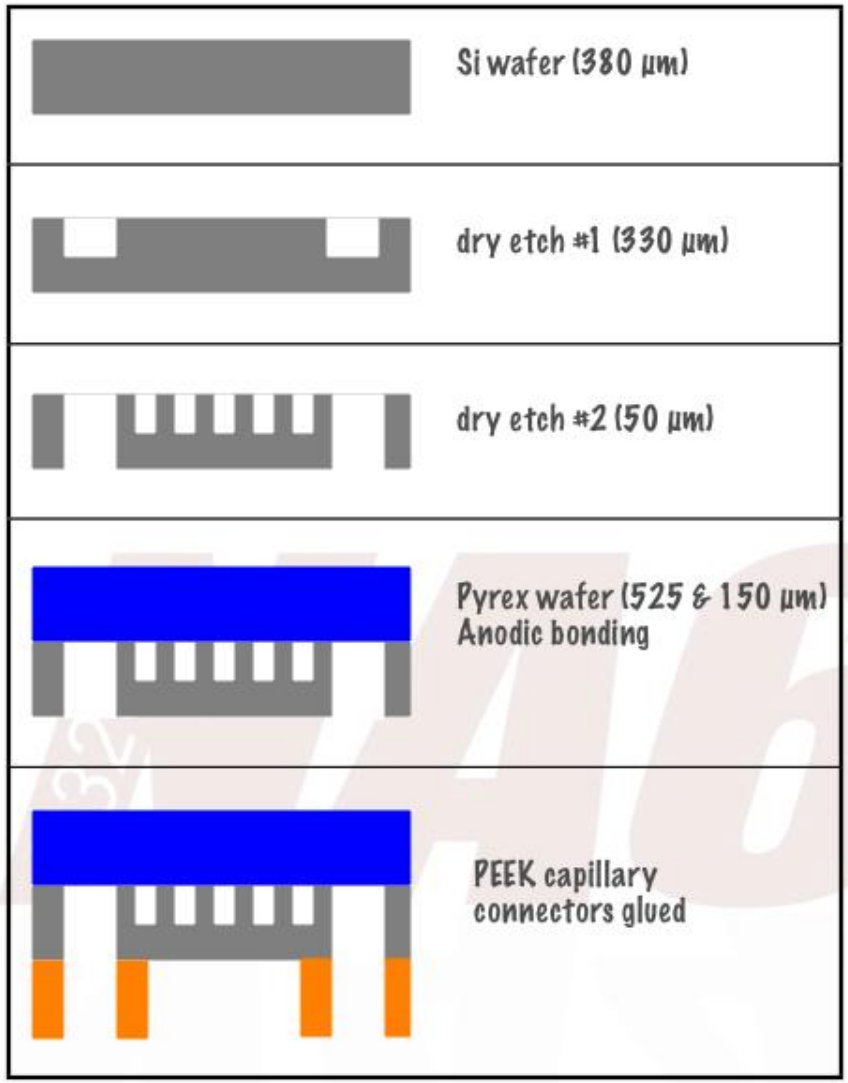
Production principle



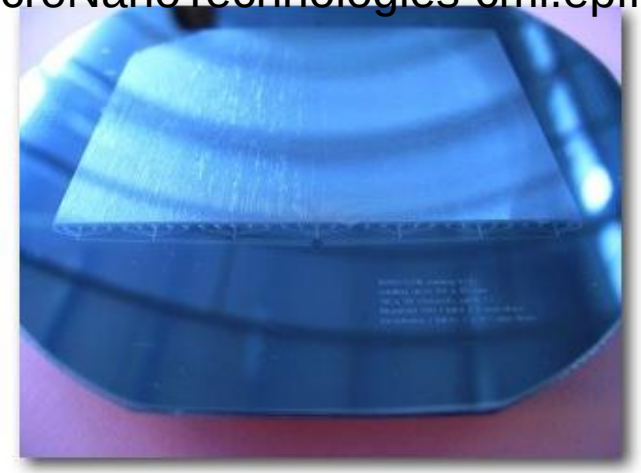
Micro channels etched in Si wafer
Cover wafer is bonded to channels
Wafers thinned in beam area

Mapelli, Nüssle

CERN / EPFL process - proto 3



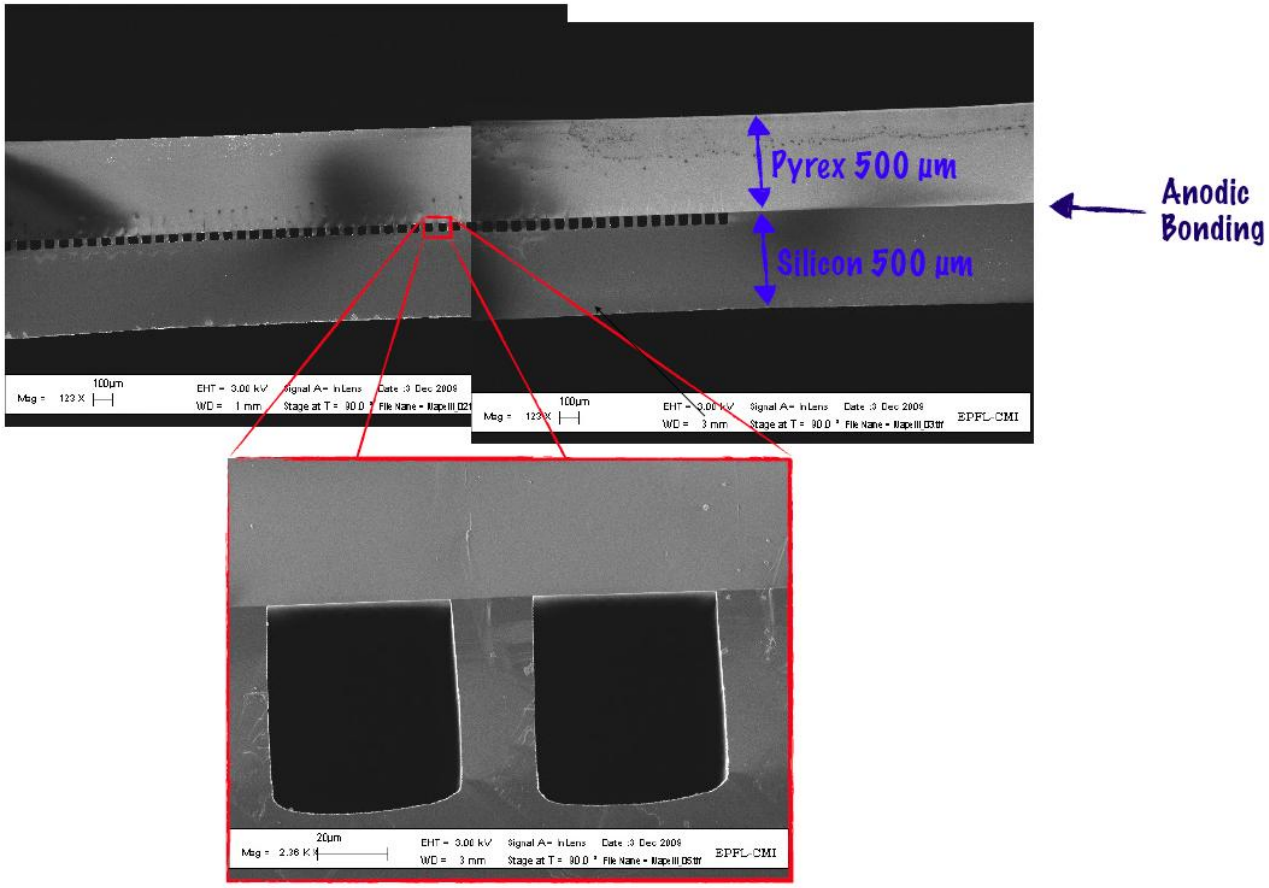
µchannel fabrication at EPFL-CMI (Center of MicroNanoTechnologies cmi.epfl,ch)



Nanoport assemblies N-333

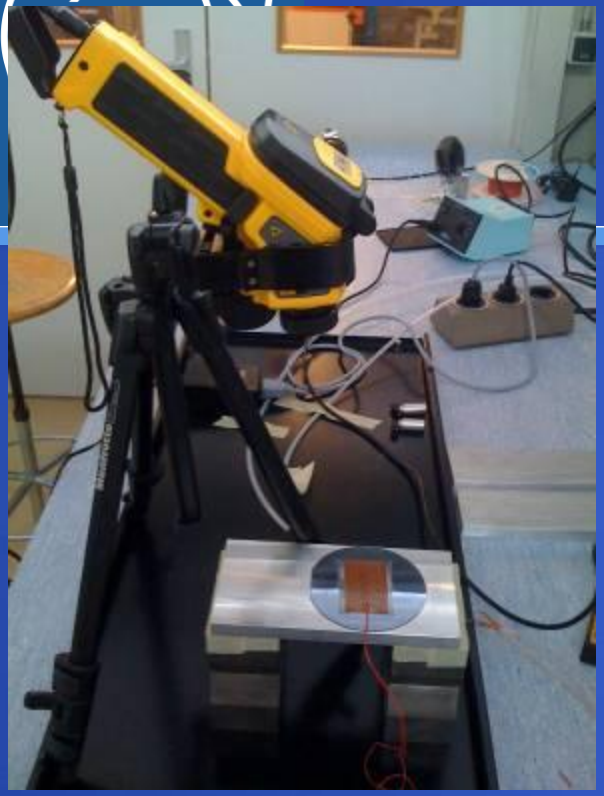
Silicon – Pyrex bonding

Si-Pyrex anodic bonding

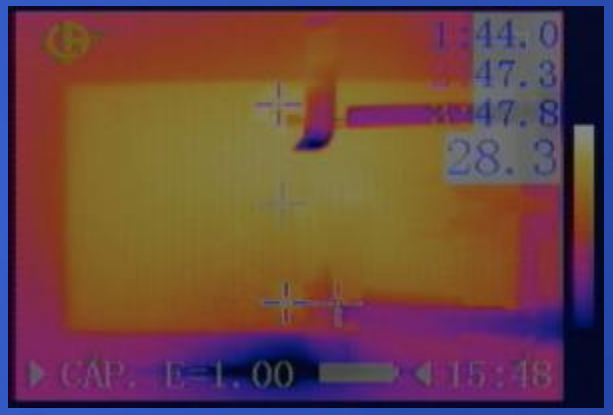


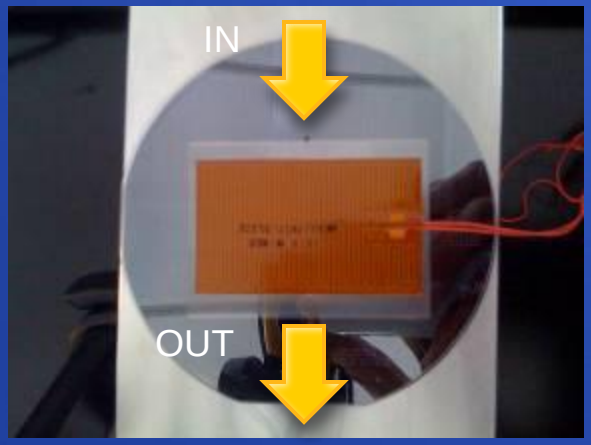
A. Mapelli - NA62-GTK µcool - 08 dec. 2009, CERN

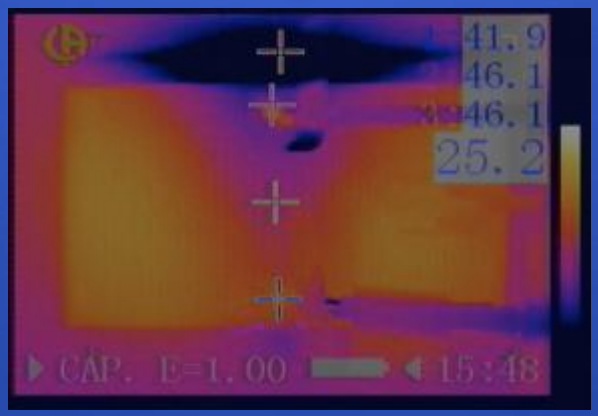
Cooling tests

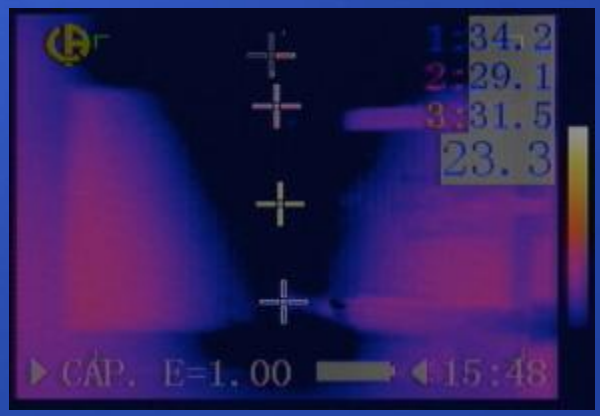


IR camera









cooling vessel for the GTK

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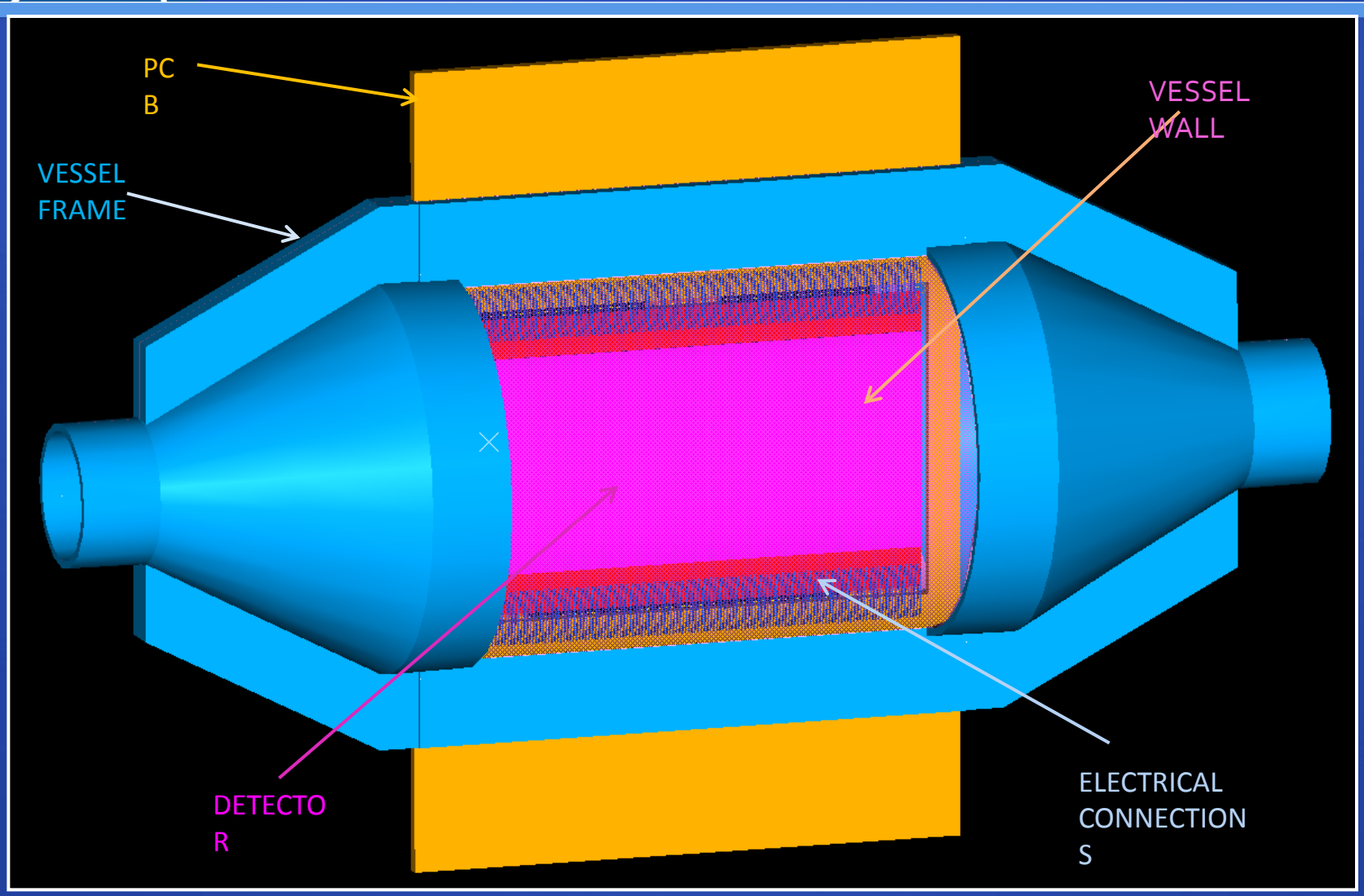
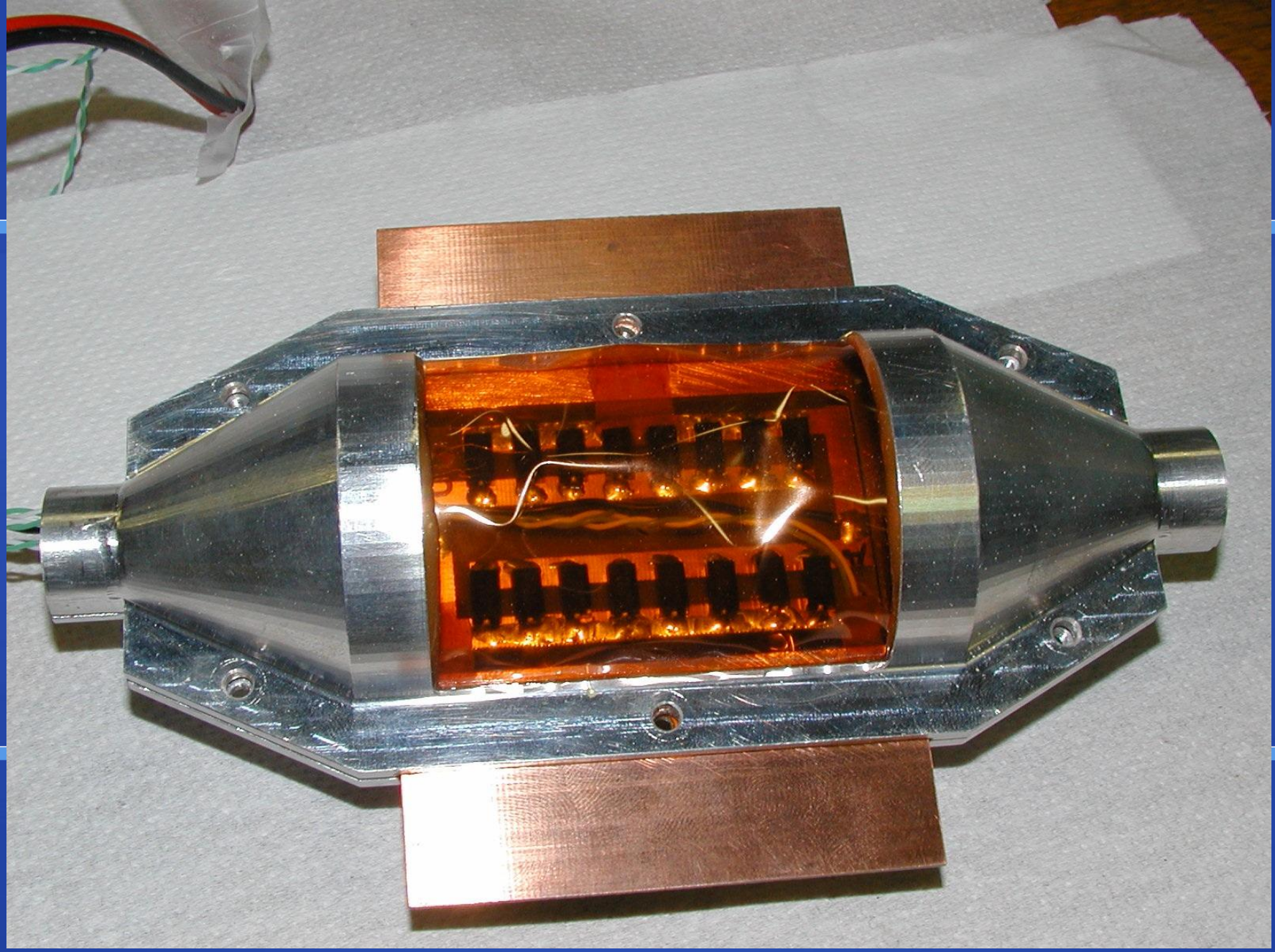
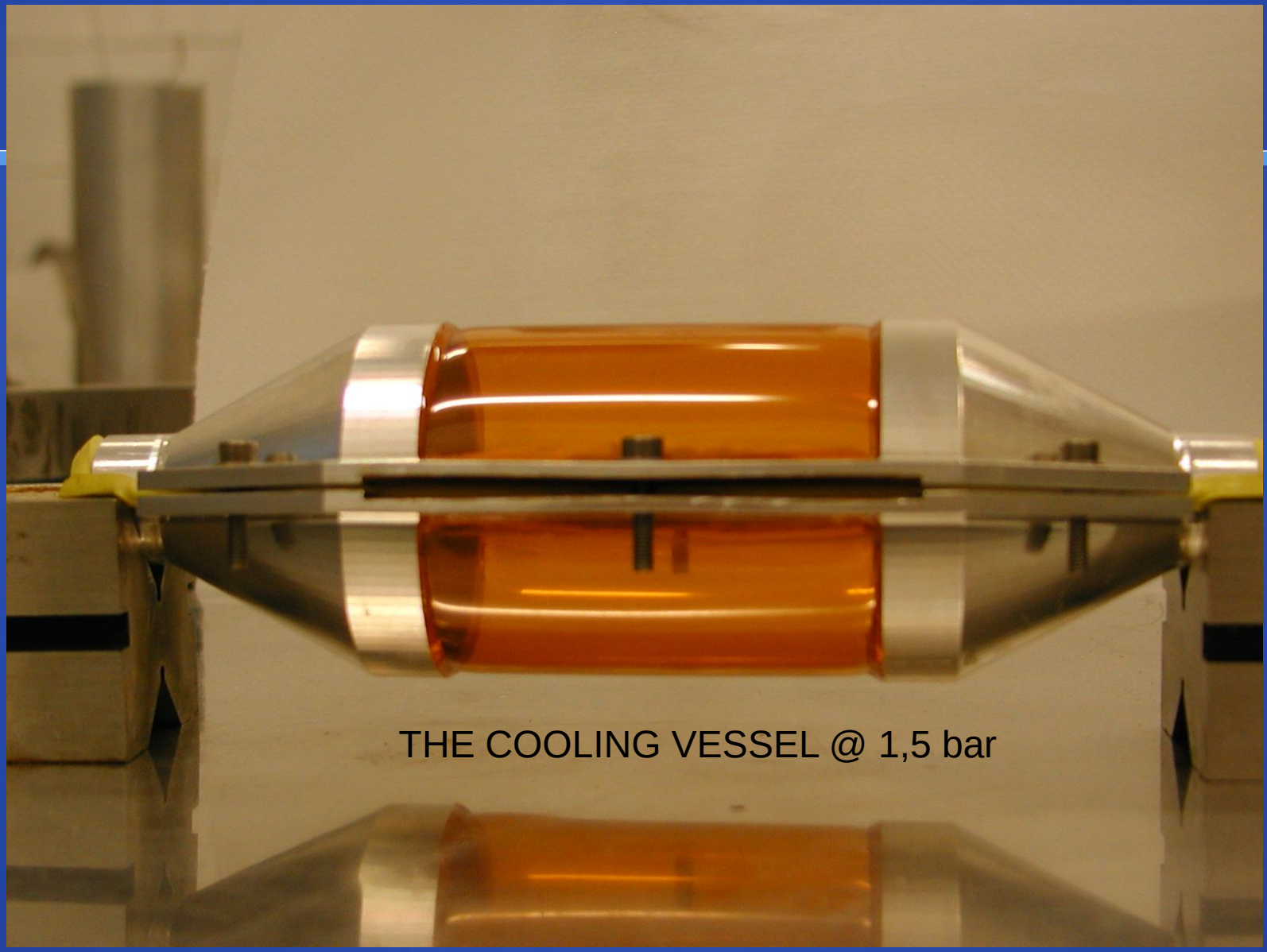
Cooling vessel





COOLING VESSEL

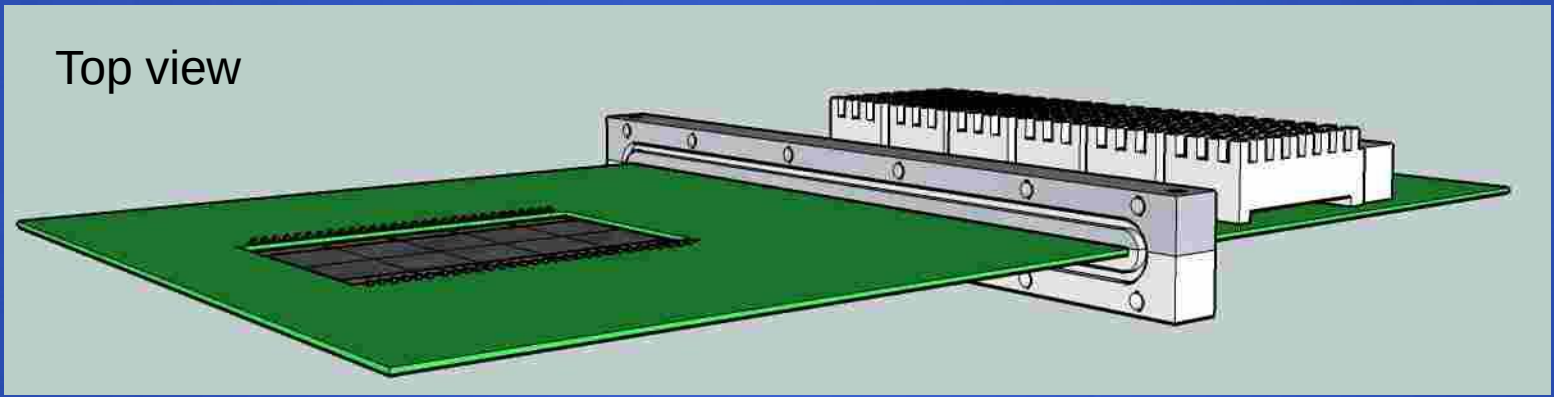


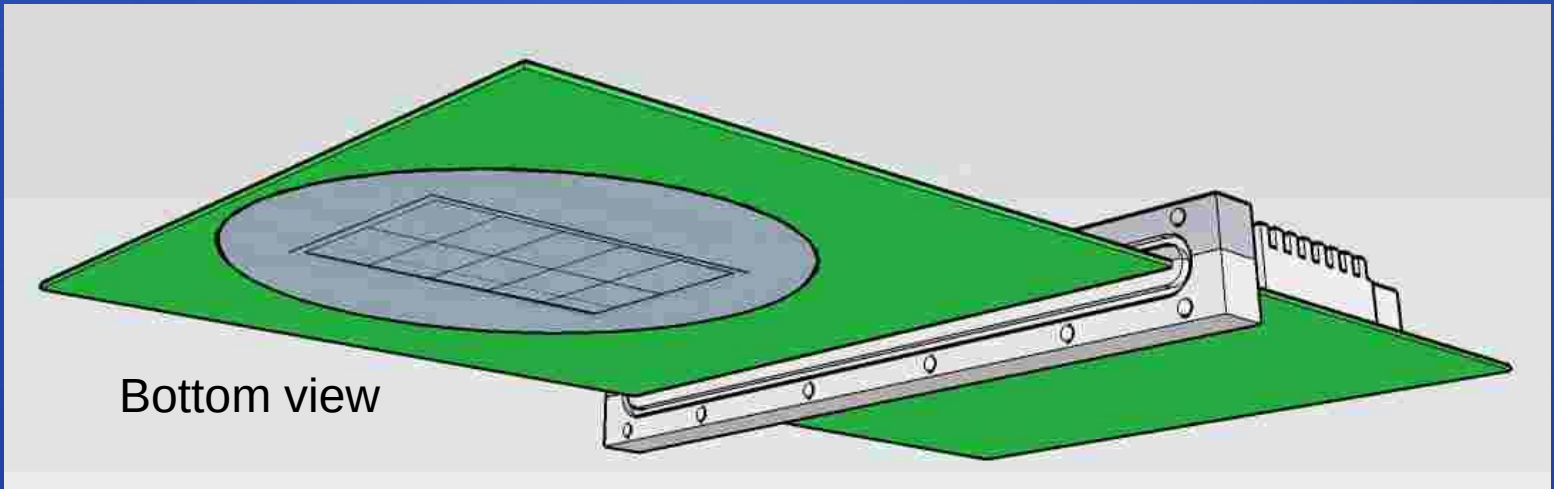
THE COOLING VESSEL @ 1,5 bar

Electro-mechanic integration

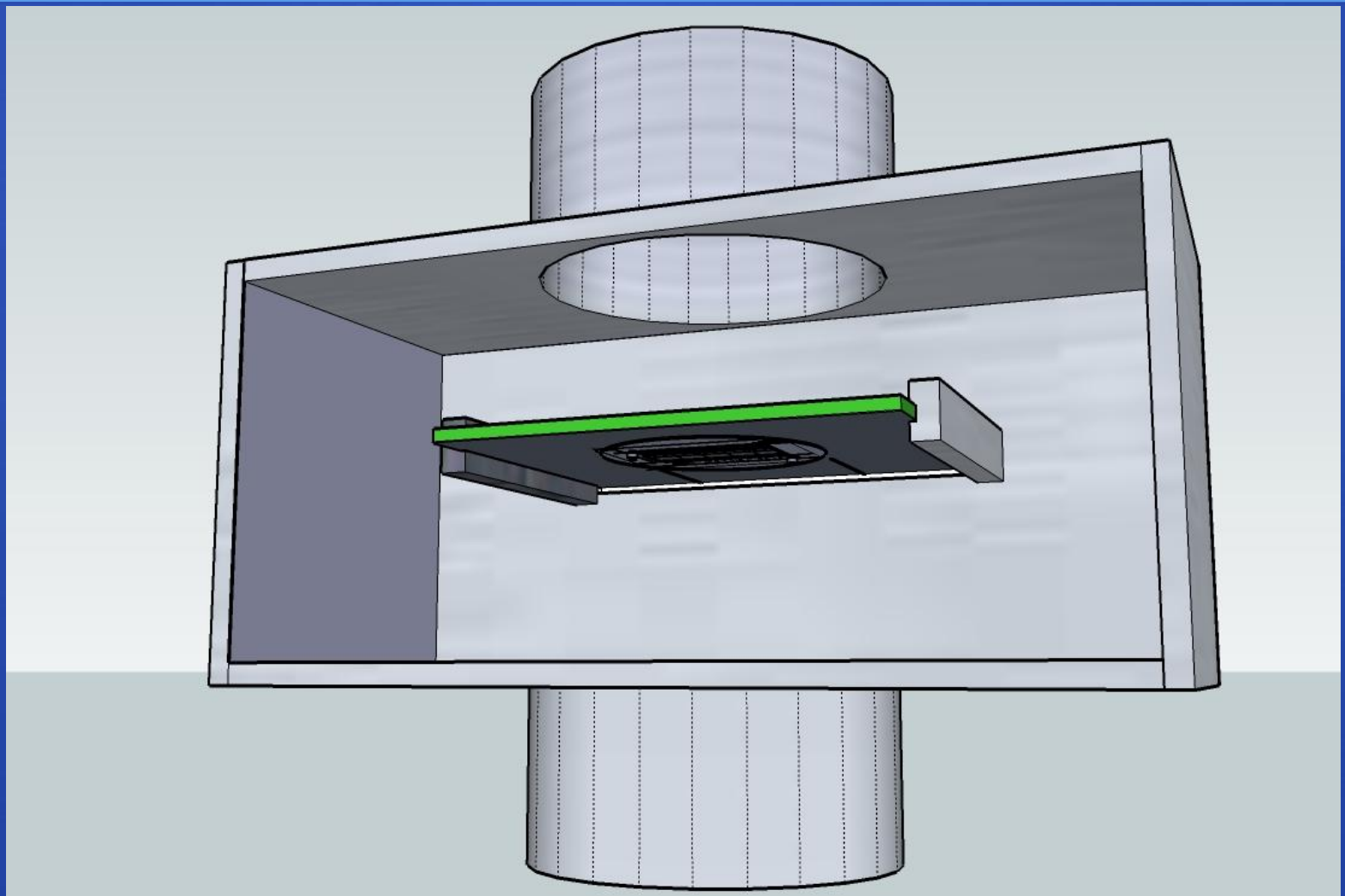
A. Kluge

GTK assembly carrier





Vessel & carrier board outside view



Next steps

- Bump bonding of sensor assembly
- Qualification of sensor assembly in laser/beam test
- Converge on one architecture
- Design of full pixel matrix
- In parallel electro-mechanical/cooling integration studies
- Installation end 2012

Summary

- 300 x 300 μm², 100 ps pixel detector for NA62 GigaTracker
- Specifications challenging, demanding integration, material budget, cooling and time stamping
- Demonstrator ASIC has shown very good results
  EOC - 55 ps full electronics chain jitter
- Integration design is advanced