ATLAS fast track trigger for SLHC
R. Brenner (on behalf of the ATLAS fast track trigger project)

- Motivation
- Atlas upgrade options
- Simulation studies
- Self seeded track trigger
- Region of interest seeded trigger
- Fast technologies for track trigger
- Conclusions
Motivations for a Level 1 track trigger

The performance of the muon trigger is limited by the resolution and granularity of the RPC system.

At SLHC one will search for rare decays and perform precision studies of processes. The ATLAS trigger performance should not degrade from today's trigger.

Single muon $10^{34}$

The performance of the muon trigger is limited by the resolution and granularity of the RPC system.
The performance of the electron trigger will depend on isolation achieved.

At SLHC one will search for rare decays and perform precision studies of processes. The ATLAS trigger performance should not degrade from today’s trigger.

The high granularity and resolution of the tracker can be used:

- To increases L1 selectivity (isolation)
- For early PID (electrons, muons)
- For lower and sharper trigger thresholds

We profit today from this in the LVL2 and HLT triggers so why not at LVL1?
Upgrade options

The ATLAS detector is rather accessible and several upgrade scenarios are studied to improve the L1 trigger for SLHC

Calorimeters

- Full readout of calorimeters (LAr and TileCal) → full granularity already at L1
- Topological triggers
- TileCal rear sampling in muon sector logic

Muon chambers

- New high rate and granularity muon chambers (small wheels)
- Muon Drift Tube (MDT) readout in L1 trigger

Trackers

- Fast TacKer (FTK), hardware track finder for ATLAS (at L1.5)
- ROI based track trigger at L1
- Self seeded track trigger at L1
Simulation studies of L1 track trigger

- All simulation presented here is done with present detector layout and at L\(\sim 10^{34}\)cm\(^{-2}\)s\(^{-1}\). Samples with higher luminosity are being prepared.
- Assume that the L1 at SLHC will be similar to current L2 at LHC.
- Study performance of calorimeters, muon chambers and trackers.
- Study robustness of trigger by degrading current L2
- Extract requirements for track trigger based on observables such as single e/\(\mu\) triggers (not on improvements of a specific physics analysis/searches)
- Understand requirements: \(\eta\) and \(\phi\) resolutions, pT, isolation etc.
Muon isolation

10 TeV MC (no pile-up):
- Signal: $Z \rightarrow \tau \tau \rightarrow \mu+X$ with $p_T > 20$ GeV
- Background: di-jet with $35 < p_T < 70$ GeV & $\mu$ with $p_T > 8$ GeV

Need to go down to $\sim 2$ GeV to achieve significant rejection

Study by: Elliot Lipeles, T. M. Hong, Doug Schaefer (Univ. of Pennsylvania)
Muon LVL1 trigger +ID LVL2 trigger $p_T$ smeared with 1.5, 2 and 2.5; eta by 0.1; phi by 0.05. No emulation of fake tracks → degrading performance of track trigger has small effect on quality

Study by: Yuto Komori (Univ. of Tokyo) and Kunihiro Nagano (KEK)
Self seeded track trigger with doublet layers

- Moderate pT dependent discrimination of hits using coincidences in closely spaced double layers
- High pT discrimination using coincidences between several doublet layers
- Has to operate at full BCO frequency (40 MHz)

![Diagram showing track trigger with doublet layers](image)

- **Barrel crosssection**
  - Track (low pT)
  - Track (hi pT)
  - Layer A
  - Layer B
  - Δr ~few mm
  - ΔR ~ 100 mm
  - Coincidences

- **Graphs**
  - Particle Count vs. pT (GeV)
  - Track impact vs. pT [GeV/c]
  - Keep ~1%
  - Keep ~0.1‰
ATLAS silicon strip design

- Basic design of silicon strip layers are after some modifications are well suited for triggering
  - Short- (~2.5cm), Long-strips (~10cm): length 1.2 m, width ~ 11 cm
  - Thickness ~ 3-5 mm
  - Laminate of core, electrical bus, sensors, hybrids, chips
  - Mass 2.26 (1.73)% X0 (34% core, 66% electrical+sensors)
Split chip approach for triggering

- Split the readout chip and add an embedded fine pitch interconnection. Analogue part near sensor to minimize noise, digital separated and connected top-bottom for coincidence logic.

Digital chip on hybrid x5

Bus cable

Sensor ~10 x 10 cm

Wrap around

Fine pitch interconnect

Wrap around

Analog chip on hybrid x10

ABCn
Binary readout

top

pipeline

bottom

n

n+1

pre-amp
disc

trigger

output

Analog chip

Digital chip
Summary split approach

- Consider effect of additional chips and interconnect material on the stave
- Compare to material estimates studied earlier as part of ongoing stave R&D
  - Effect of trigger components is not large
- Of potentially more concern are thermal and electrical interference
- Impact of axial/axial vs axial/stereo not yet known

<table>
<thead>
<tr>
<th>Stave</th>
<th>Flex SS</th>
<th>Flex LS</th>
<th>Flex LS + Trig</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>0.73</td>
<td>0.73</td>
<td>0.73</td>
</tr>
<tr>
<td>Module</td>
<td>1.49</td>
<td>0.96</td>
<td>1.07</td>
</tr>
<tr>
<td>Glue</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
</tr>
<tr>
<td>Total %Xo</td>
<td>2.26</td>
<td>1.73</td>
<td>1.84</td>
</tr>
</tbody>
</table>
Simulation results

The shift of hits between top and bottom layers separates low pT tracks from high pT. Example for 10cm long strips layer at R=1m. Doublet separation=4.5mm

Even with 400 pileup combinatorial background is small compared to correlated background

Study by: M. Garcia-Sciveres et al.

Combinatorial $\sim \frac{1}{\text{granularity}}$
Correlated $\sim$ material
Region of Interest seeded trigger

L0: $\Delta \phi = 0.2$, $\Delta \eta = 0.2$ at Calo $\Delta z = 40$ cm at beam line

- An L0 similar to the current L1-Calo and L1-Muon defines the regions of interest (Rols), no tracking information in Rol definition
- Rol defines and eta-phi region for strips and pixel information to be extracted, Rols about 1% of the detector/event
- L1 uses inner detector information from the Rols that were defined in L0
- Can also do a detailed correlation with outer detector
L0 implementation

- Calo and muon detectors provide a high rate L0 trigger with RoI information (500 kHz - 1MHz) with a latency < 3.2 µs, Regional Readout Request (R3)
- The L0 information is moved to a L1 buffer on the front-end chip
- Only L0 information from RoI is transferred off-detector
- Full detector readout after L1 trigger with latency 50-256 µs
The RoI trigger can be easily accommodated in present tracker. Design studies under way in the strip readout working group for its next prototype FE-chip, ABCN-130. RoI based trigger gives maximum flexibility with little impact on tracker design but requires a global TDAQ upgrade of ATLAS, with all detectors accepting long L1 trigger latency.
Advantages of RoI seeded trigger

- **Flexibility:**
  - any RoI driven processing possible at 1 MHz
  - Full tracking in RoI with 50-100 μs for algorithm, complexity limited by external computing
  - MDT information in RoIs at L1 (like μ-Fast algorithm in current L2)
  - EM and jet clustering and shower-shapes with full granularity
  - Refined track-shower matching

- **Decouples tracker geometry from trigger:**
  - Sophisticated trigger algorithms are implemented in external hardware (computers, associative memory,...) not in dedicated very fast L1 hardware.
  - Does not impose additional constraints on ID configuration i.e. layers, granularity,...
Template method: Fast TracKer (FTK), trigger at L1.5

- Process all data from pixels and SCT on a L1A
- Fast processing in custom made dedicated Associative Memory chips (AM)
- Template method with $10^9$ patterns (roads) to see the silicon hits leaving the detector at full speed
- Design demonstrated by simulation to work up to $L = 3 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$
- Will not help the L1 problem at SLHC but the technology is interesting for SLHC
- Project has submitted a Technical Proposal waiting for approval for a TDR (deployment 2016?)
Fast template method with CAMs

- Match pattern in strips or pixels with precomputed templates
- Templates are stored in Ternary-CAMs (Column Accessible Memory) providing storage and fast match
- Every part of the detector is special, no symmetry exploited
- Main questions
  - How many templates depending on detector geometry?
  - Fake rate?
  - Hardware implementation?
- Applicable for both ROI and Self Seeded track trigger
Simulation studies of patterns and fake rates

- Results of “toy MC” + reconstruction (barrel only), minimum pT of 10 GeV
- SLHC upgrade tracker layout

### No redundancy

<table>
<thead>
<tr>
<th>design</th>
<th>(N_{\text{total}}) [billion]</th>
<th>100</th>
<th>200</th>
<th>400</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 shorts (3/3)</td>
<td>3</td>
<td>100</td>
<td>750</td>
<td>6000</td>
</tr>
<tr>
<td>1 pixel* 3 shorts (4/4)</td>
<td>20</td>
<td>10</td>
<td>125</td>
<td>2000</td>
</tr>
<tr>
<td>2 pixel* 3 shorts (5/5)</td>
<td>80</td>
<td>1</td>
<td>30</td>
<td>1000</td>
</tr>
<tr>
<td>5 shorts (5/5)</td>
<td>230</td>
<td>0.01</td>
<td>0.3</td>
<td>10</td>
</tr>
<tr>
<td>5 shorts last layer at 86 cm (5/5)</td>
<td>100</td>
<td>0.01</td>
<td>0.3</td>
<td>10</td>
</tr>
</tbody>
</table>

### Redundancy

<table>
<thead>
<tr>
<th>design</th>
<th>(N_{\text{total}}) [billion]</th>
<th>100</th>
<th>200</th>
<th>400</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 shorts last layer at 86 cm (4/5)</td>
<td>160</td>
<td>5</td>
<td>60</td>
<td>1000</td>
</tr>
<tr>
<td>3 short doublets (5/6)</td>
<td>100</td>
<td>0.05</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>3 short doublets (6 cm spacing) (5/6)</td>
<td>30</td>
<td>0.01</td>
<td>0.3</td>
<td>10</td>
</tr>
</tbody>
</table>

pixel*: z-granularity coarsened from 250 μm to 2.4 cm.

Would allow for lower pT cut and standalone trigger (low pile-up)

Study by: S. Schmitt, A. Schoening (Uni Heidelberg).
Wireless data transfer

- 60 GHz technology offers a data transfer BW of 5-10 Gbit/s

- Technology compatible with tracker
  - Size of components are small, low mass (antenna ~1 cm², chip ~few mm²)
  - Power consumption is low ex. 90nm CMOS Low-Power 60GHz Transceiver (Marcu et al.) 170mW in transmit mode and 138mW in receive mode

- Allow radial data transfer for topological trigger
Conclusions

- Event selection at L1 will be a challenge at SLHC
- ATLAS is investigating several upgrade options to improve the L1 trigger
- A large improvement in trigger rates, selectivity, thresholds seen if tracking information used in L1 trigger
- ATLAS is investigating two basic schemes to readout tracking information for L1 trigger
- Data bandwidth and trigger latency is a challenge for L1 trigger. New solutions in data transfer and processing are investigated.

More information on fast track trigger in “Workshop on Intelligent Trackers”, Feb 2010:

- [http://indico.cern.ch/conferenceDisplay.py?confId=68677](http://indico.cern.ch/conferenceDisplay.py?confId=68677)
- Proceeding to appear in JINST (http://jinst.sissa.it/jinst/common/JINST_proceedings6.jsp)
Back-up
## RoI data bandwidth calculation

### Inputs:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>Beam Crossing Rate</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Desired L0 Rate</td>
<td>500 KHz - 1 MHz</td>
</tr>
<tr>
<td>Desired L1 Rate</td>
<td>20 KHz (min) - 100 KHz (max)</td>
</tr>
<tr>
<td>Fraction of Data in RoI</td>
<td>2% (min) - 10% (max)</td>
</tr>
<tr>
<td>Number of L0 buffers</td>
<td>≈ 128 - 256</td>
</tr>
<tr>
<td>Number of L1 buffers</td>
<td>≈ 50 - 256</td>
</tr>
</tbody>
</table>

### Latencies:

<table>
<thead>
<tr>
<th>Latency</th>
<th>Calculation</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0 latency</td>
<td>( \frac{L0 \text{ buffer size}}{\text{Beam Crossing Rate}} ) = 3.2-6.4 , \mu s</td>
</tr>
<tr>
<td>L1 latency</td>
<td>( \frac{L1 \text{ buffer size}}{L0 \text{ Accept Rate}} ) = 50-256 , \mu s</td>
</tr>
</tbody>
</table>

### Data Output Bandwidth:

Bandwidth  

\( \text{full-event @ L1 Rate} + \text{RoI data @ L0 Rate} \)

\( \approx ((20-100) \, \text{KHz} + (2\%-10\%) \times 1 \, \text{MHz}) \) full-events

\( \approx 40 \, \text{KHz} - 200 \, \text{KHz} \) full-events

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Required bandwidth depends primarily on L1 rate and RoI size.
Data bandwidth self-seeded

• “Natural” bandwidth given by standard 100kHz L1A.
  – This is 0.25% of raw sensor hits (100kHz/40Mhz)
• Each doublet layer needs ~5x natural BW for THAT layer
  – 1% + 0.25% of raw hits instead of just 0.25%
• Assuming 2 doublet layers and 9 hits total, this results in
  roughly double the natural BW for the whole detector-
  same as ROI
• Final answer depends on optimization-
  – What momentum threshold (Δphi cut) is desired
  – How little mass can be achieved
  – How is the mass distributed