



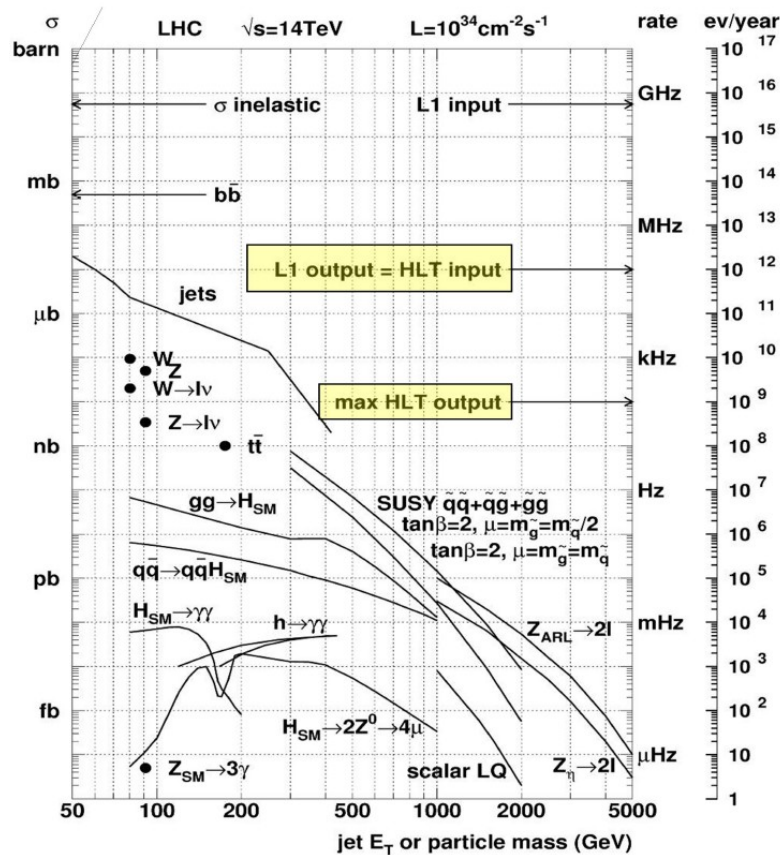
ATLAS fast track trigger for SLHC

R. Brenner (on behalf of the ATLAS fast track trigger project)

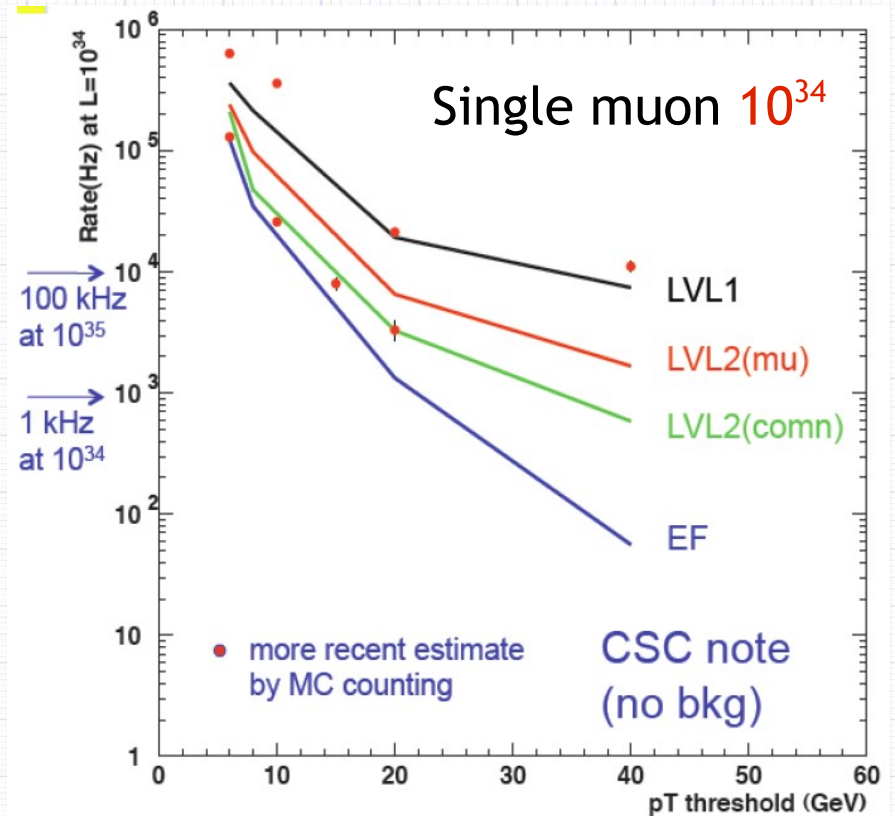
- Motivation
- Atlas upgrade options
- Simulation studies
- Self seeded track trigger
- Region of interest seeded trigger
- Fast technologies for track trigger
- Conclusions



Motivations for a Level 1 track trigger



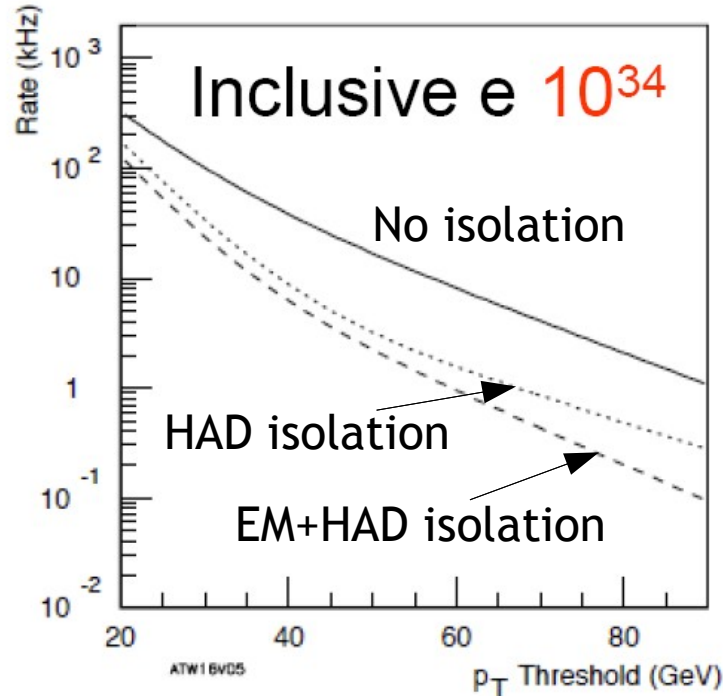
At SLHC one will search for rare decays and perform precision studies of processes. The ATLAS trigger performance should not degrade from today's trigger.



The performance of the muon trigger is limited by the resolution and granularity of the RPC system.



Motivation cont.



The performance of the electron trigger will depend on isolation achieved

At SLHC one will search for rare decays and perform precision studies of processes. The ATLAS trigger performance should not degrade from today's trigger.

The high granularity and resolution of the tracker can be used:

- To increase L1 selectivity (isolation)
- For early PID (electrons, muons)
- For lower and sharper trigger thresholds

We profit today from this in the LVL2 and HLT triggers so why not at LVL1?



Upgrade options

- The ATLAS detector is rather accessible and several upgrade scenarios are studied to improve the L1 trigger for SLHC

Calorimeters

Technical Proposal

- Full readout of calorimeters (LAr and TileCal) → full granularity already at L1
- Topological triggers
- TileCal rear sampling in muon sector logic

Muon chambers

- New high rate and granularity muon chambers (small wheels)
- Muon Drift Tube (MDT) readout in L1 trigger

Trackers

Technical Proposal

- Fast TackEr (FTK), hardware track finder for ATLAS (at L1.5)
- ROI based track trigger at L1
- Self seeded track trigger at L1



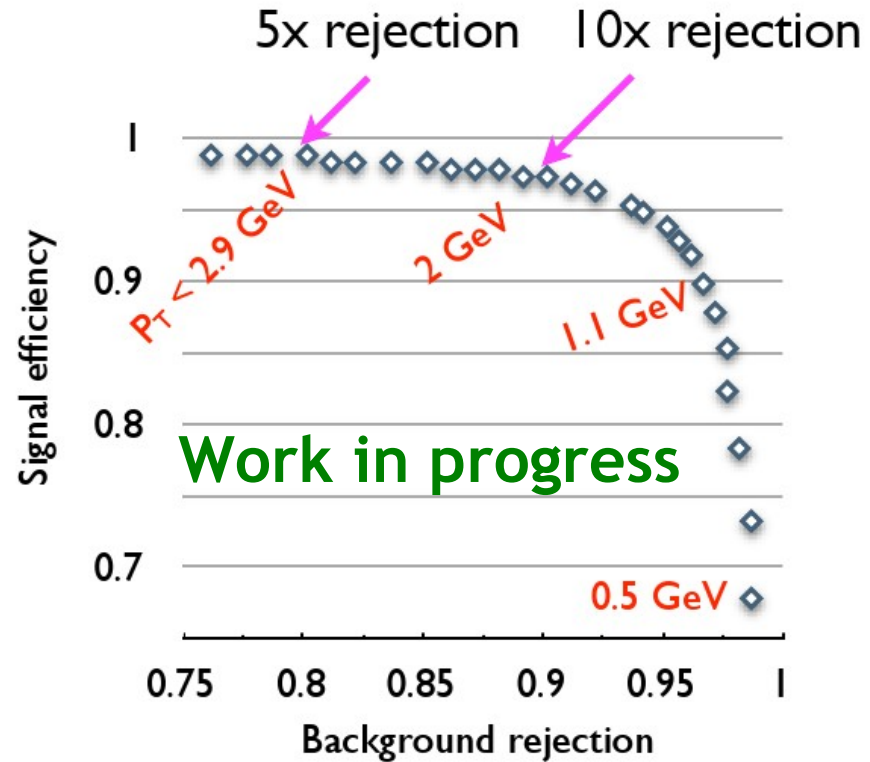
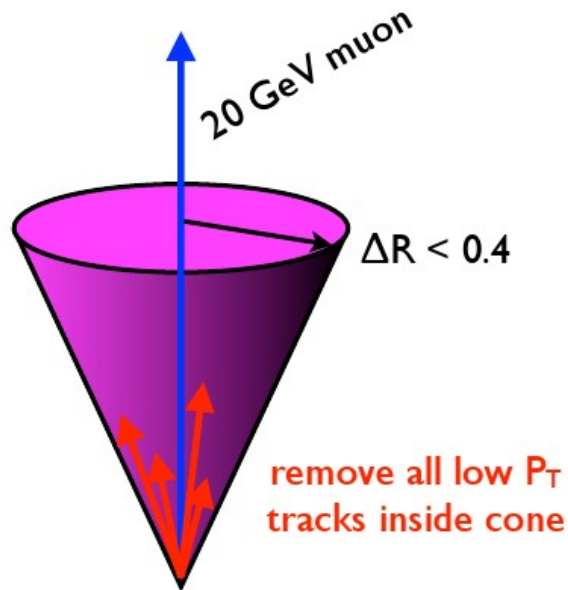
Simulation studies of L1 track trigger

- All simulation presented here is done with present detector layout and at $L \sim 10^{34} \text{cm}^{-2}\text{s}^{-1}$. Samples with higher luminosity are being prepared.
- Assume that the L1 at SLHC will be similar to current L2 at LHC.
- Study performance of calorimeters, muon chambers and trackers.
- Study robustness of trigger by degrading current L2
- Extract requirements for track trigger based on observables such as single e/μ triggers (not on improvements of a specific physics analysis/searches)
- Understand requirements: η and φ resolutions, p_T , isolation etc.



Muon isolation

Isolated muon



- 10 TeV MC (no pile-up):

- Signal: $Z \rightarrow \tau\tau \rightarrow \mu+X$ with $p_T > 20$ GeV

- Background: di-jet with $35 < p_T < 70$ GeV & μ with $p_T > 8$ GeV

Need to go down to ~2 GeV to achieve significant rejection

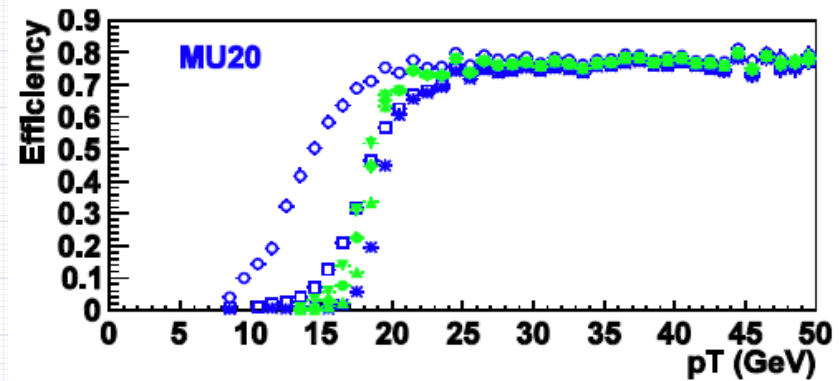
Study by: Elliot Lipeles, T. M. Hong, Doug Schaefer (Univ. of Pennsylvania)



Muon + track trigger quality

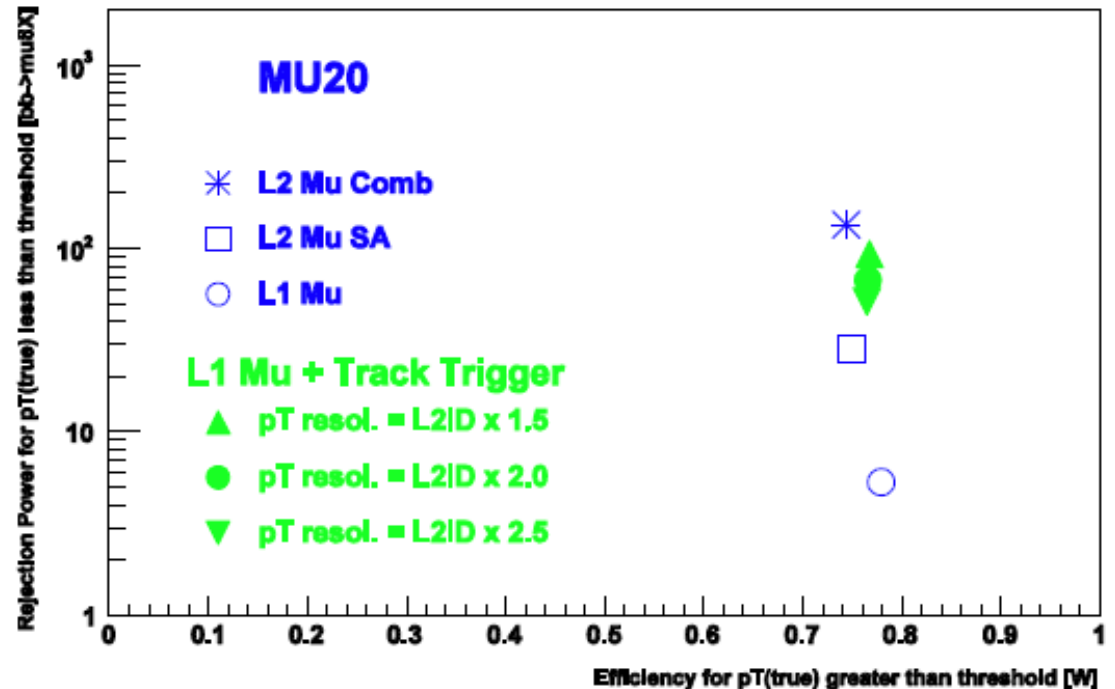
Muon LVL1 trigger +ID LVL2
trigger pT smeared with 1.5, 2
and 2.5; eta by 0.1; phi by 0.05.
No emulation of fake tracks

→ degrading performance of
track trigger has small effect
on quality



Trigger turn-on curve

Efficiency vs. rejection

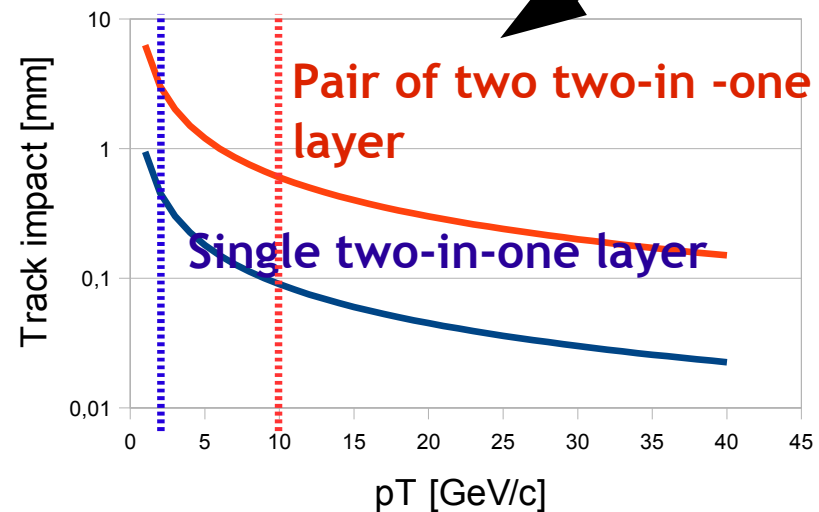
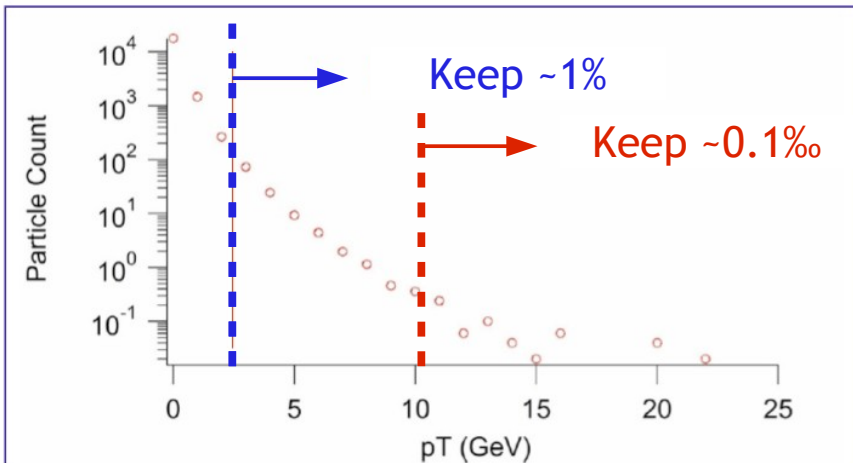
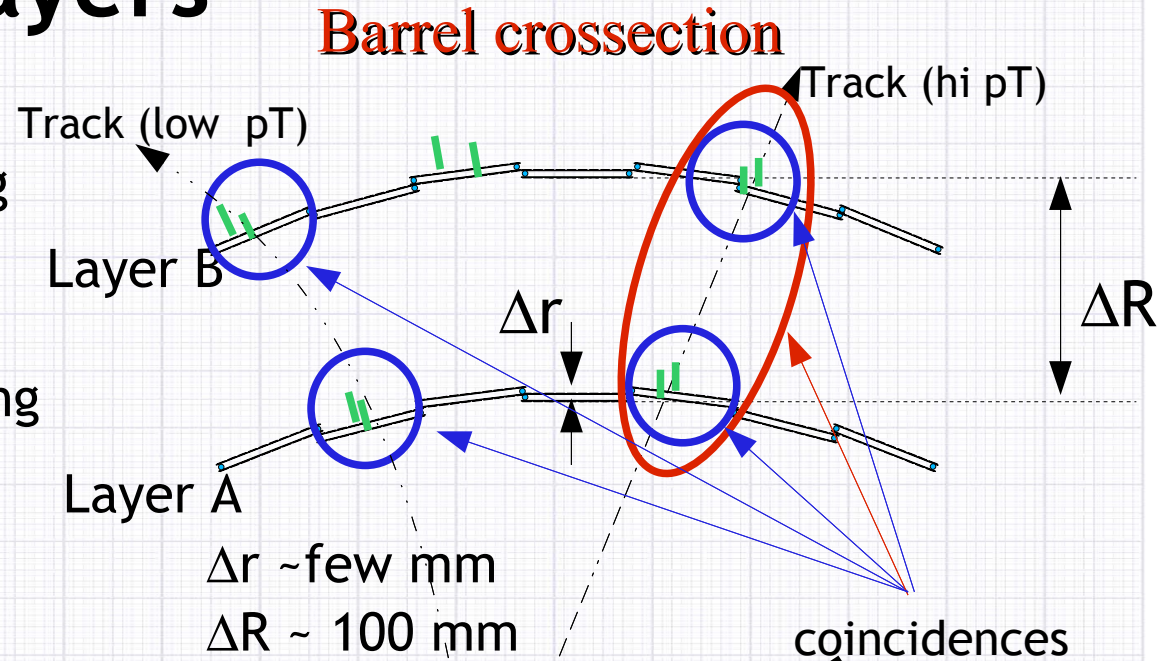


Study by: Yuto Komori (Univ. of Tokyo) and Kunihiro Nagano (KEK)



Self seeded track trigger with doublet layers

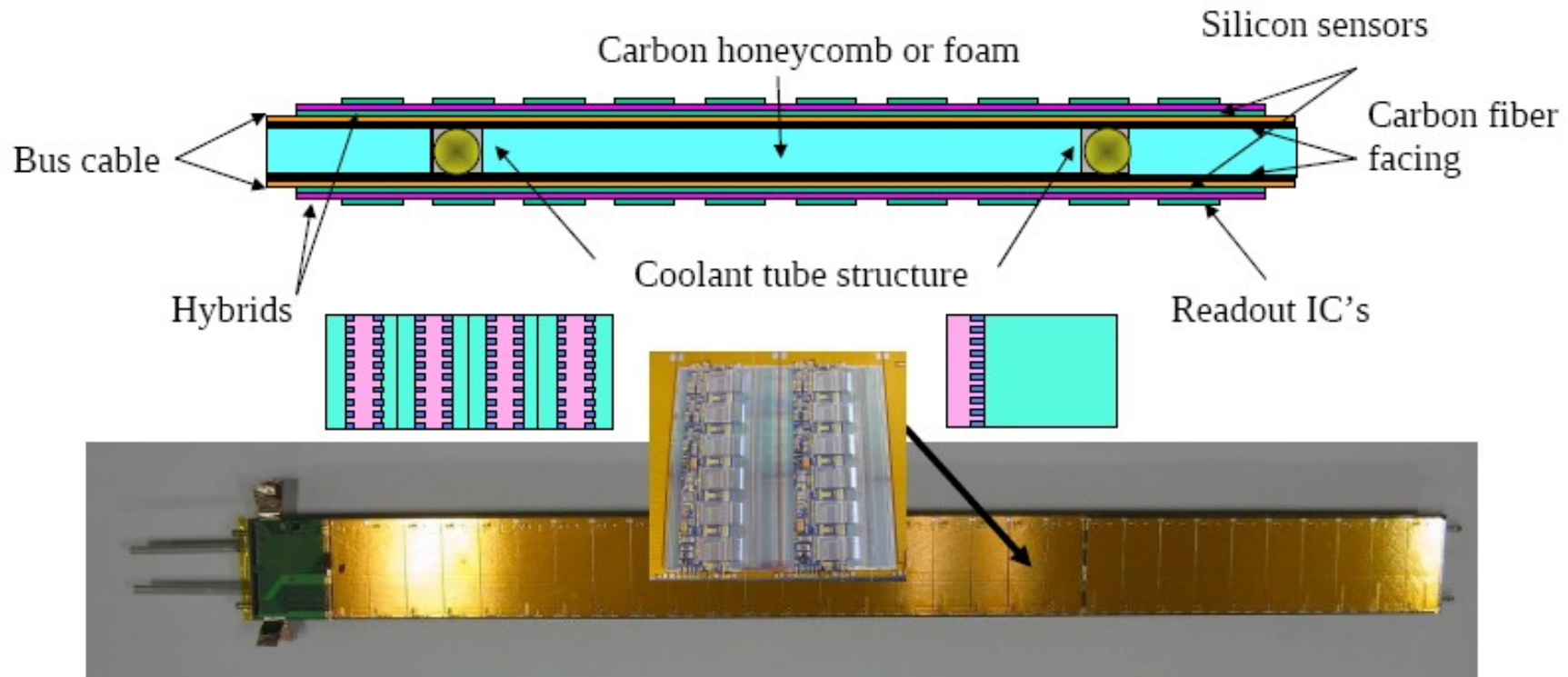
- Moderate p_T dependent discrimination of hits using coincidences in closely spaced double layers
- High p_T discrimination using coincidences between several doublet layers
- Has to operate at full BCO frequency (40 MHz)





ATLAS silicon strip design

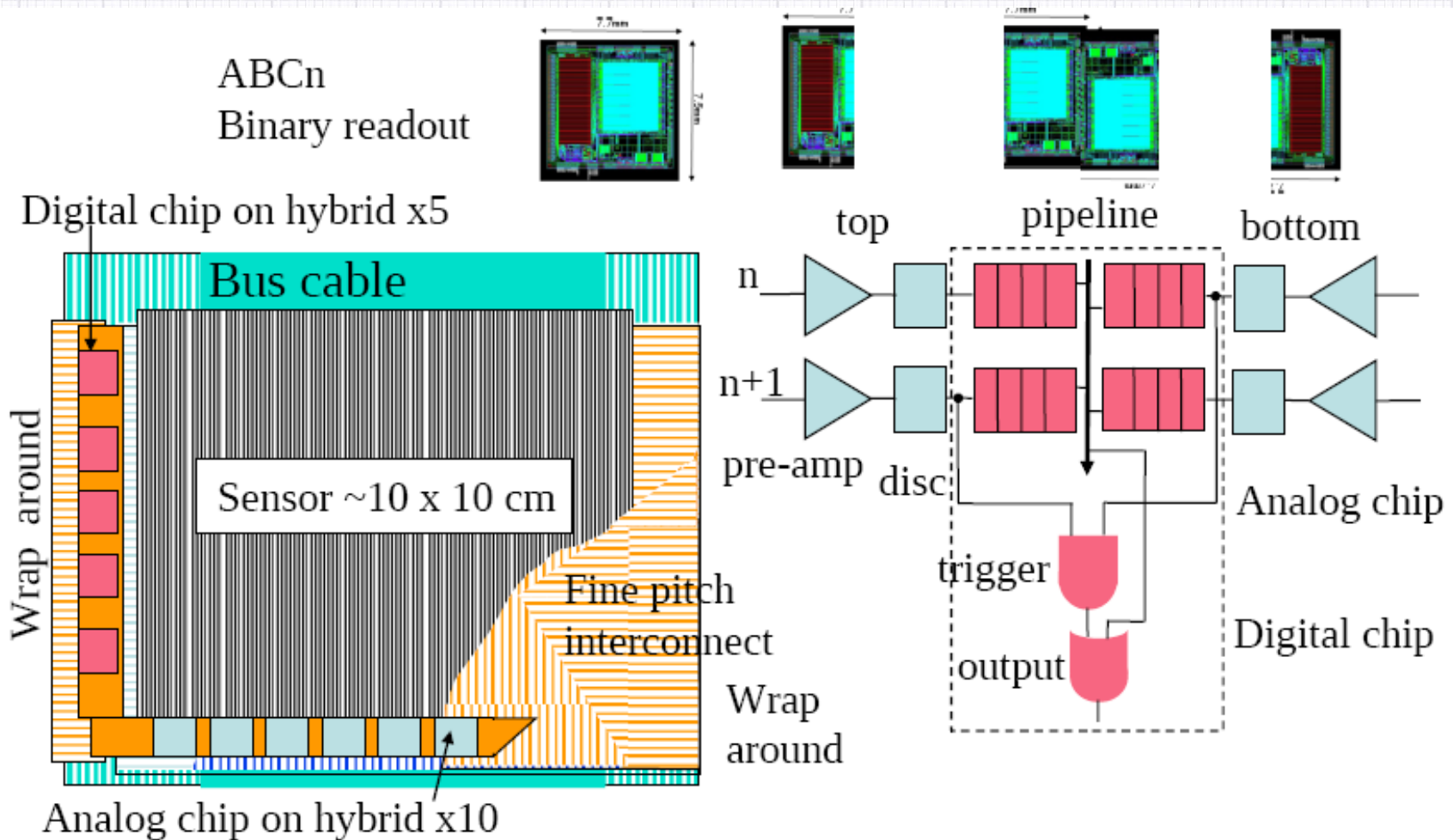
- Basic design of silicon strip layers are after some modifications are well suited for triggering
 - Short- (~2.5cm), Long-strips (~10cm): length 1.2 m, width ~ 11 cm
 - Thickness ~ 3-5 mm
 - Laminate of core, electrical bus, sensors, hybrids, chips
 - Mass 2.26 (1.73)% X0 (34% core, 66% electrical+sensors)





Split chip approach for triggering

- Split the readout chip and add an embedded fine pitch interconnection. Analogue part near sensor to minimize noise, digital separated and connected top-bottom for coincidence logic.





Summary split approach

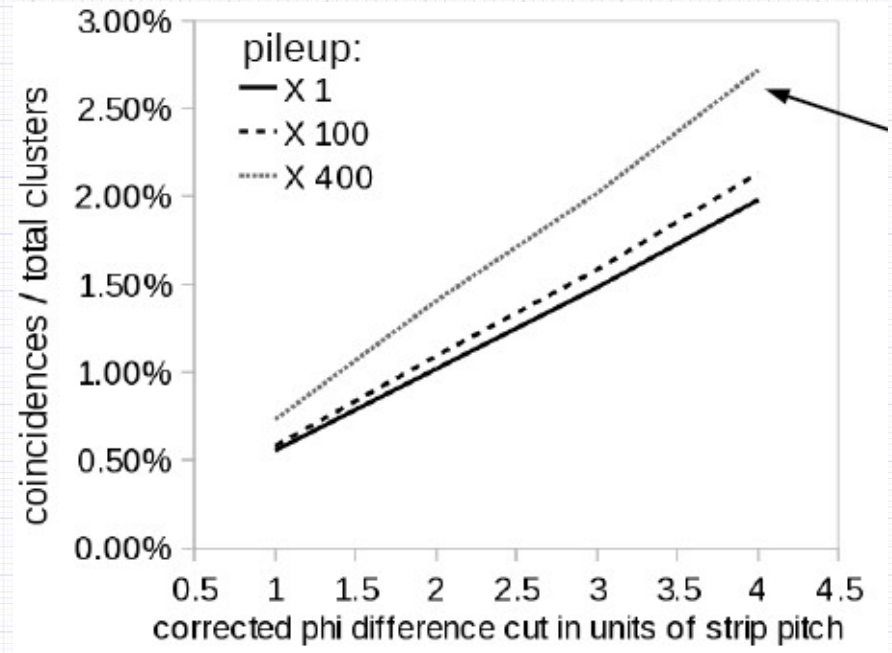
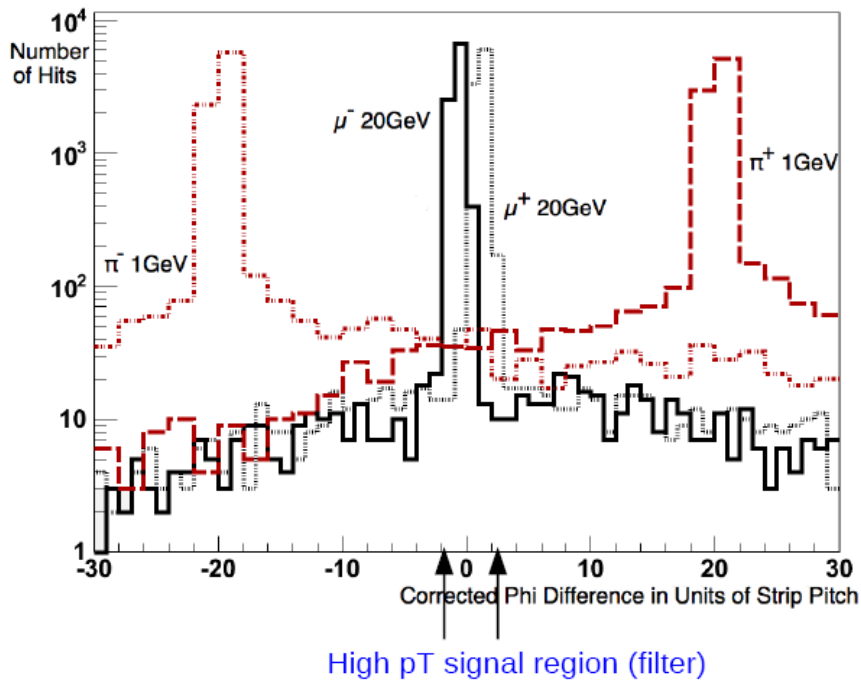
- Consider effect of additional chips and interconnect material on the stave
- Compare to material estimates studied earlier as part of ongoing stave R&D
 - Effect of trigger components is not large
- Of potentially more concern are thermal and electrical interference
- Impact of axial/axial vs axial/stereo not yet known

Stave	Flex SS	Flex LS	Flex LS + Trig
Core	0.73	0.73	0.73
Module	1.49	0.96	1.07
Glue	0.04	0.04	0.04
Total %Xo	2.26	1.73	1.84



Simulation results

The shift of hits between top and bottom layers separates low p_T tracks from high p_T . Example for 10cm long strips layer at $R=1m$. Doublet separation=4.5mm



- Even with 400 pileup combinatorial background is small compared to correlated background

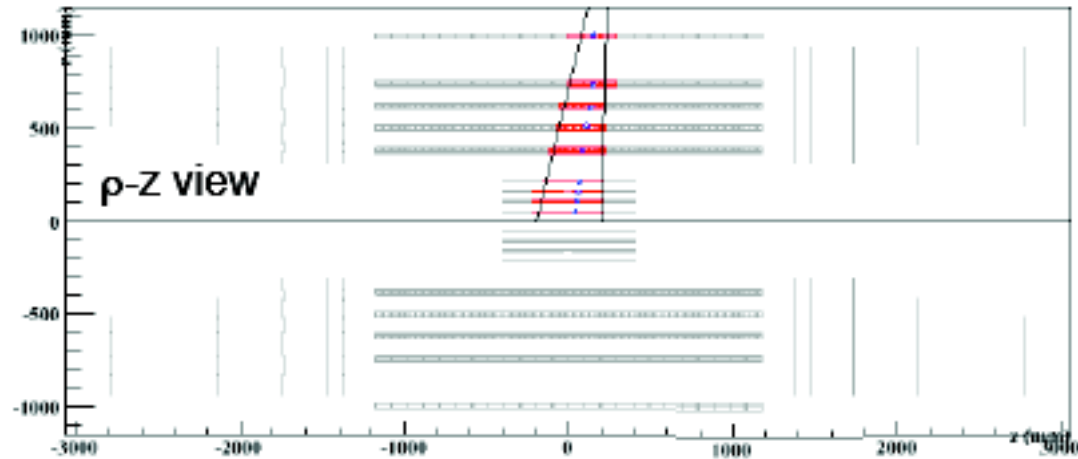
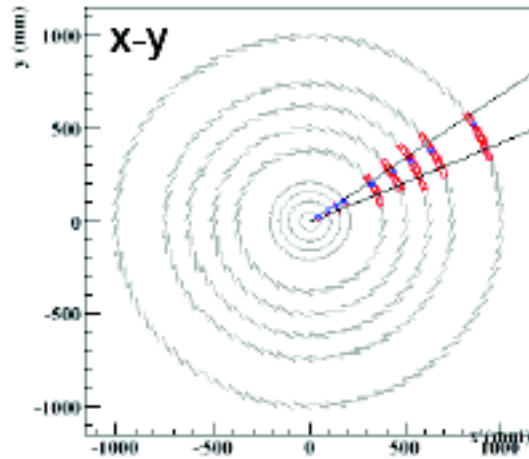
Combinatorial $\sim 1/\text{granularity}$
Correlated $\sim \text{material}$

Study by: M. Garcia-Sciveres et al.



Region of Interest seeded trigger

Rol: $\Delta\phi=0.2$, $\Delta\eta=0.2$ at Calo $\Delta z=40\text{cm}$ at beam line



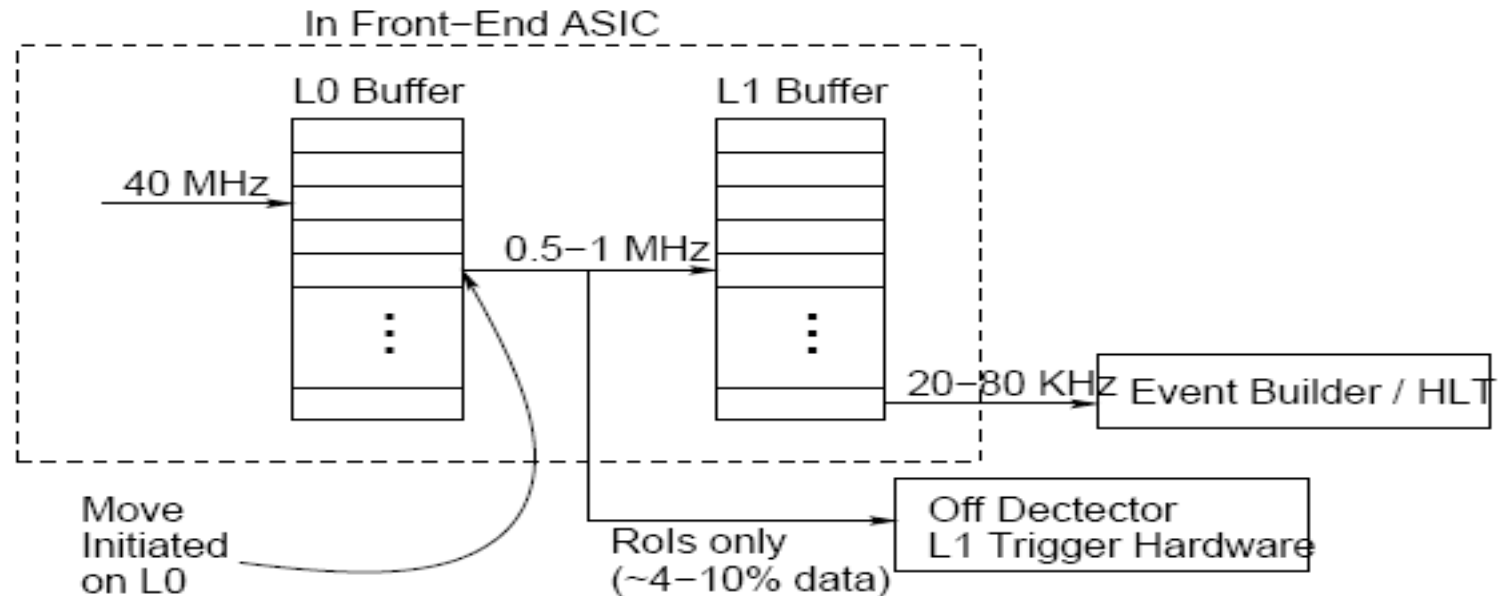
- An L0 similar to the current L1-Calor and L1-Muon defines the regions of interest (Rols), no tracking information in Rol definition
- Rol defines an eta-phi region for strips and pixel information to be extracted, Rols about 1% of the detector/event
- L1 uses inner detector information from the Rols that were defined in L0
- Can also do a detailed correlation with outer detector



L0 implementation

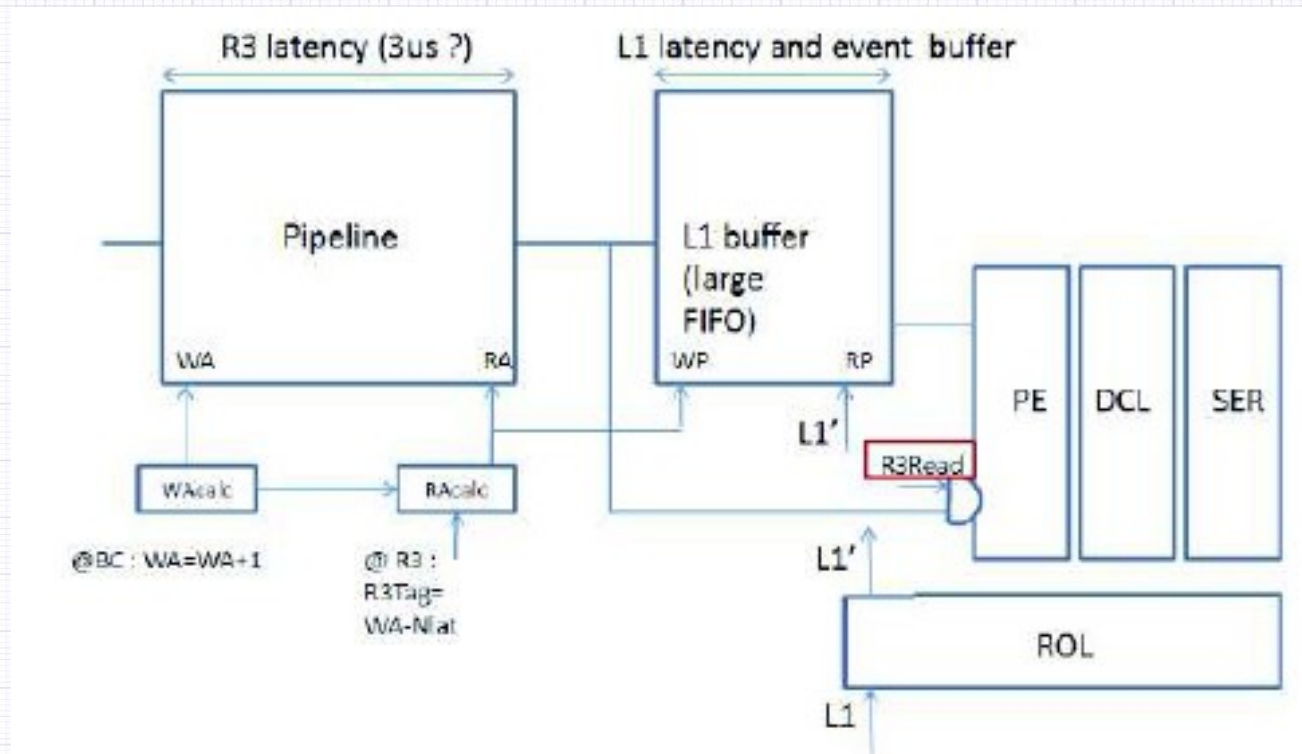
- Calo and muon detectors provide a high rate L0 trigger with Rol information (500 kHz - 1MHz) with a latency $< 3.2 \mu\text{s}$, Regional Readout Request (R3)
- The L0 information is moved to a L1 buffer on the front-end chip
- Only L0 information from Rol is transferred off-detector
- Full detector readout after L1 trigger with latency 50-256 μs

Conceptual Schematic:





Conceptual FE-chip design



- The Rol trigger can be easily accommodated in present tracker.
- Design studies under way in the strip readout working group for its next prototype FE-chip, ABCN-130
- Rol based trigger gives maximum flexibility with little impact on tracker design but requires a global TDAQ upgrade of ATLAS, with all detectors accepting long L1 trigger latency



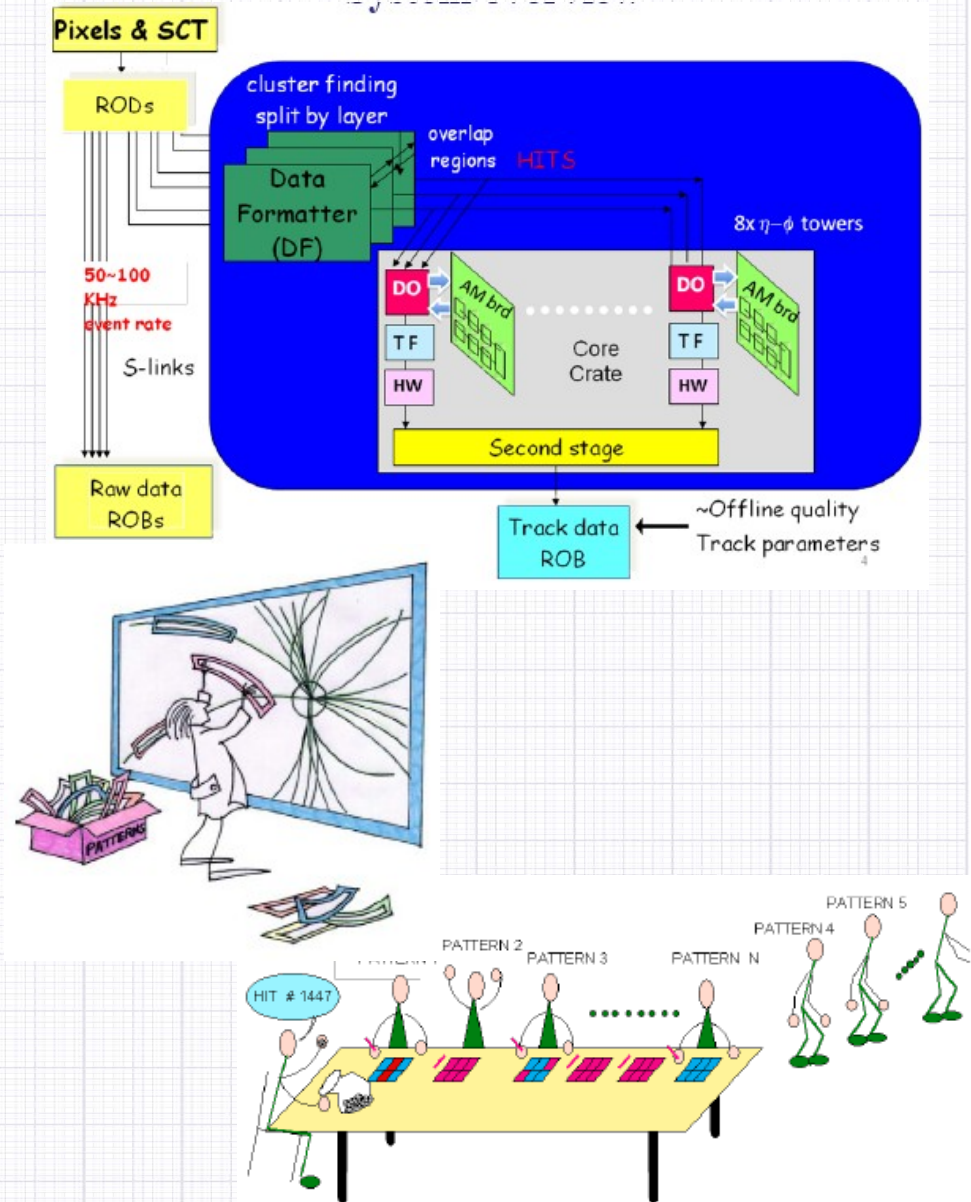
Advantages of RoI seeded trigger

- Flexibility:
 - any RoI driven processing possible at 1 MHz
 - Full tracking in RoI with 50-100 μ s for algorithm, complexity limited by external computing
 - MDT information in Rols at L1 (like μ -Fast algorithm in current L2)
 - EM and jet clustering and shower-shapes with full granularity
 - Refined track-shower matching
- Decouples tracker geometry from trigger:
 - Sophisticated trigger algorithms are implemented in external hardware (computers, associative memory,...) not in dedicated very fast L1 hardware.
 - Does not impose additional constraints on ID configuration i.e. layers, granularity,...



Template method: Fast Tracker (FTK), trigger at L1.5

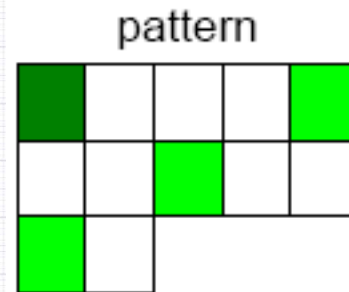
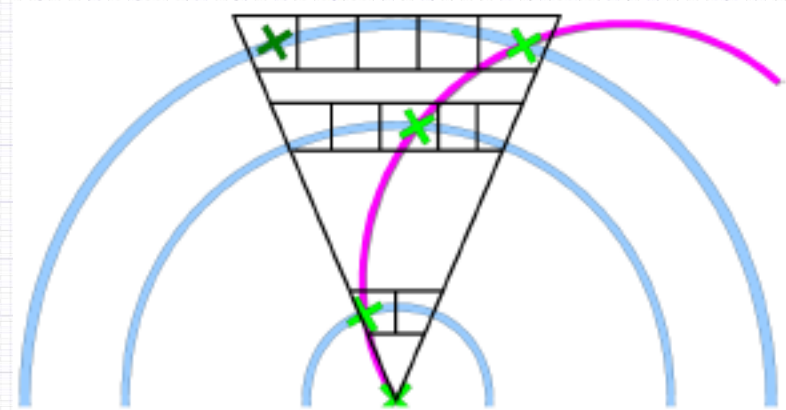
- Process all data from pixels and SCT on a L1A
- Fast processing in custom made dedicated Associative Memory chips (AM)
- Template method with 10^9 patterns (roads) to see the silicon hits leaving the detector at full speed
- Design demonstrated by simulation to work up to $L = 3 \cdot 10^{34} \text{cm}^{-2} \text{s}^{-1}$
- Will not help the L1 problem at SLHC but the technology is interesting for SLHC
- Project has submitted a Technical Proposal waiting for approval for a TDR (deployment 2016?)



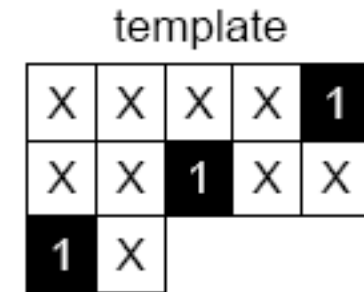


Fast template method with CAMs

- Match pattern in strips or pixels with precomputed templates
- Templates are stored in Ternary-CAMs (Column Accessible Memory) providing storage and fast match
- Every part of the detector is special, no symmetry exploited
- Main questions
 - How many templates depending on detector geometry?
 - Fake rate?
 - Hardware implementation?
- Applicable for both ROI and Self Seeded track trigger



from detector



precomputed

X = don't care



Simulation studies of patterns and fake rates

- Results of “toy MC” + reconstruction (barrel only), minimum pT of 10 GeV
- SLHC upgrade tracker layout

No redundancy

design	N_{total} [billion]	fake tracks / N pile-up events		
		100	200	400
3 shorts (3/3)	3	100	750	6000
1 pixel* 3 shorts (4/4)	20	10	125	2000
2 pixel* 3 shorts (5/5)	80	1	30	1000
5 shorts (5/5)	230	0.01	0.3	10
5 shorts last layer at 86 cm (5/5)	100	0.01	0.3	10

Redundancy

5 shorts last layer at 86 cm (4/5)	160	5	60	1000
3 short doublets (5/6)	100	0.05	2	50
3 short doublets (6 cm spacing) (5/6)	30	0.01	0.3	10

pixel*: z-granularity coarsened from 250 μm to 2.4 cm.

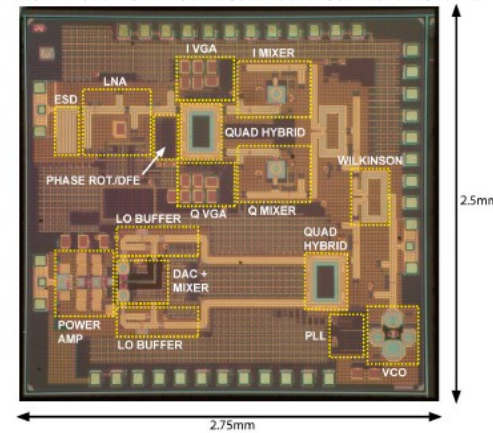
→ Would allow for lower pT cut and standalone trigger (low pile-up)

Study by: S. Schmitt, A. Schoening (Uni Heidelberg).

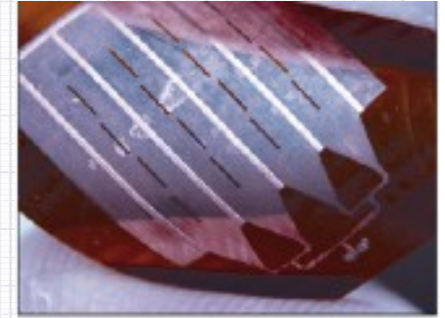


Wireless data transfer

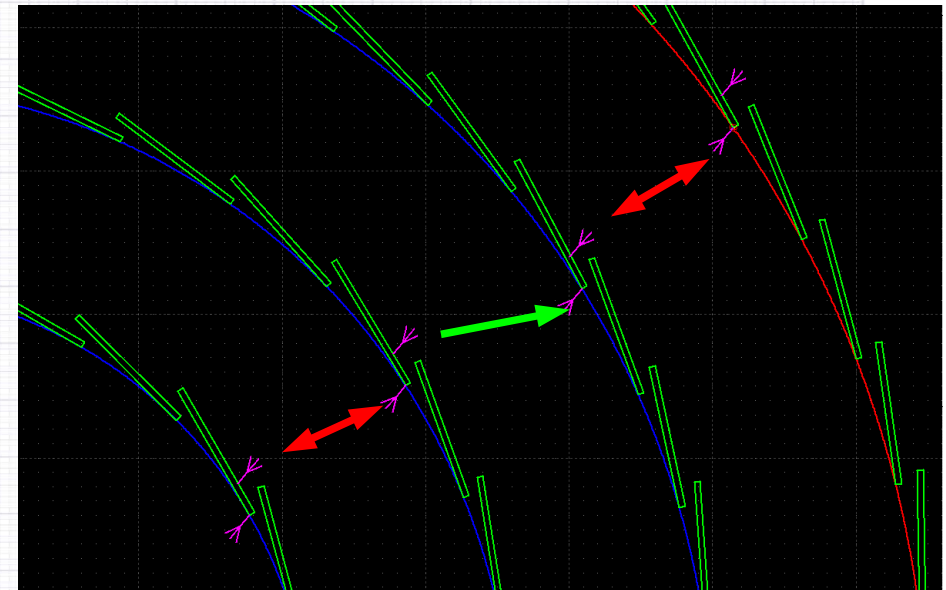
- 60 GHz technology offers a data transfer BW of 5-10 Gbit/s
- Technology compatible with tracker
 - Size of components are small, low mass (antenna $\sim 1 \text{ cm}^2$, chip $\sim \text{few mm}^2$)
 - power consumption is low ex. 90nm CMOS Low-Power 60GHz Transceiver (Marcu et al.) 170mW in transmit mode and 138mW in receive mode
- Allow radial data transfer for topological trigger



60 GHz transceiver



60 GHz slot antenna on kapton



Inter layer intelligence



Conclusions

- Event selection at L1 will be a challenge at SLHC
- ATLAS is investigating several upgrade options to improve the L1 trigger
- A large improvement in trigger rates, selectivity, thresholds seen if tracking information used in L1 trigger
- ATLAS is investigating two basic schemes to readout tracking information for L1 trigger
- Data bandwidth and trigger latency is a challenge for L1 trigger. New solutions in data transfer and processing are investigated.

More information on fast track trigger in “Workshop on Intelligent Trackers”, Feb 2010:

→ <http://indico.cern.ch/conferenceDisplay.py?confId=68677>

→ Proceeding to appear in JINST

(http://jinst.sissa.it/jinst/common/JINST_proceedings6.jsp)



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Back-up



Rol data bandwidth calculation

Inputs:

Beam Crossing Rate	40 MHz
Desired L0 Rate	500 KHz - 1 MHz
Desired L1 Rate	20 KHz (min) - 100 KHz (max)
Fraction of Data in Rol	2%(min) - 10% (max)
Number of L0 buffers	≈ 128 - 256
Number of L1 buffers	≈ 50 - 256

Latencies:

$$\text{L0 latency} = \frac{\text{L0 buffer size}}{\text{Beam Crossing Rate}} = 3.2\text{-}6.4 \mu\text{s}$$

$$\text{L1 latency} = \frac{\text{L1 buffer size}}{\text{L0 Accept Rate}} = 50\text{-}256 \mu\text{s}$$

Data Output Bandwidth:

$$\begin{aligned} \text{Bandwidth} & \text{ full-event @ L1 Rate + Rol data @ L0 Rate} \\ & \approx ((20\text{-}100) \text{ KHz} + (2\%\text{-}10\%) \times 1 \text{ MHz}) \text{ full-events} \\ & \approx 40 \text{ KHz} - 200 \text{ KHz full-events} \end{aligned}$$

Required bandwidth depends primarily on L1 rate and Rol size



Data bandwidth self-seeded

- “Natural” bandwidth given by standard 100kHz L1A.
 - This is 0.25% of raw sensor hits (100kHz/40Mhz)
- Each doublet layer needs $\sim 5x$ natural BW for THAT layer
 - 1% + 0.25% of raw hits instead of just 0.25%
- Assuming 2 doublet layers and 9 hits total, this results in roughly double the natural BW for the whole detector-
 \sim same as ROI
- Final answer depends on optimization-
 - What momentum threshold ($\Delta\phi$ cut) is desired
 - How little mass can be achieved
 - How is the mass distributed