# MAMBO III
# Monolithic Active Pixel Matrix with Binary Counters

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# Presentation Outline

- Applications
- Previous Work: MAMBO II
  - Design
  - Results
- MAMBO III development
  - Goals
  - Schematic
  - Layout
- T-Micro (ZyCube) 3D Integration
- MAMBO IV: Future work

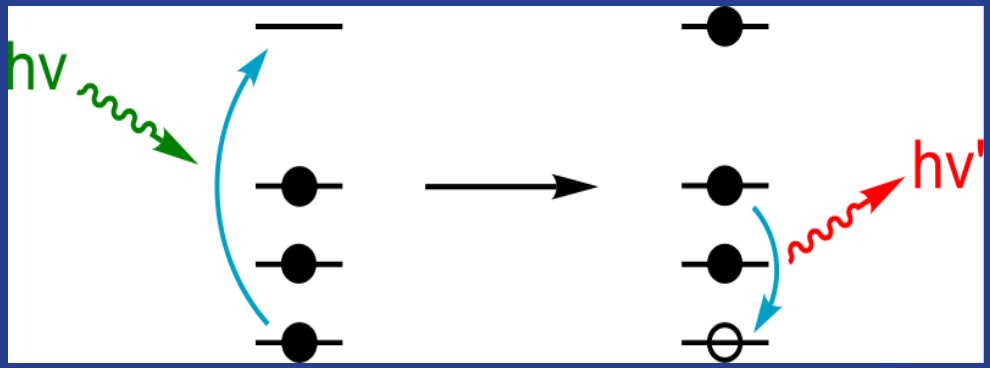
# POSSIBLE APPLICATIONS

# Possible applications

- Low energy applications up to 12kEv

E.g.

- X-ray autoradiography
- Fluorescence X-ray spectroscopy

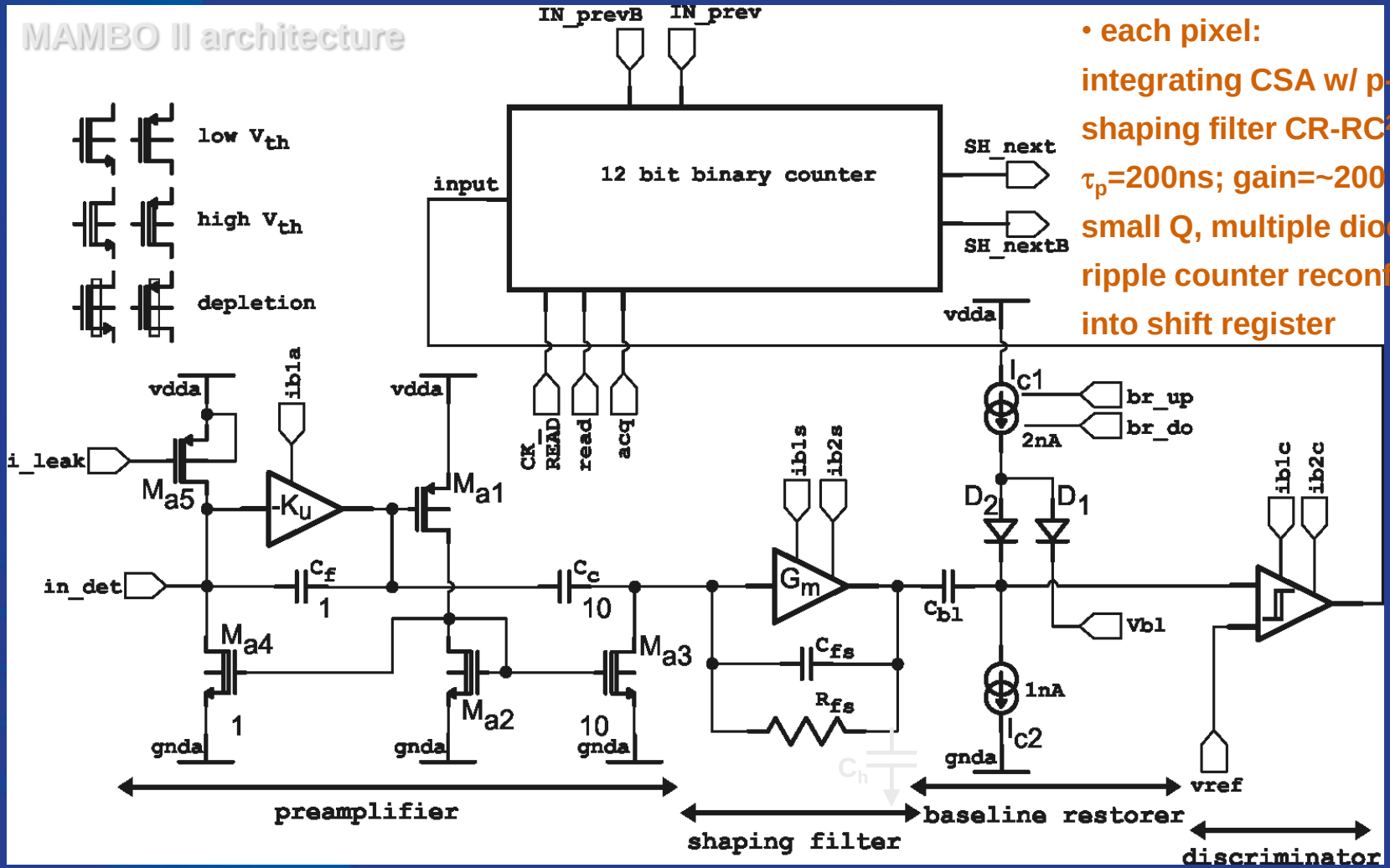


# PREVIOUS WORK

# MAMBO2

## Design details of pixel imaging detector „MAMBO"

**MAMBO = Monolithic Active Pixel Matrix with Binary Counters**




- each pixel:
  integrating CSA w/ p-z network, shaping filter CR-$RC^2$ with $\tau_p$=200ns; gain=~200 μV/$e^-$ for small Q, multiple diodes/pixel, ripple counter reconfigurable into shift register
- compact design excluding use of physical resistors

$C_c$=28 fF, $C_{fs}$=3.3 fF, $R_{fs}$=50 MΩ, $G_m$=5.8 μS, $C_h$=30 fF,



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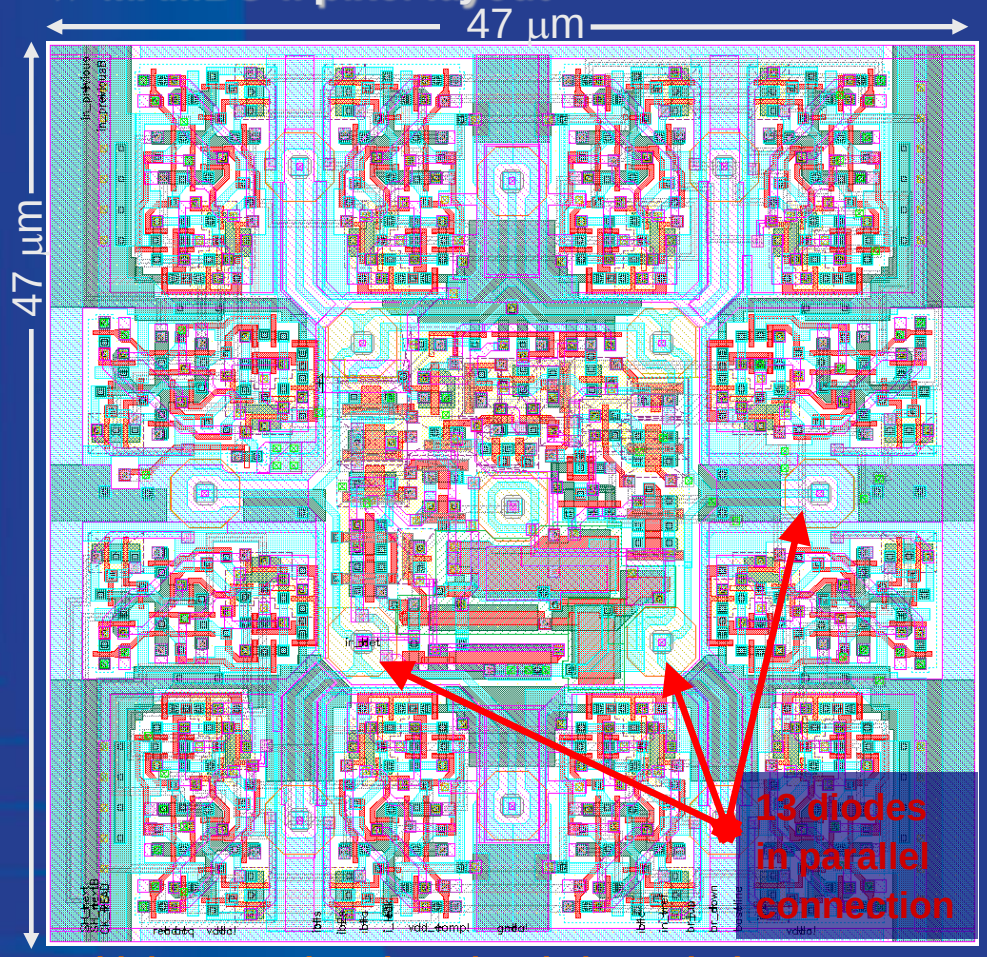
# MAMBO2: PREVIOUS WORK….

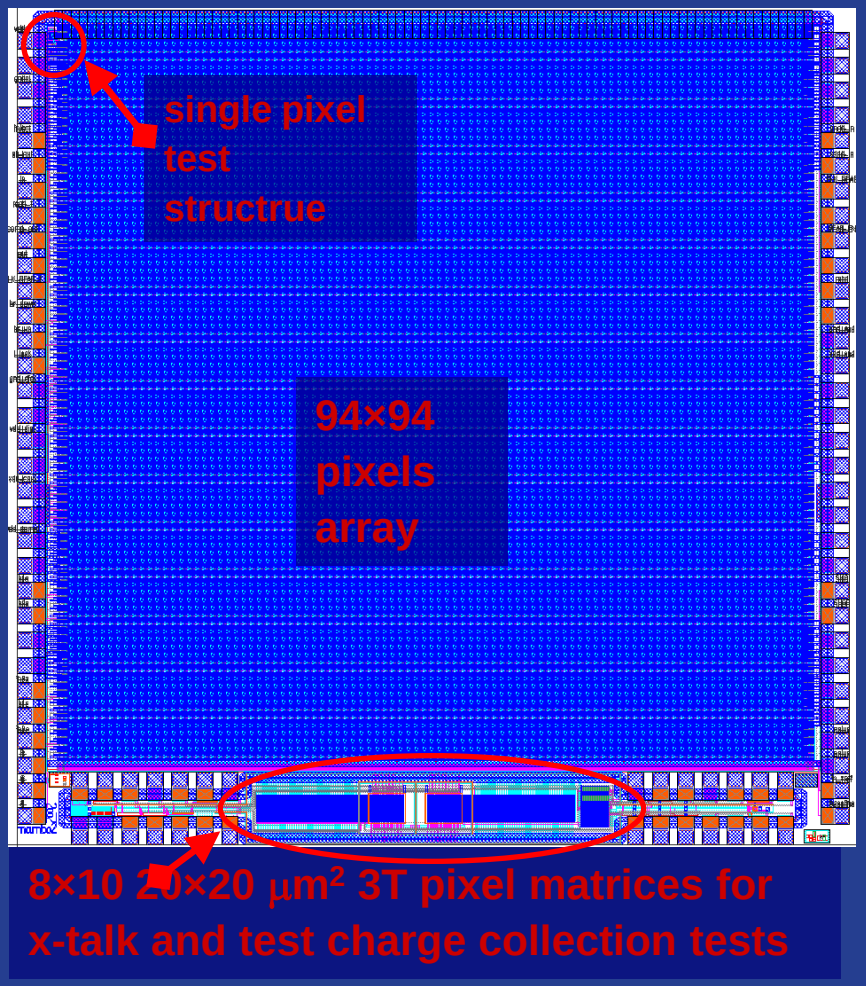
## Design details of pixel imaging detector „MAMBO"

- MAMBO II pixel layout




Multiple p-taps (used as signal electrodes) present per pixel for reduction of shifts of threshold voltages.
Partial success: adjustment of bias voltages and currents (referred to $V_{GS}$) up to several tens of mV still required for $V_{back}$ from the range from 0 to 10V.

- MAMBO II chip layout




Single pixel test structure is a fully functional ciruit allowing monitoring: shaper output, discriminator output, counter output



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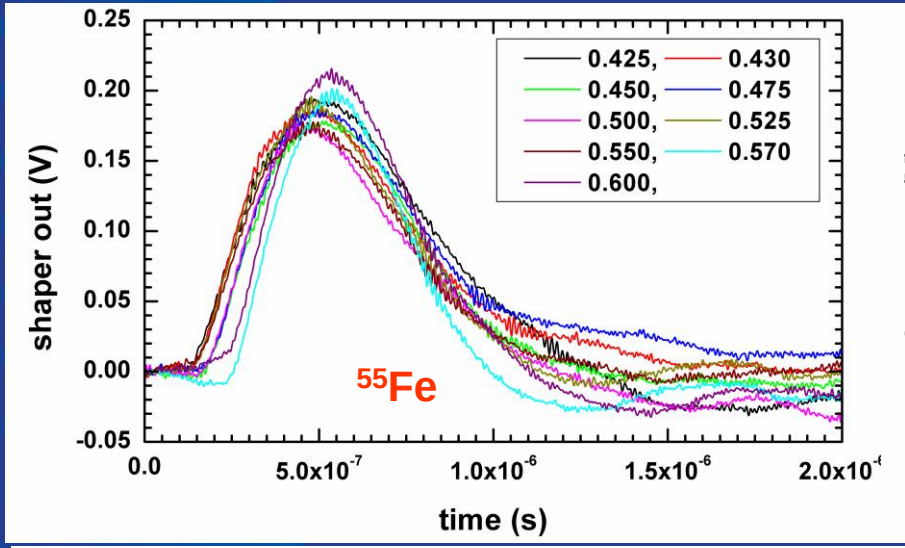
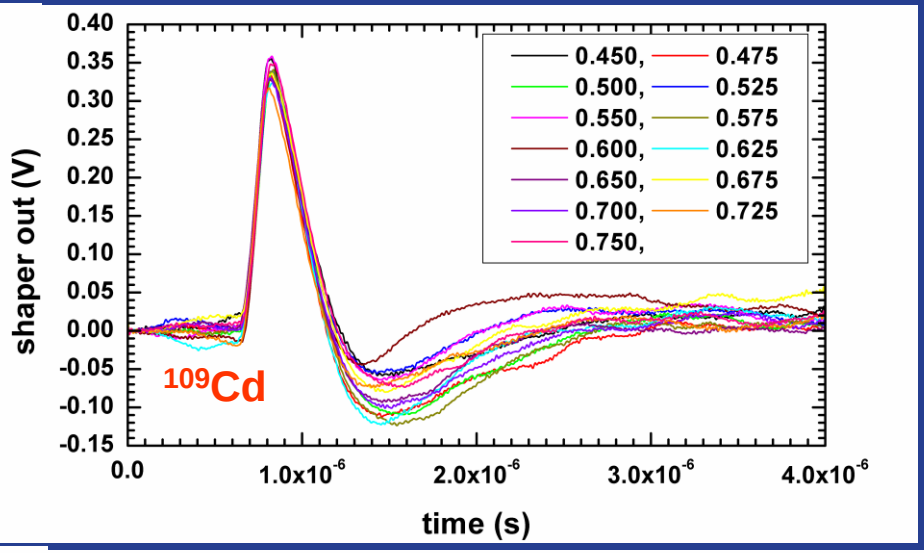
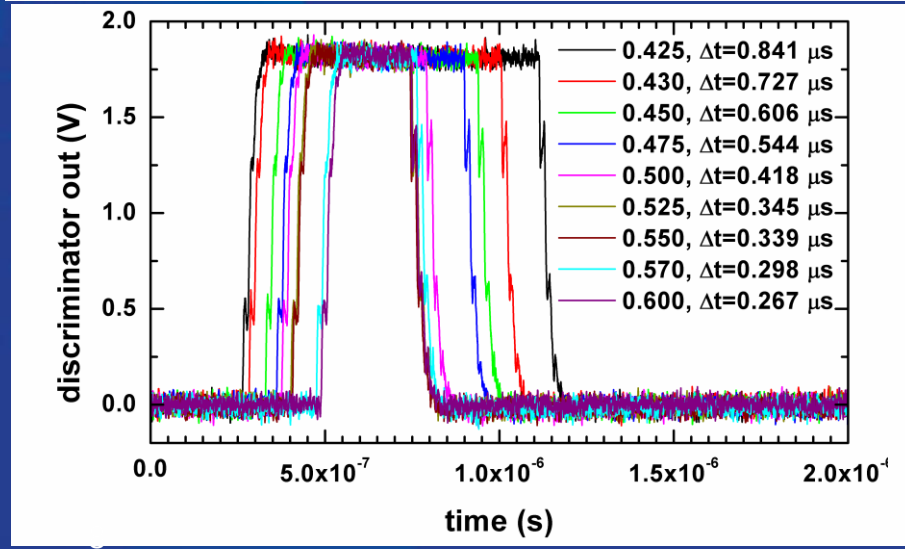
# Achievements, observations and investigations

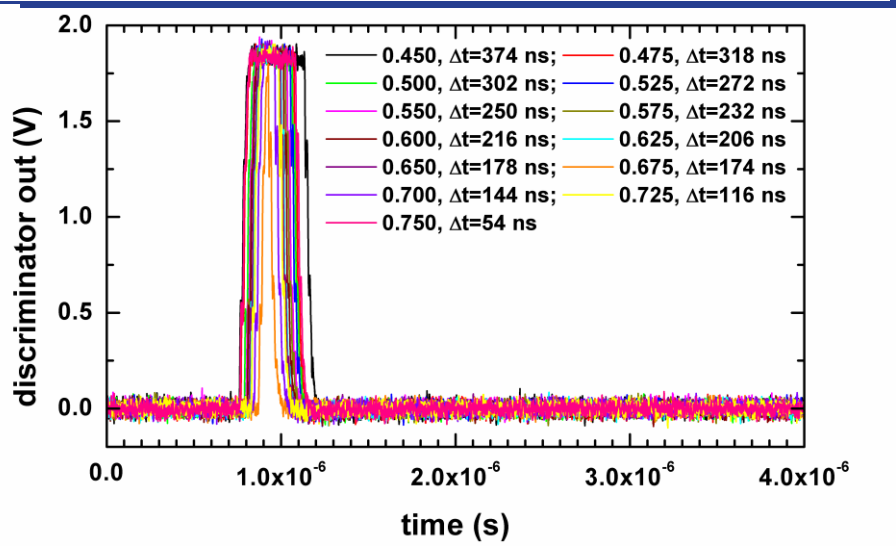
## MAMBO II single pixel test

### Monitoring of the shaper and discriminator outputs (transient signals )



# Conclusions

**credo:** ***strength of the SOI monolithic active pixel technology is integration of whole processing circuitry directly into 'the focal plane'***

- **the OKI process offers enhancements: through BOX contacts and diode and ohmic implants in the substrate material for the first time in a commercial approach!**
- **monolithic detector structures can operate depleted for the first time succesfully!**
- **matrices using 3T-type pixels can succesfully be built (NMOS/PMOS switches may be used); – some progress but not too much beyond bulk MAPS.**
- **mutual influence of CMOS circuitry and the detector is affecting designs of more advanced circuits for imaging.**
- **FD-SOI represents challenges for precise analog circuits, one would prefer different flavor!**
- **the properties of the substrate material and how it is depleted is far from being understood. The depletion may depend on transient and statically hold voltage states in the CMOS circuitry!**
- **observed high sensitivity to irradiation; overnight exposure under 100 μCi $^{109}$Cd under full operation causes ~100 mV voltage levels shifts.**

- **the process must be enhanced.**

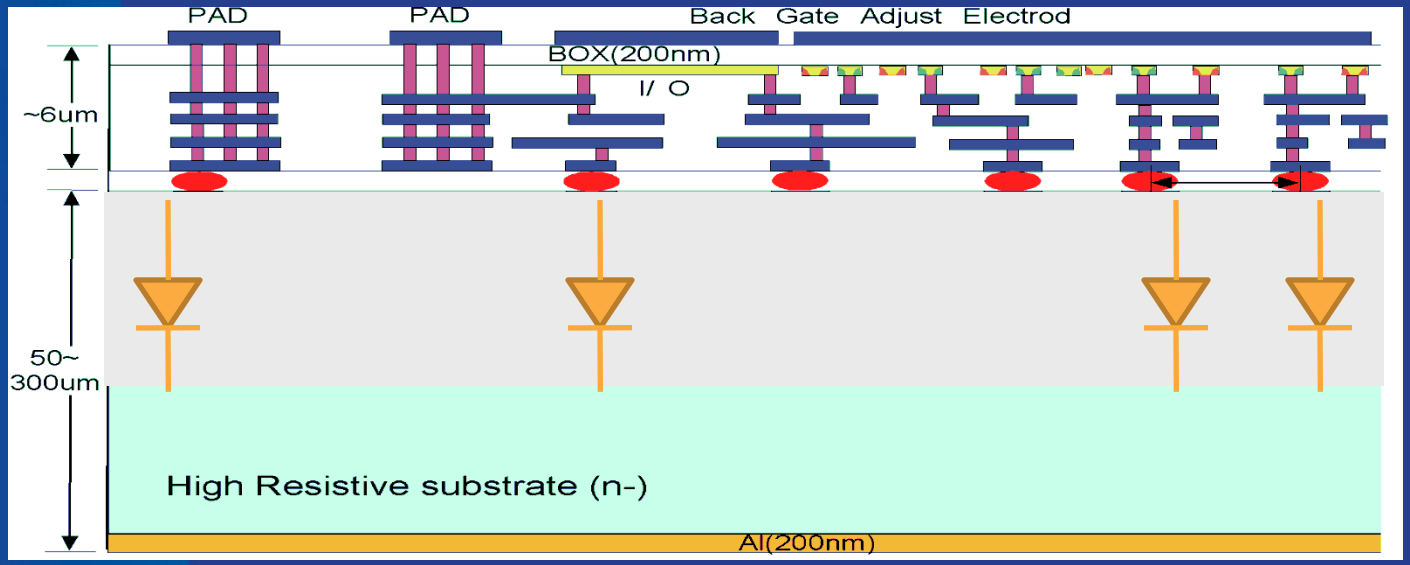
**The first priorities are to separate substrate and CMOS circuitry**

# MAMBO III

# Goals

- R&D
- Detector and electronics on different layers (to avoid coupling)
- Diodes with PPLUS with BPW to reduce leakage
- Diode of the same size as the pixel to obtain parallel electric field in active volume, and avoid potential pockets
- Shielding on detector layer
- Possibility of changing gated diode voltage to enhance performance of the diode
- Explore 3D IC technology with T-Micro

# 3D : MAMBO 3




MAMBO 3 top ASIC

MAMBO 3 bottom ASIC



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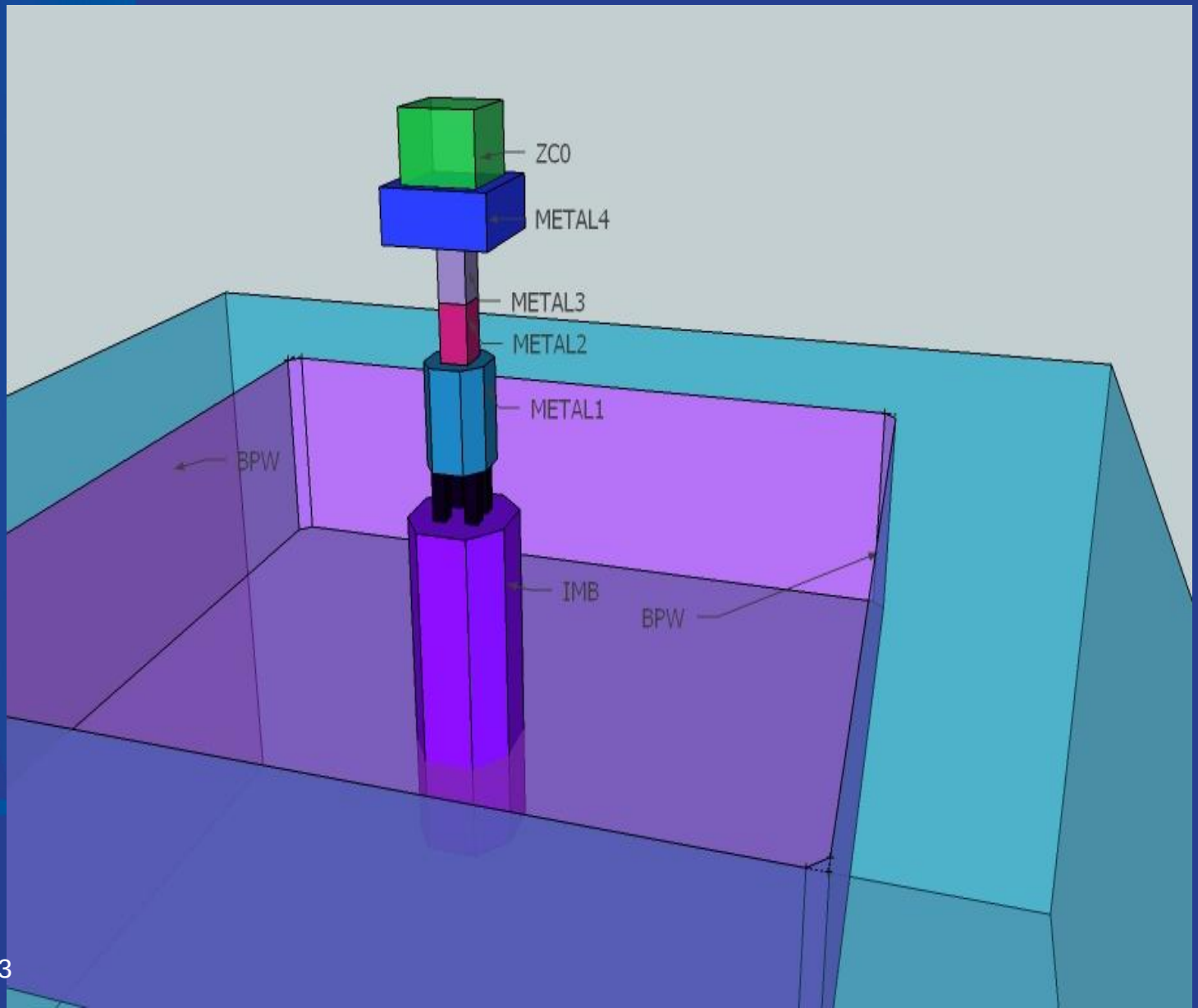
# 3D Model: Diode (Bottom Pixel)



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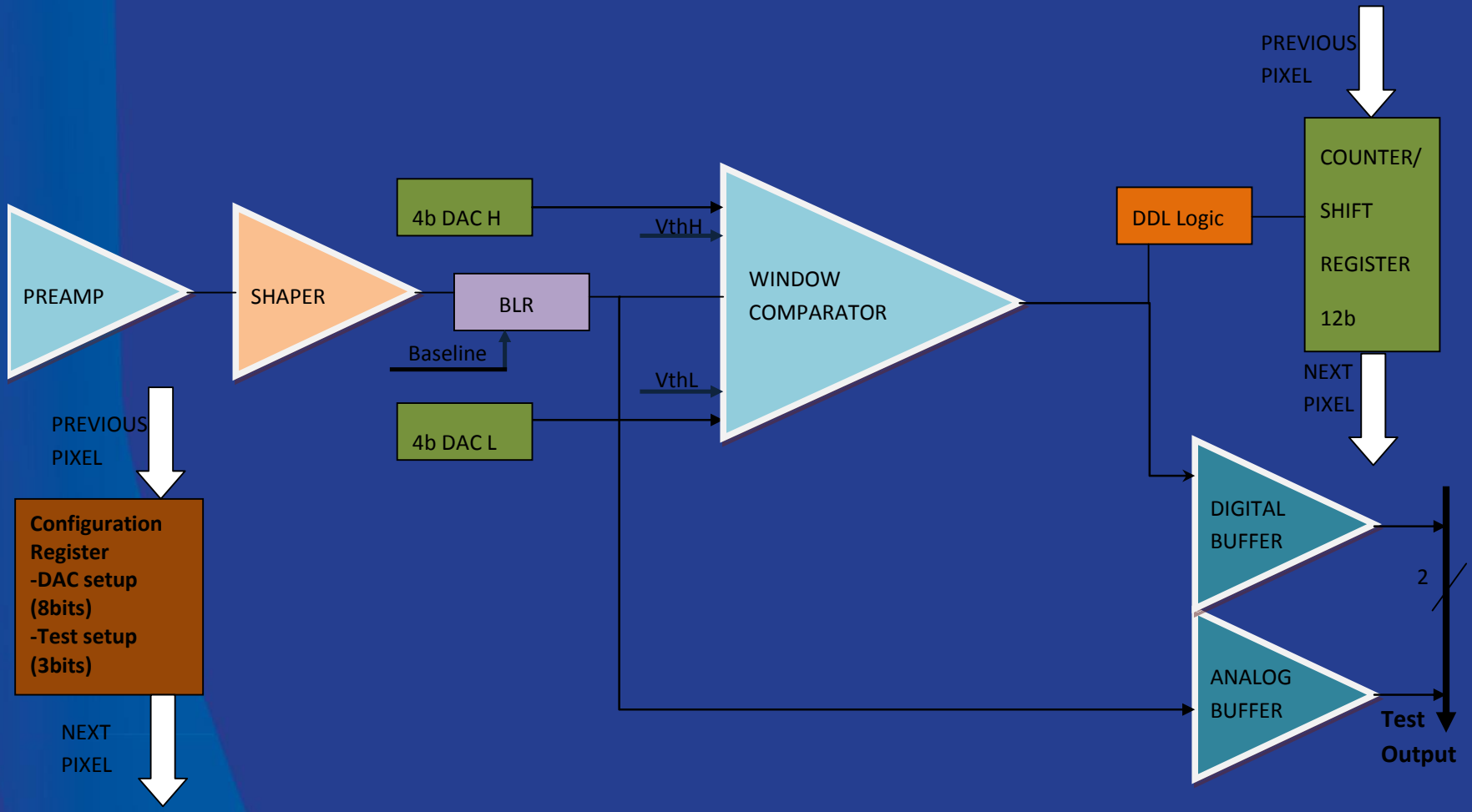
# Top ASIC: PIXEL Design



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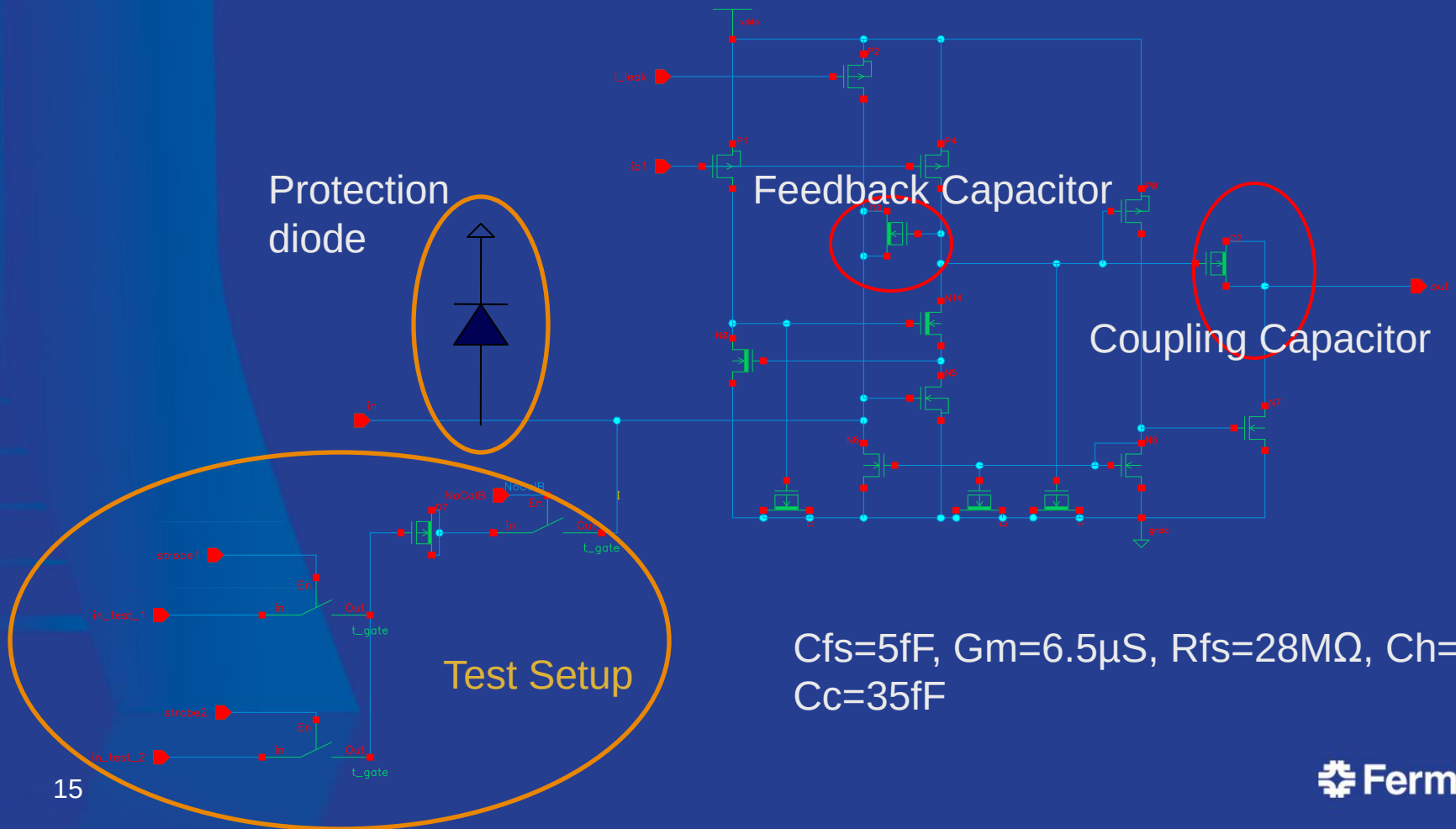
# Preamplifier

- Regulated Cascode
- Leakage current compensation
- 1.7fF I/P test capacitance



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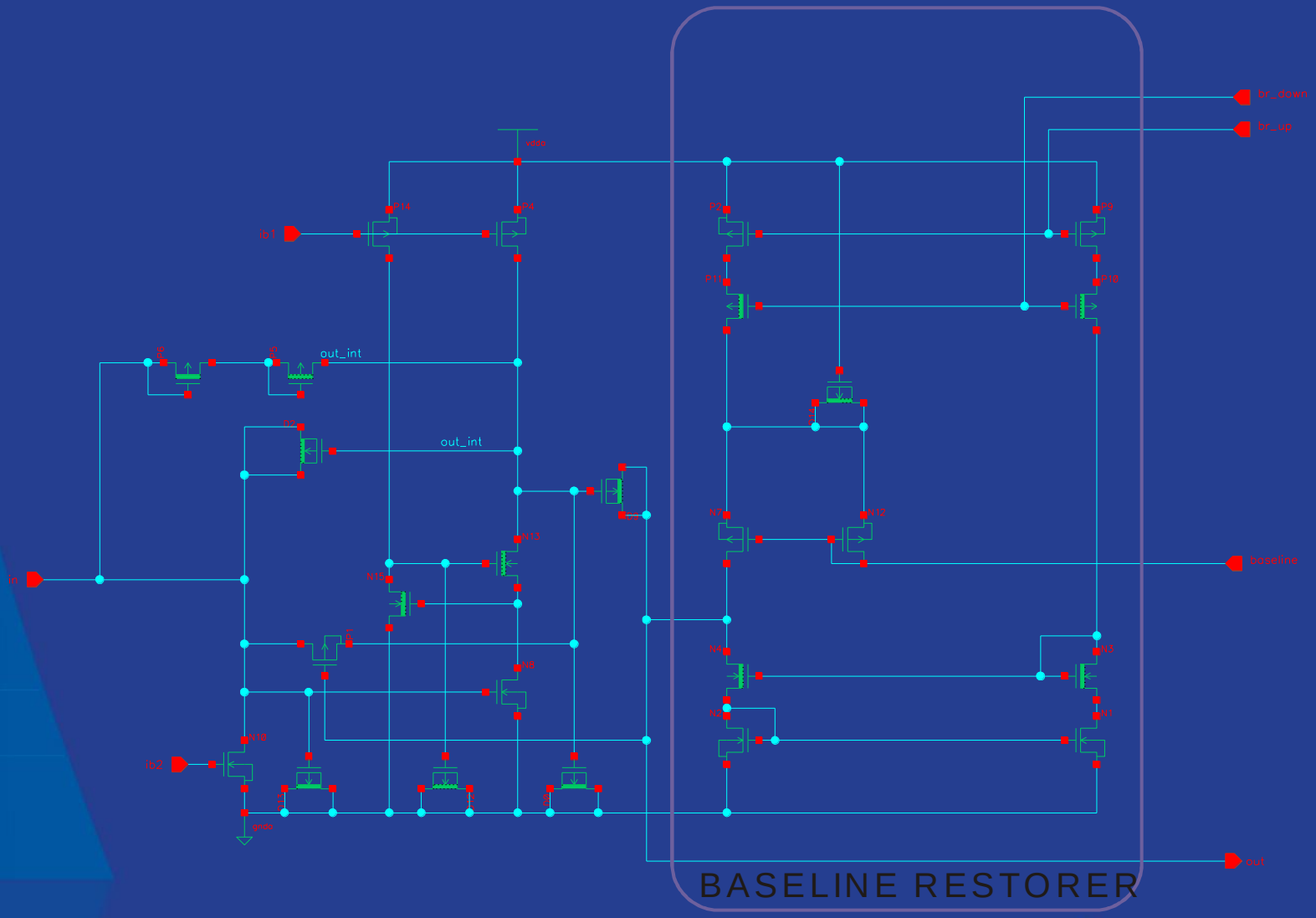
# Shaper and Baseline Restorer



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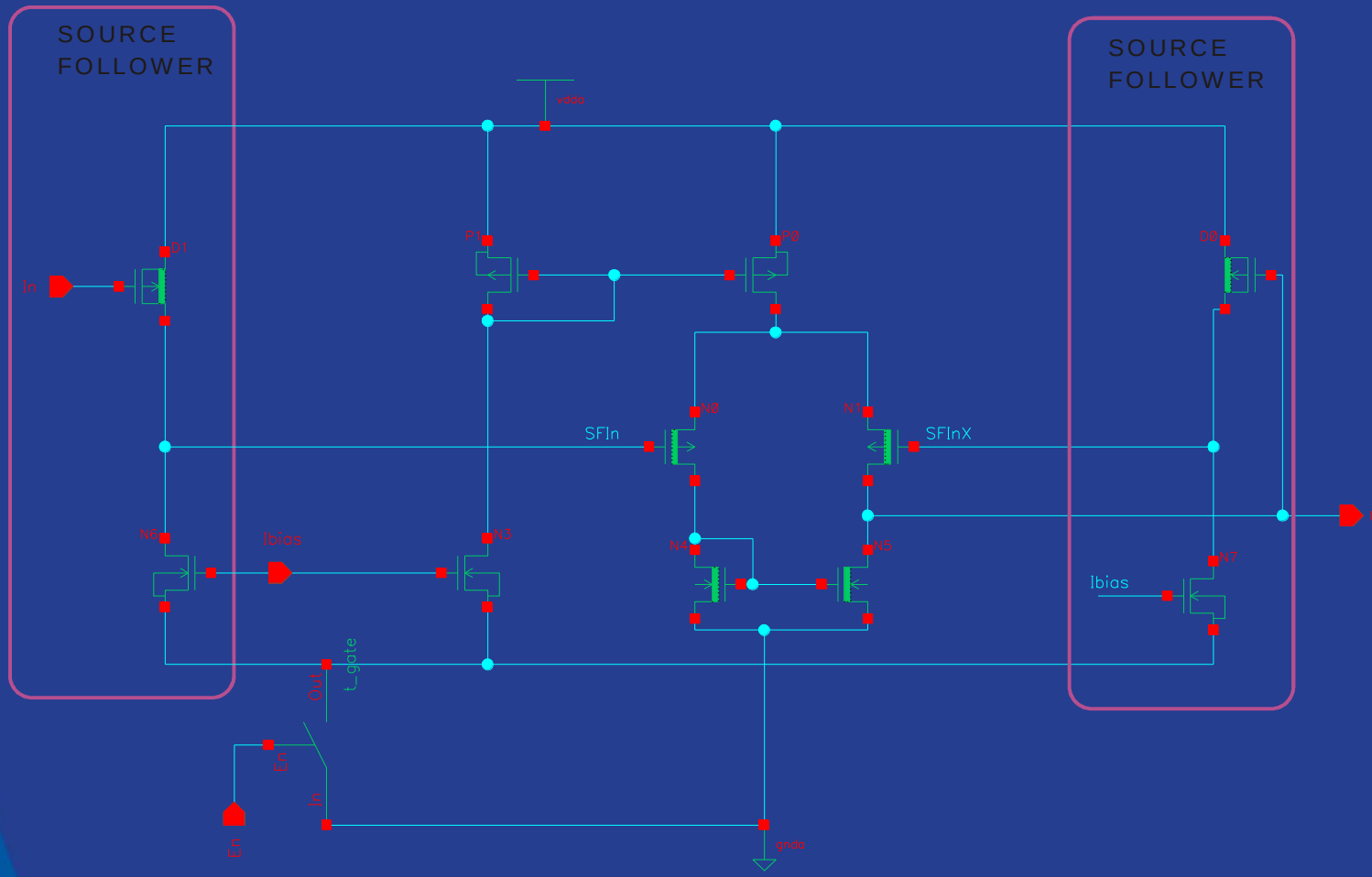
# Analog Test Buffer

- Source Followers using Zero Vt DMOS transistors
- Single Stage amplifier
- Disconnected during normal mode of operation
- 10 µA current



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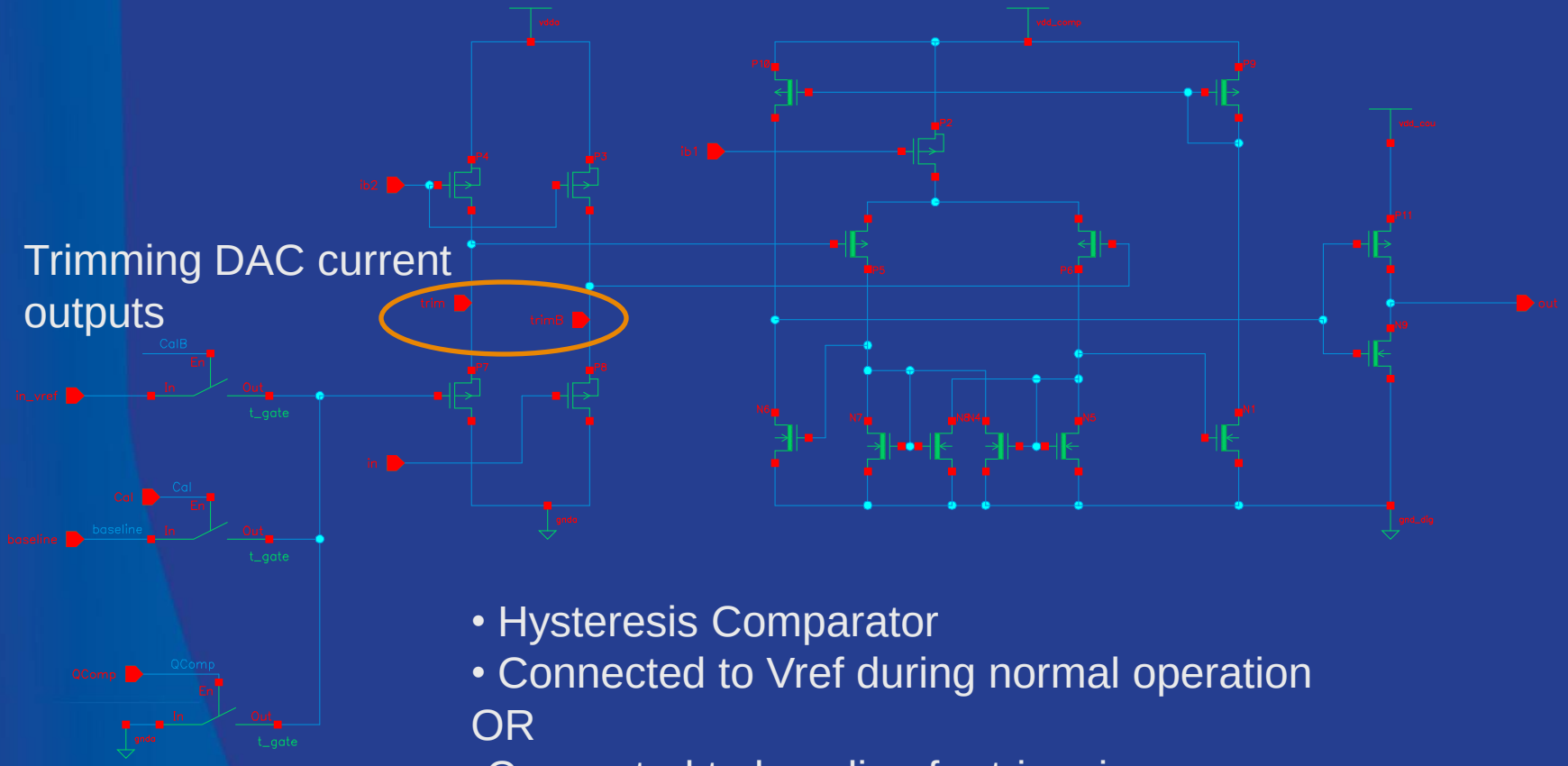
# Comparator

Trimming DAC current outputs




- Hysteresis Comparator
- Connected to Vref during normal operation

OR

- Connected to baseline for trimming

OR

- Connected to gnd! when disabled



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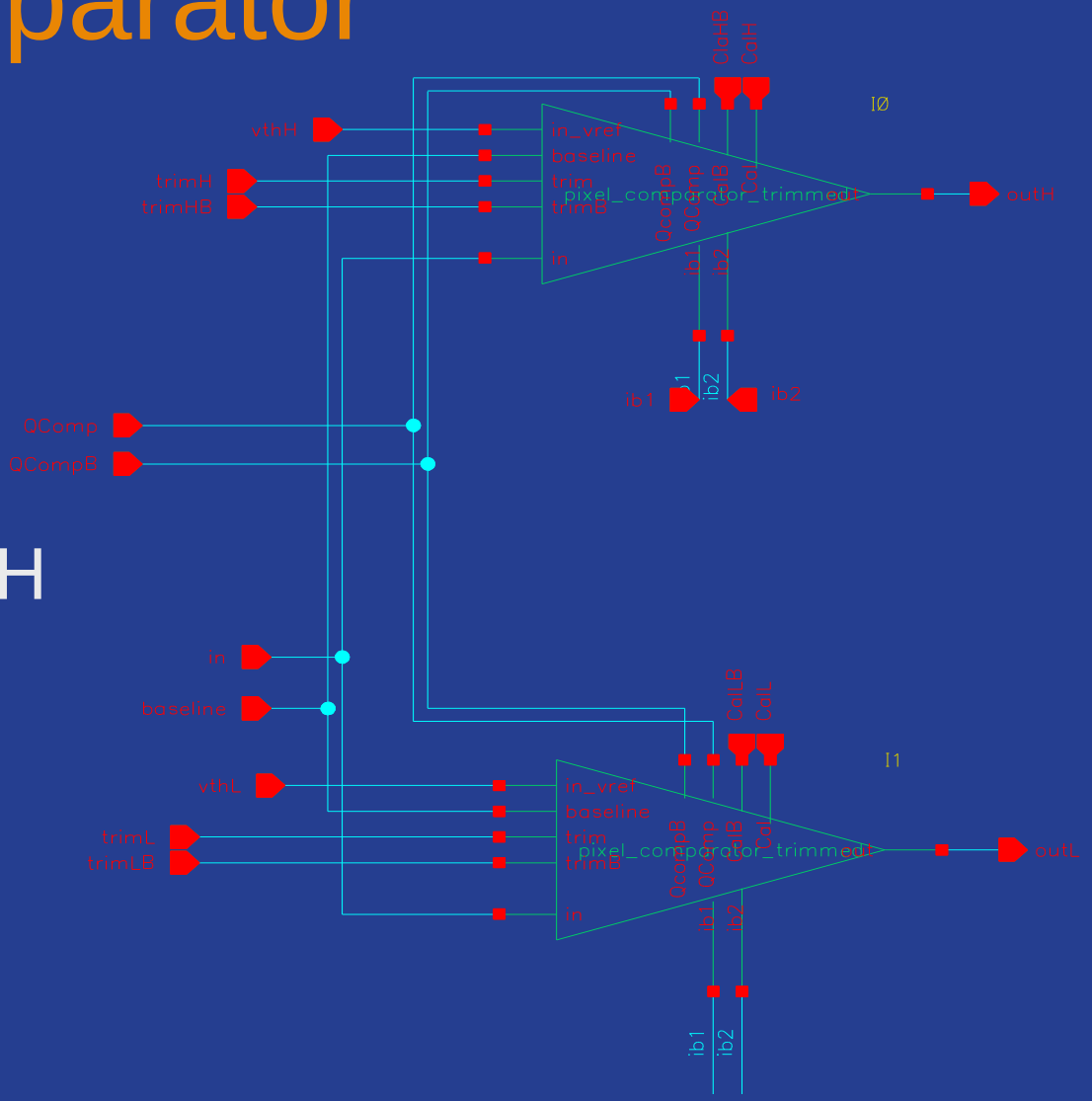
# Window Comparator

- VthL – Lower Threshold
- VthH –Upper Threshold
- VthL < Signals < VthH is recorded as HIT
- Comparators are independently trimmed to cancel offsets



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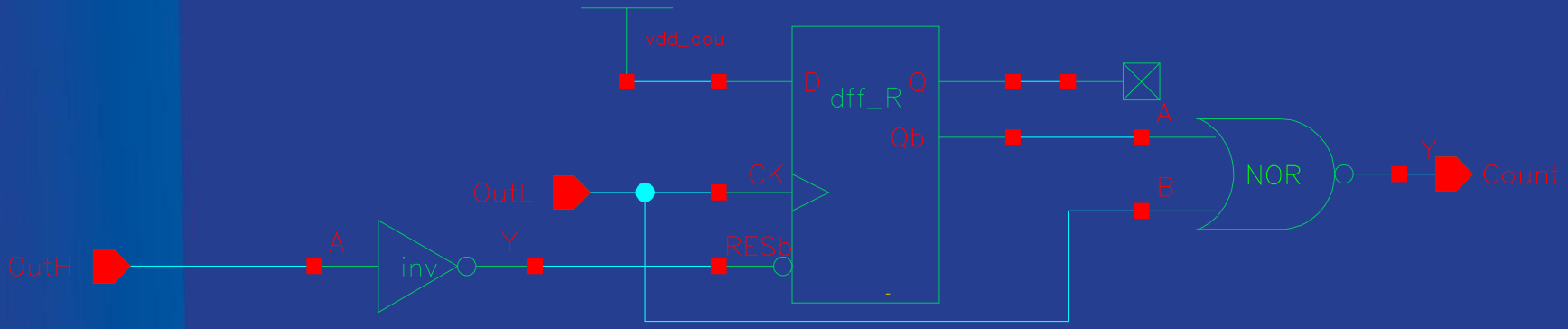
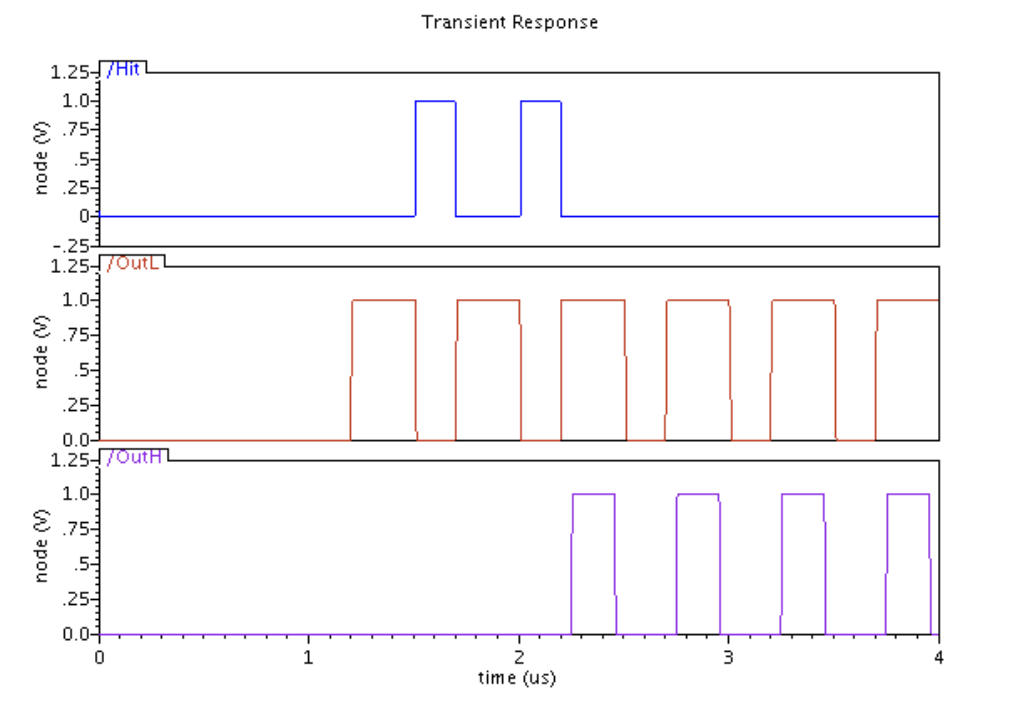
# Double Discriminator Logic




- Output of the Lower Threshold comparator behaves as a clock
- Output of the Upper Threshold comparator behaves as a Reset
- When both comparators fire the hit is not counted



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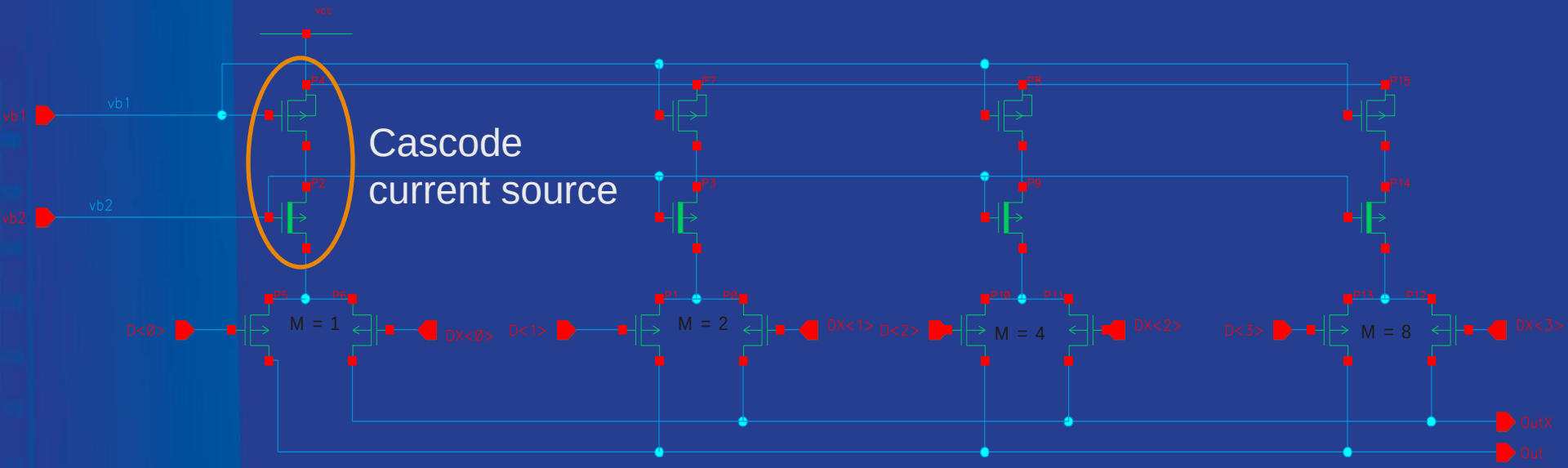
# Current Steering DAC (4 bits)




- Binary weighted current mirrors
- Switches are also binary weighted
- Current can be steered either to positive or negative output



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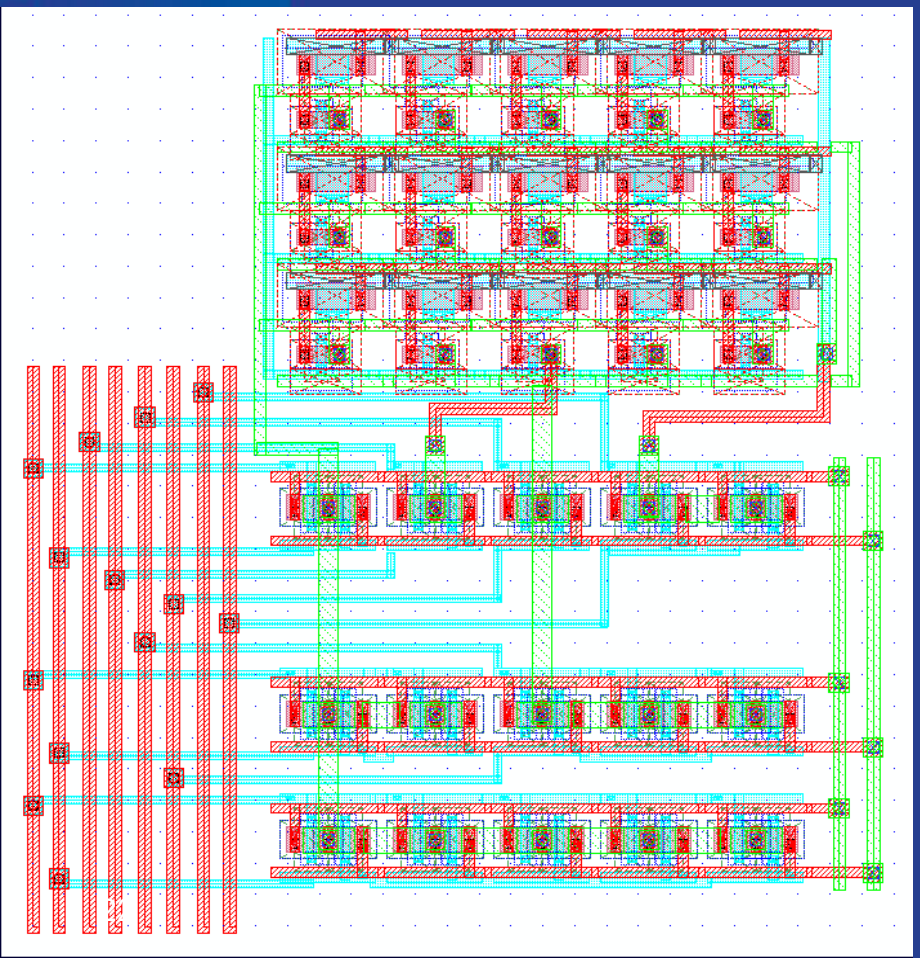
# DAC Layout



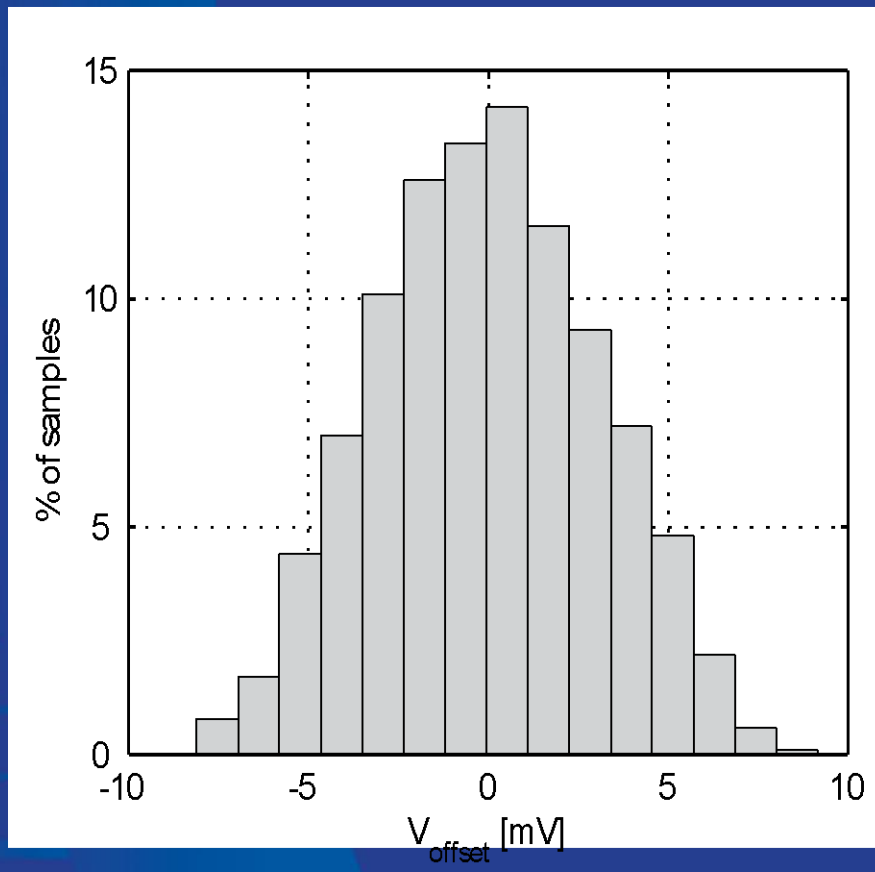
| | | | | |
|---|---|---|---|---|
| 4 | 3 | 4 | 3 | 4 |
| 4 | 2 | 1 | 2 | 4 |
| 4 | 3 | 4 | 3 | 4 |

Conventional  symmetrical common centroid geometry for current mirrors
Helps to average out global errors
•Matching is critical for monotonic performance

# Trimming DACs

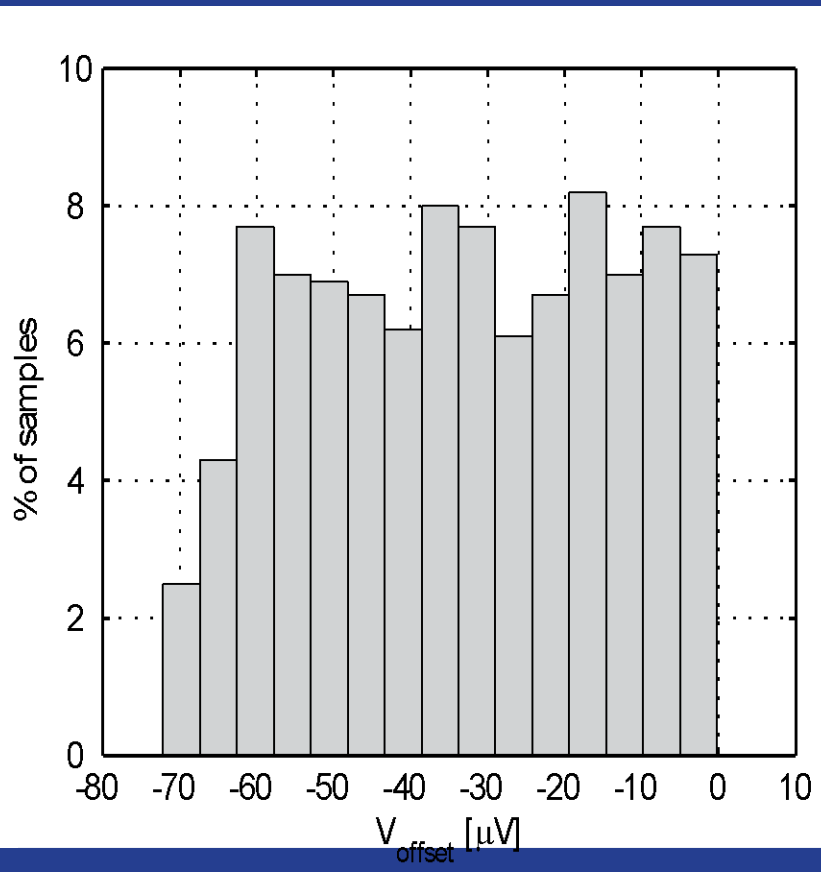
Matching is expected to be worse for SOI, Data here corresponds to a typical bulk CMOS process

## Offset distribution before compensation




- Gaussian distribution
- Depends on component matching

## Offset distribution after digital compensation




- Uniform distribution
- Residual offset depends on DAC resolution



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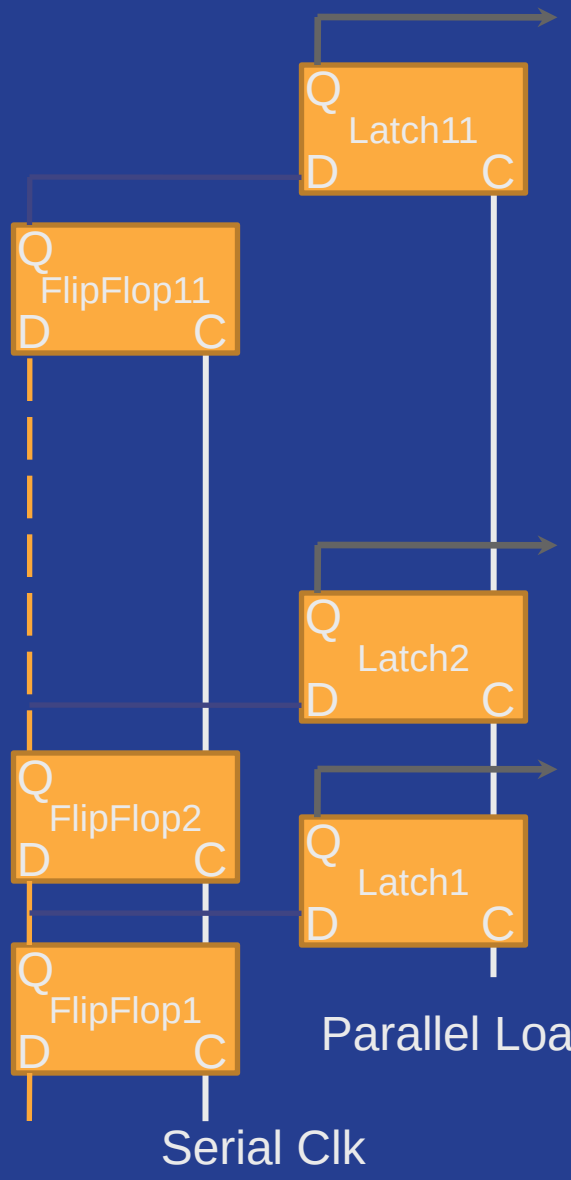
# Configuration Register

- Serial In Parallel Load
- (4b x 2) for DAC settings
- 3 bit test setup
- Test Control block used as decoder to control switches for test

| | Setup |
|---|---|
| 000 | Normal Operation |
| 001 | Analogue Output for test calibration |
| 010 | Test Input,  counter connected |
| 011 | Calibrate DAC L |
| 100 | Calibrate DAC H |
| 101 | xx |
| 110 | xx |
| 111 | Pixel Disabled |



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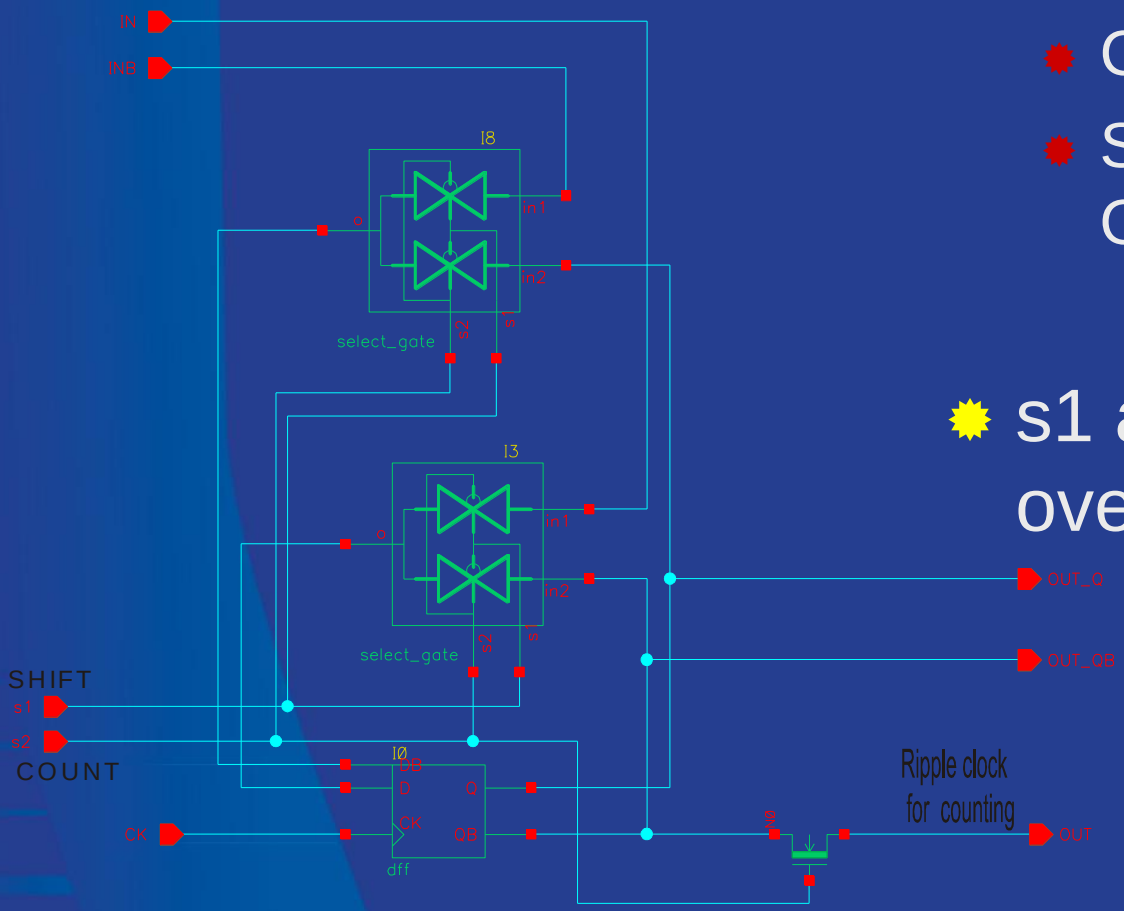
# 1bit Counter




- Can be configured as:
  - Counter (s1 is ON)
  - Shift Register (s2 is ON)
- s1 and s2 are non-overlapping clocks



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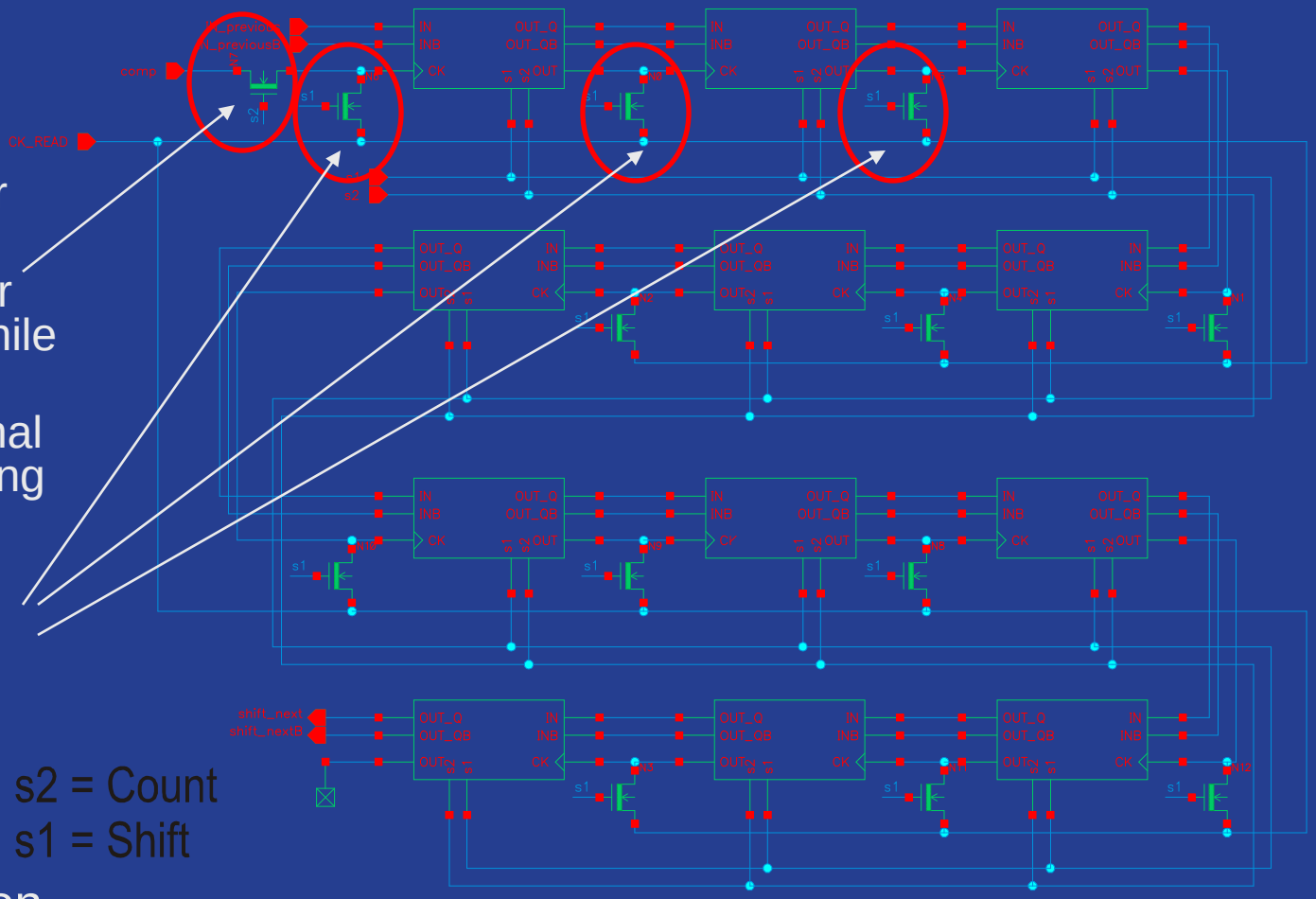
# Counter /Shift Register

- 12 bit ripple counter
- Count switch disconnects counter from comparator while shifting
- CK_READ is external clock used for shifting data
- Shift switch applied shifting clock




s2 = Count
s1 = Shift

- s1 and s2 are non-overlapping clocks



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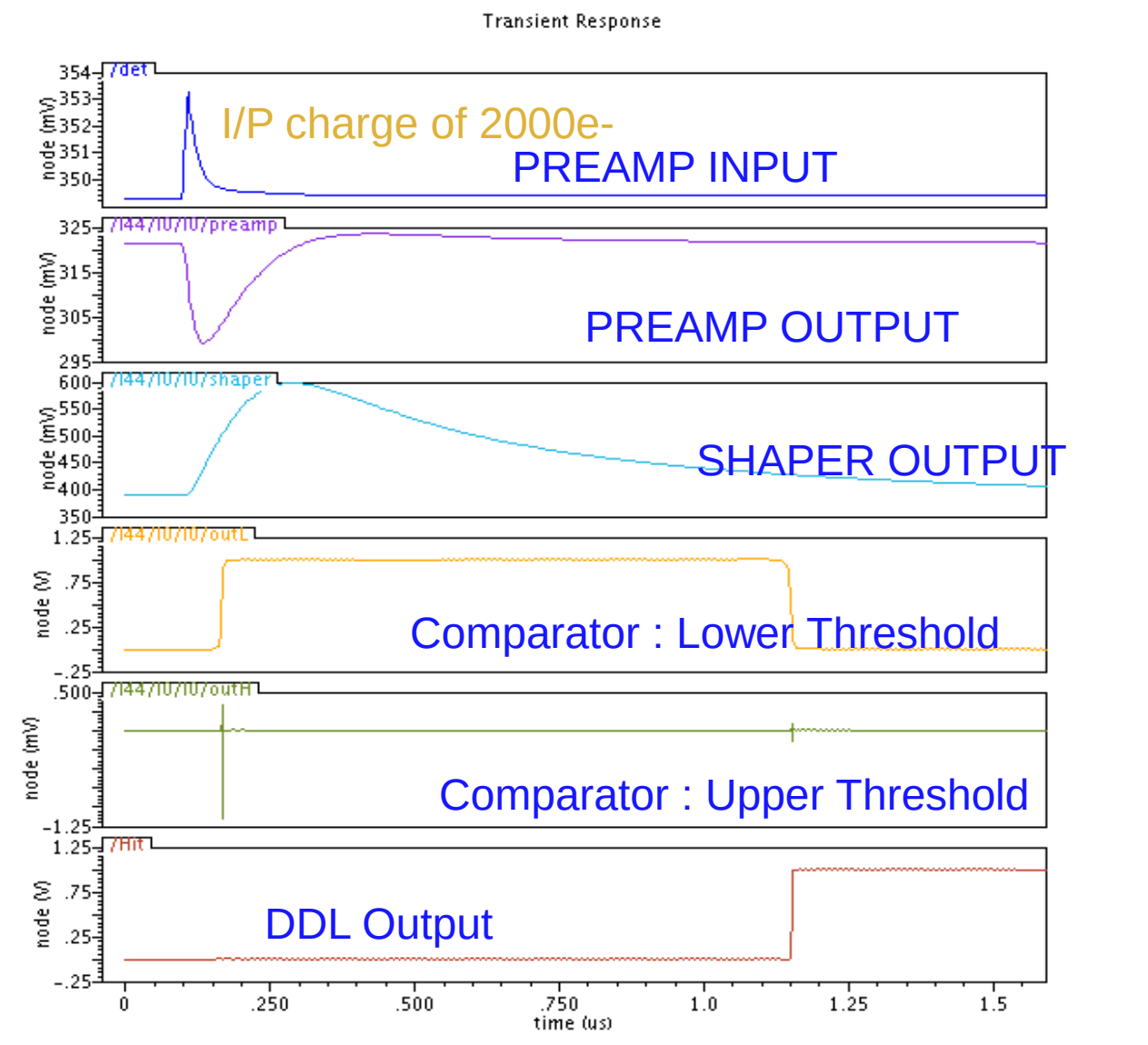
# Simulation result



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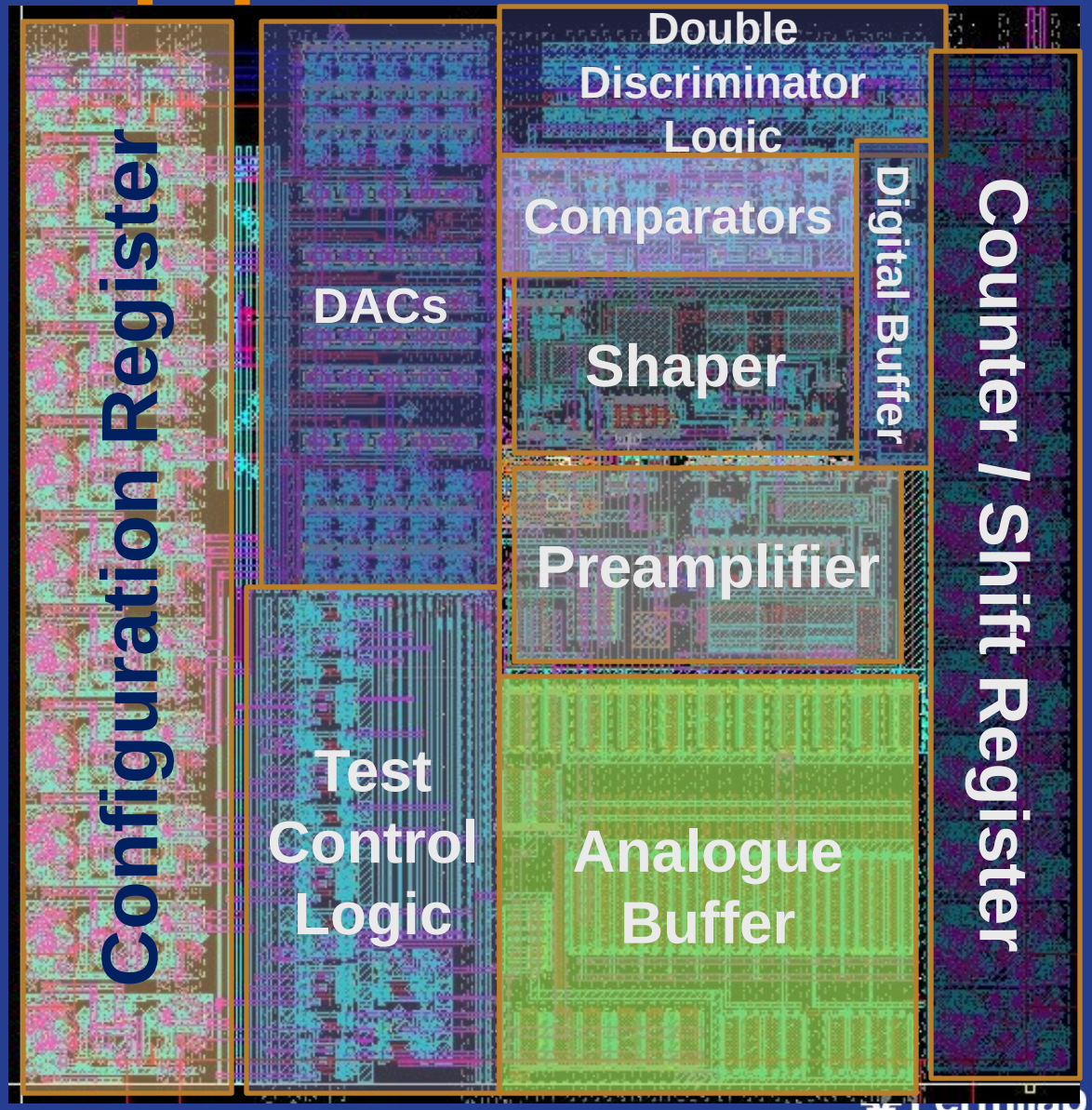
# LAYOUT

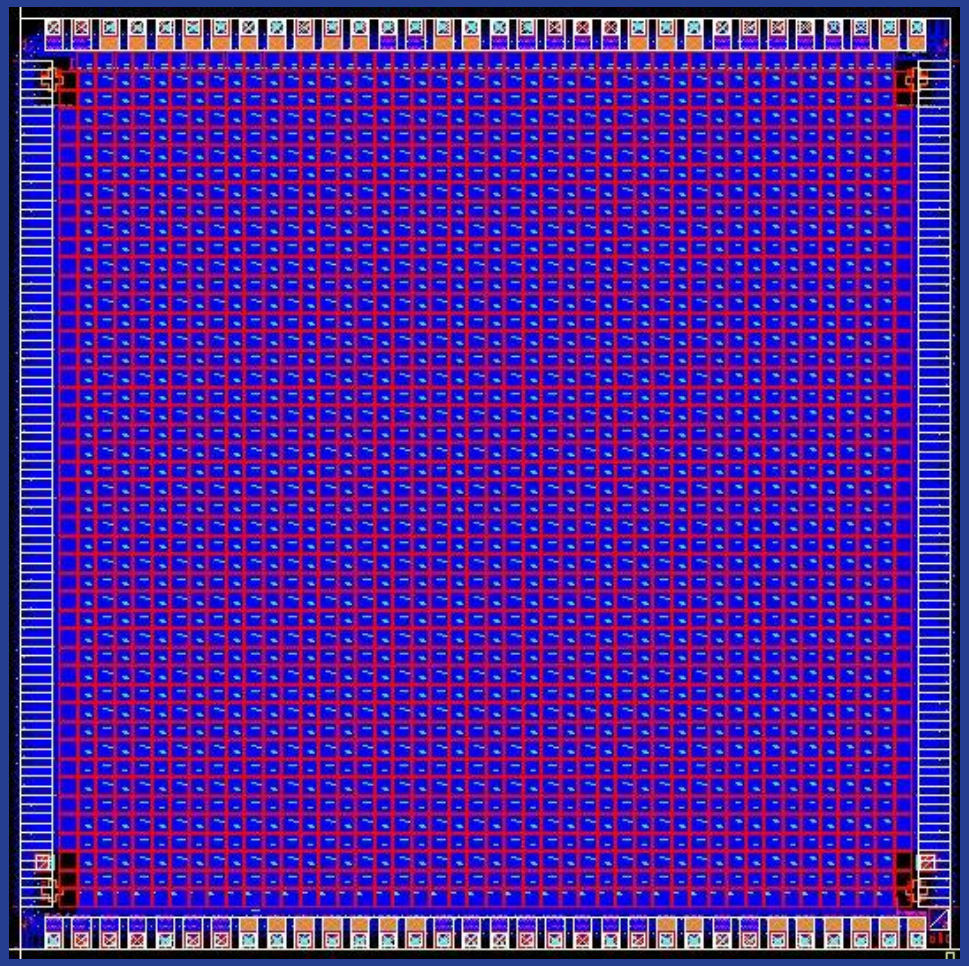
# MAMBO3: top pixel

- 100µ x 100µm
- Transistor count ~ 950
- Analogue and Digital buffers only active during single pixel test



# Upper Chip

- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- Each column has additional buffering of analog and digital signals
- Pads with back metal opening
- Alignment markers on all 4 corners

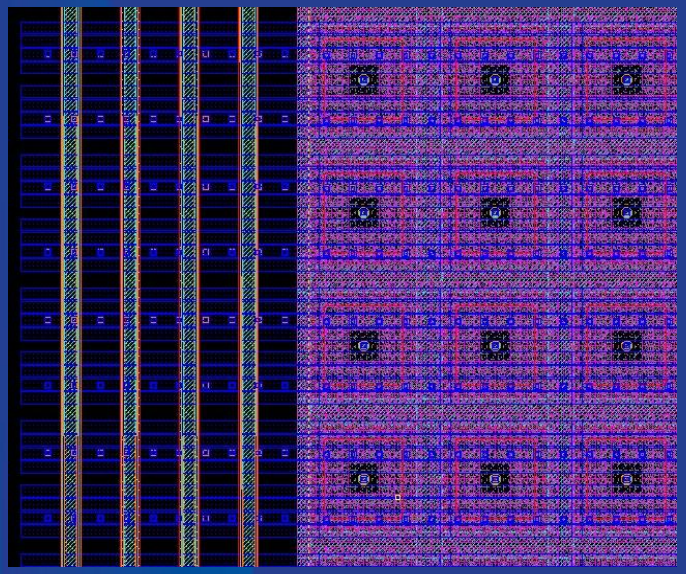


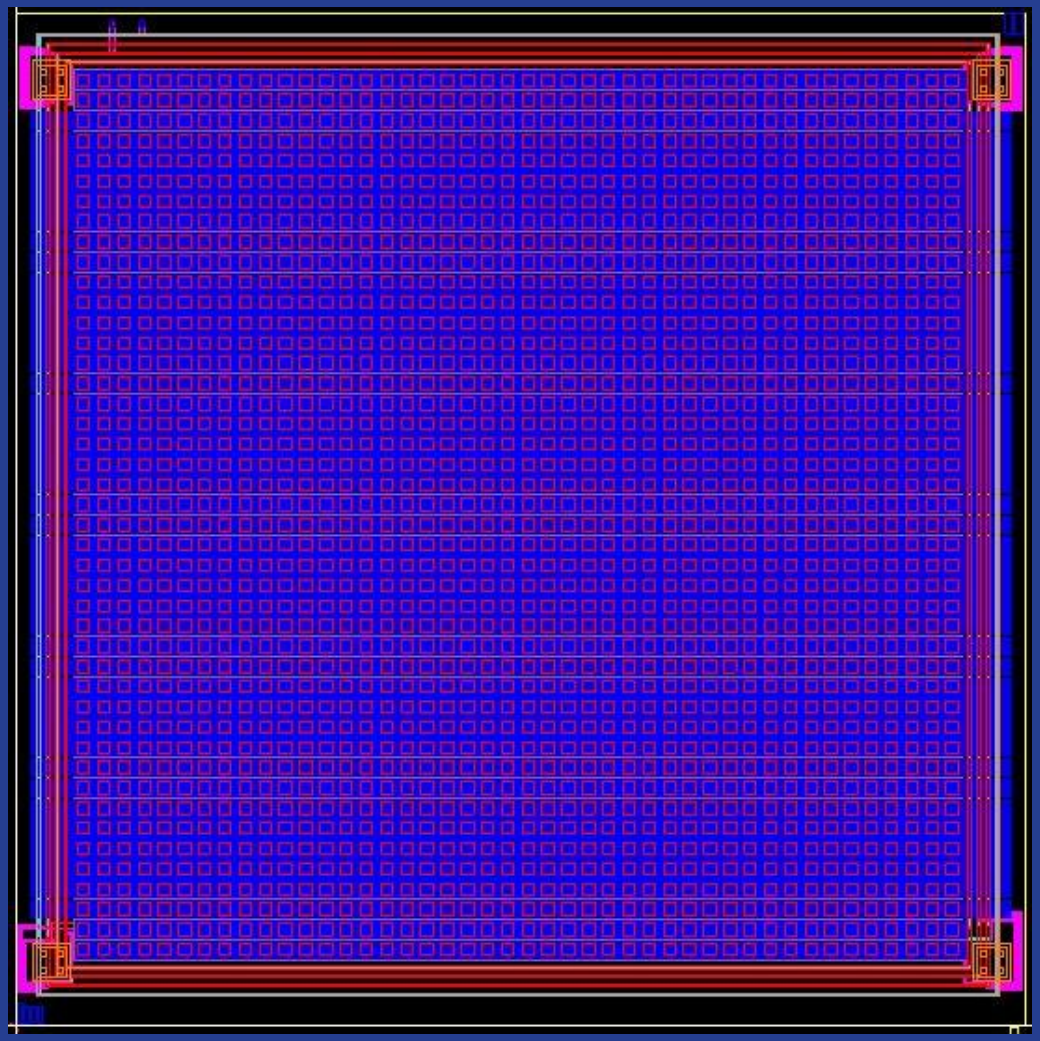
# Lower chip: Diode Pixel

DIODE

100µ x 100µ

# Lower Chip

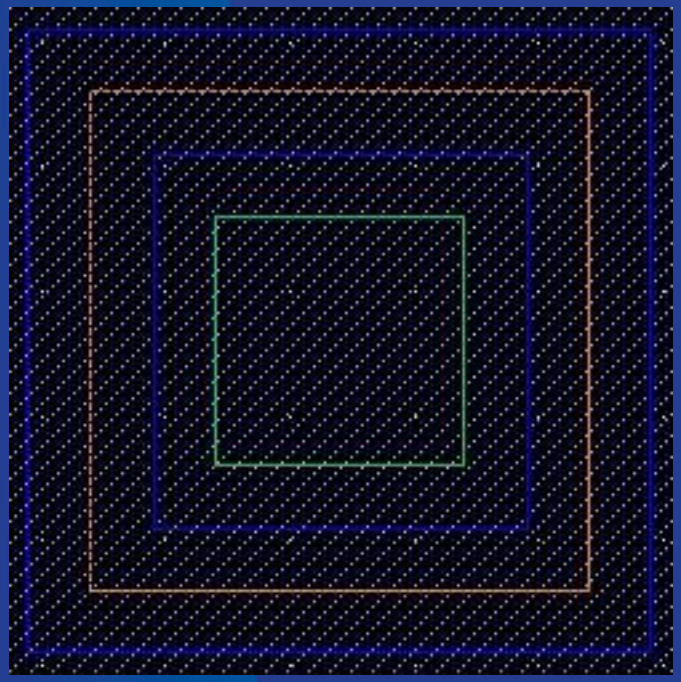


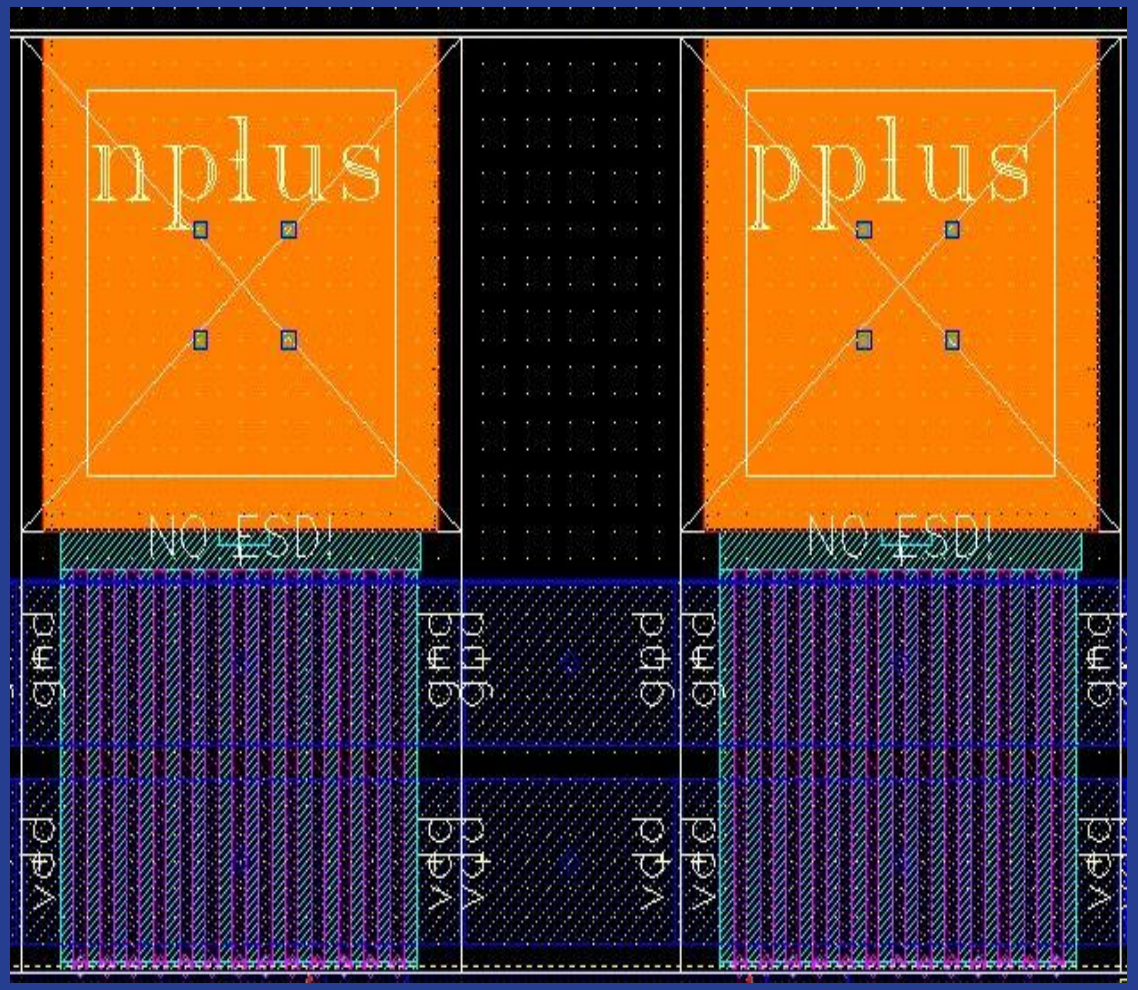


- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- 4 guard rings around the matrix
- No bond Pads contains only micro bump pads, aligned with the top chip.
- Alignment markers on all 4 corners

# Chip connection

**MICROBUMP (5µmx5µm)**






-Diode connection per pixel
-Dummy connections
-guard rings
-diode shielding (gnd!)
-gate control



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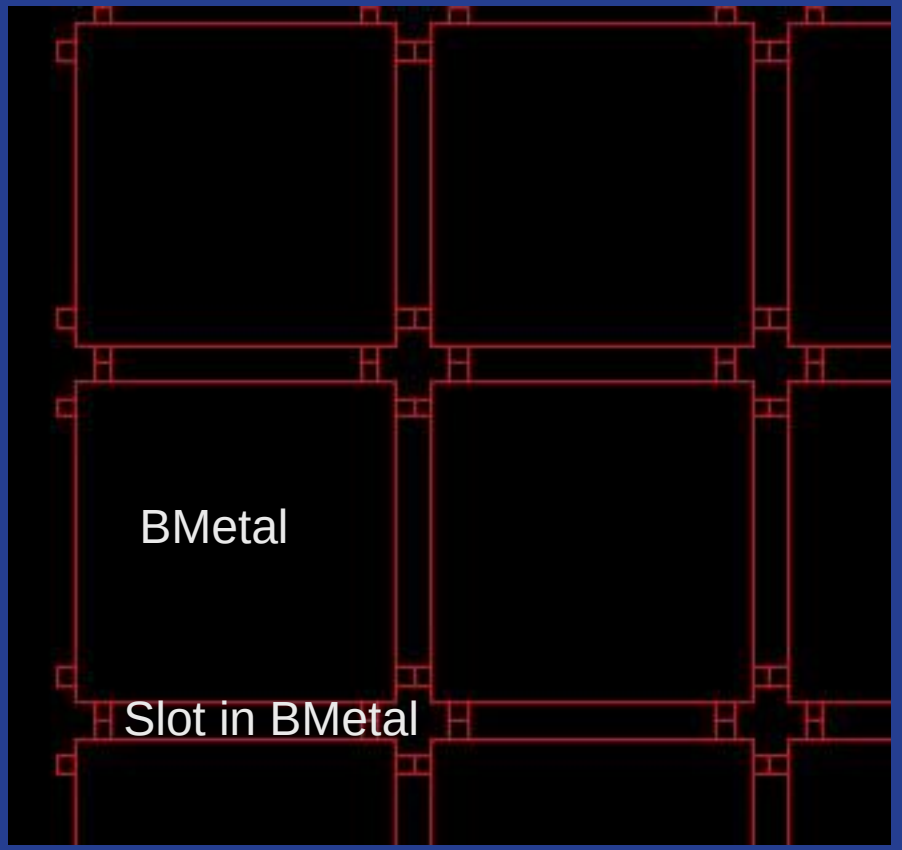
# Protection

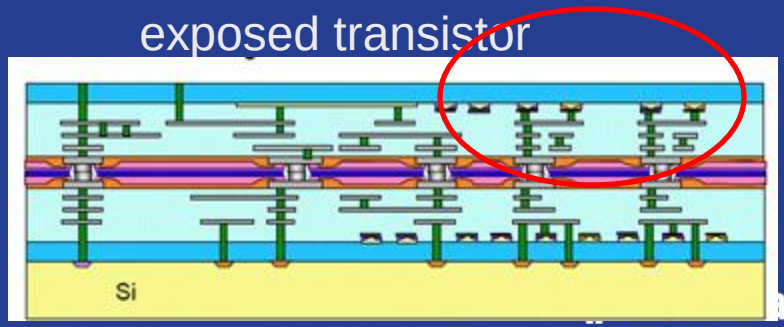
• After handle wafer is removed the bodies of transistors and sensitive nodes are exposed to electrical coupling from external environment

•Backplane connected to Analogue Ground per pixel

•Peripheral digital logic connected to Digital ground plane

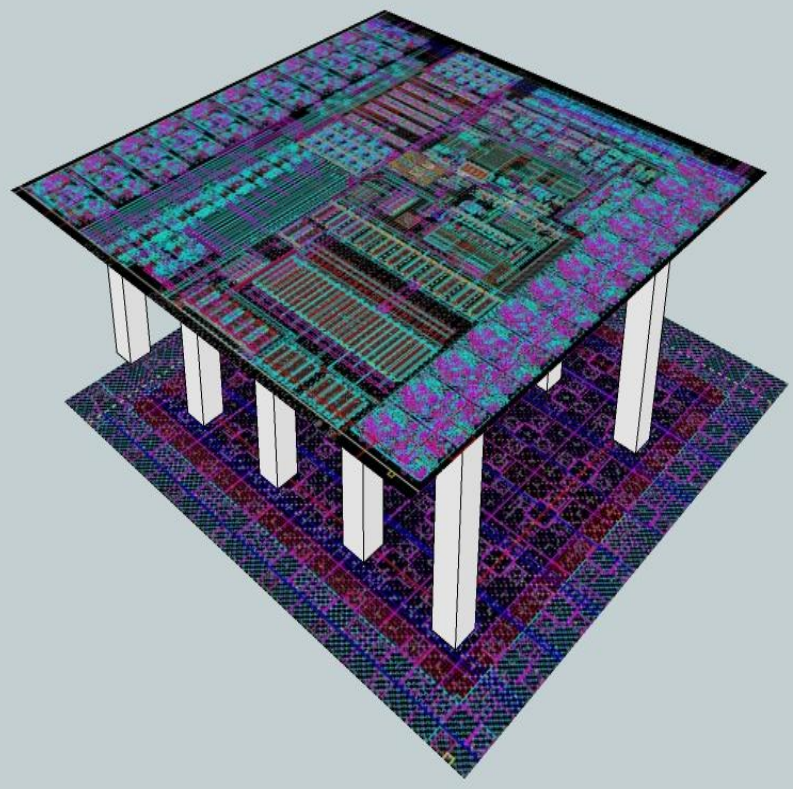


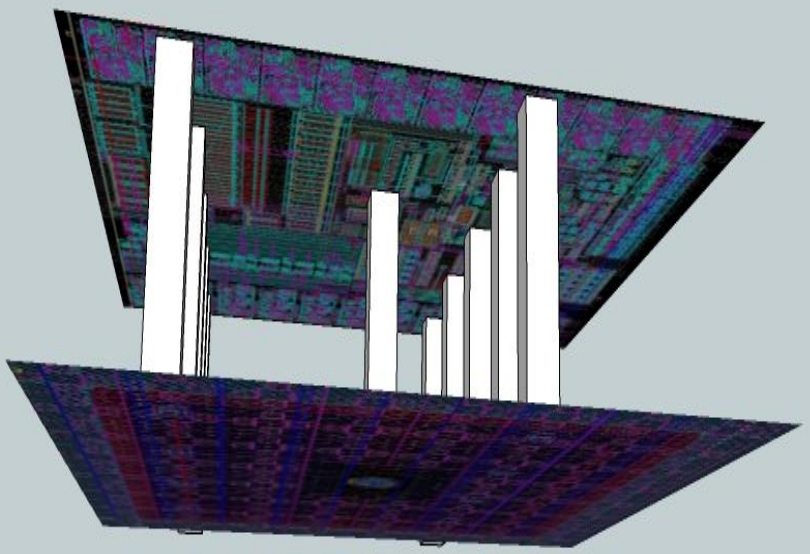

Shielding per pixel using back metal



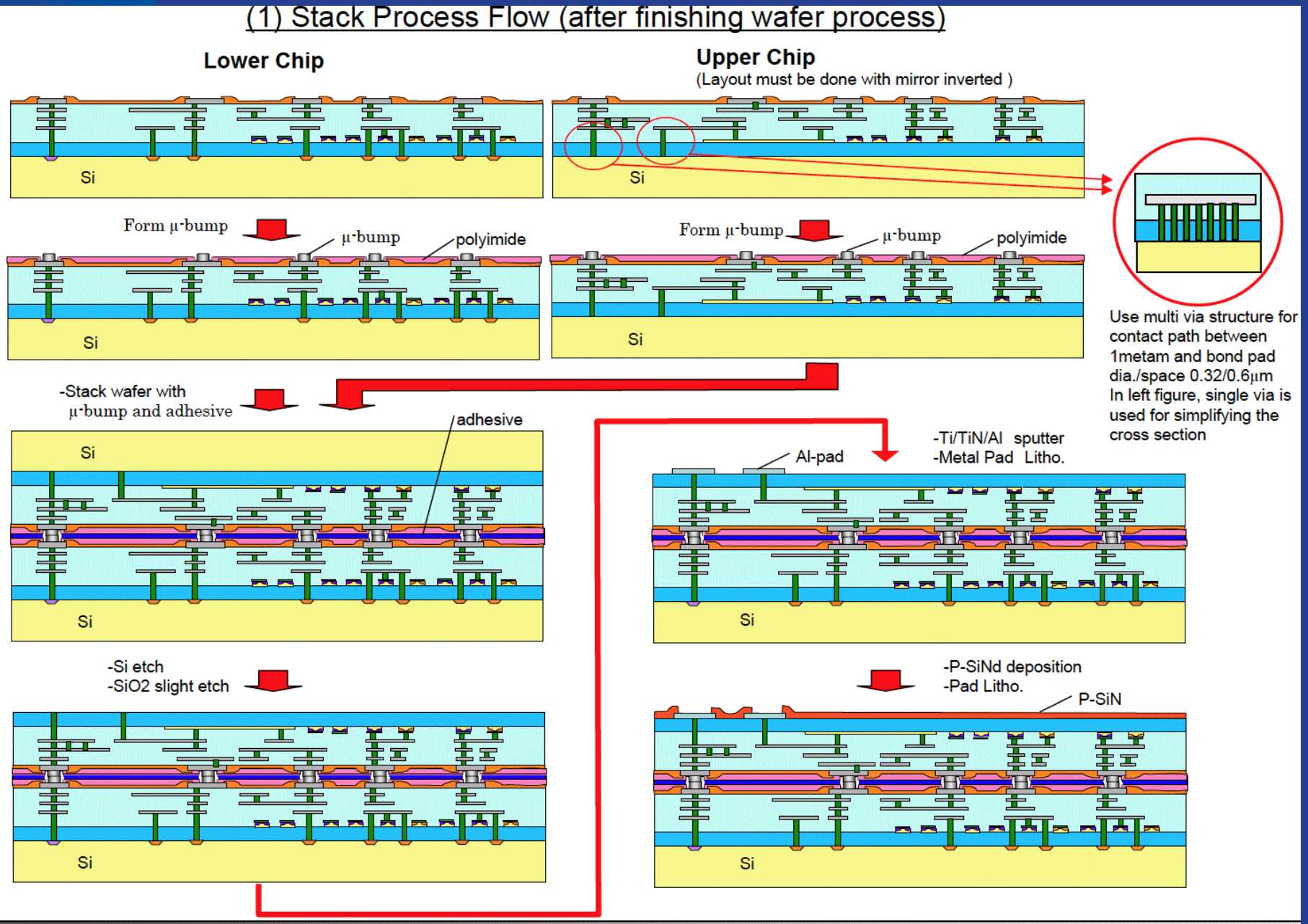
# INTEGRATION

# 3D Model

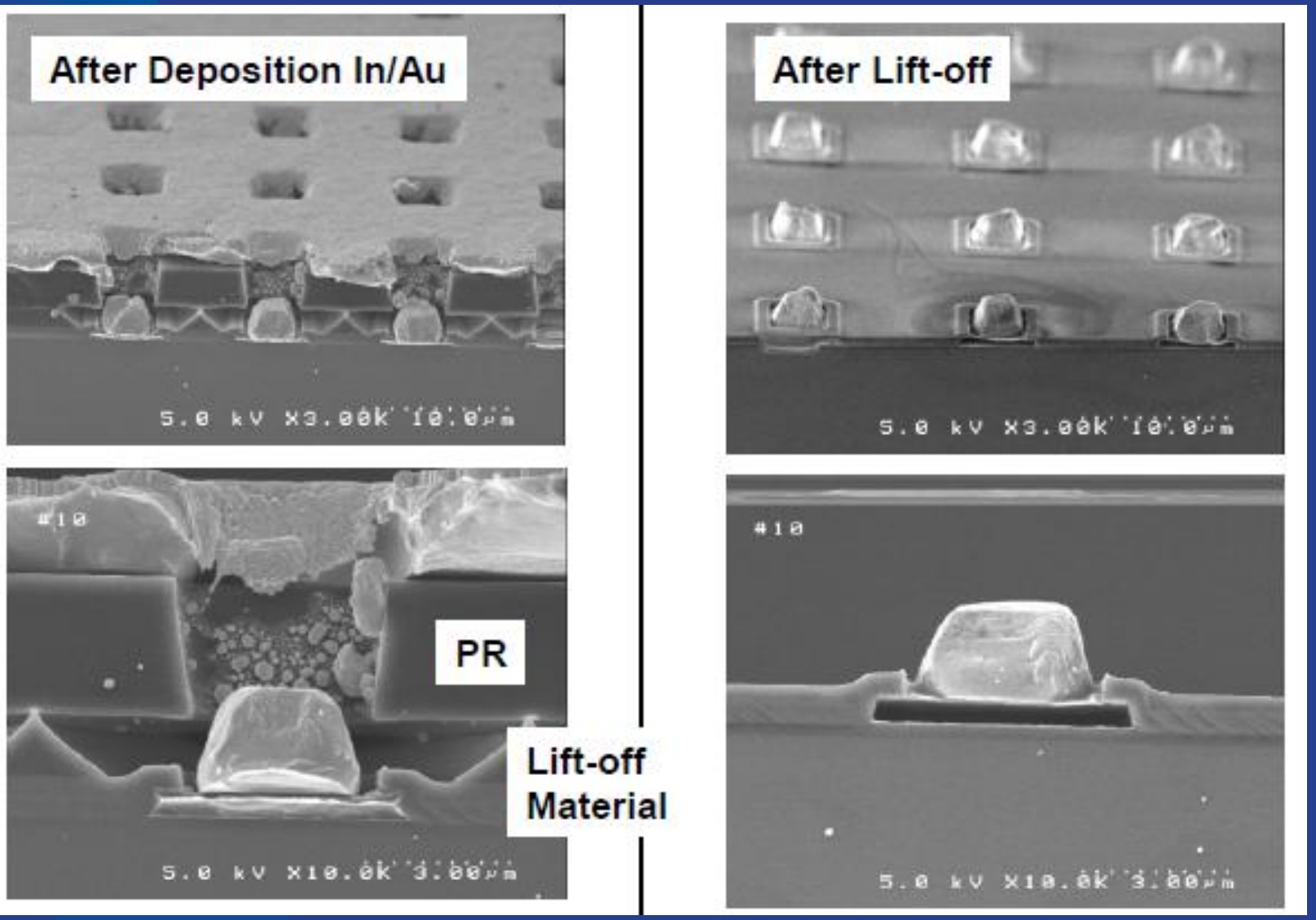




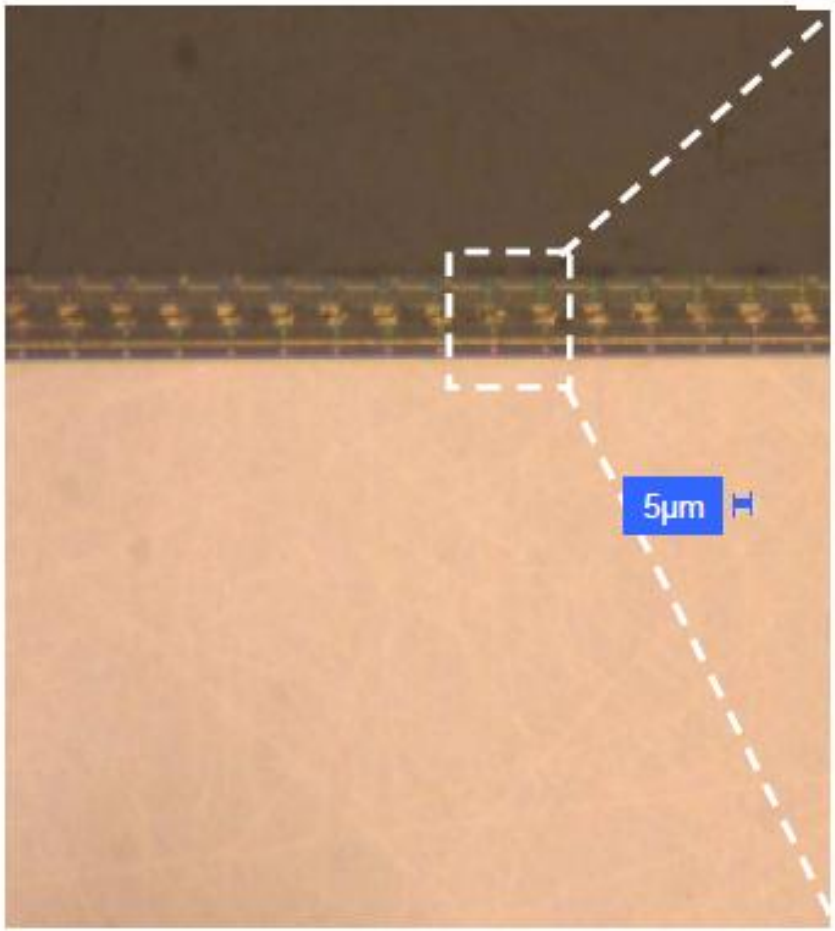
# T-Micro 3D Integration process

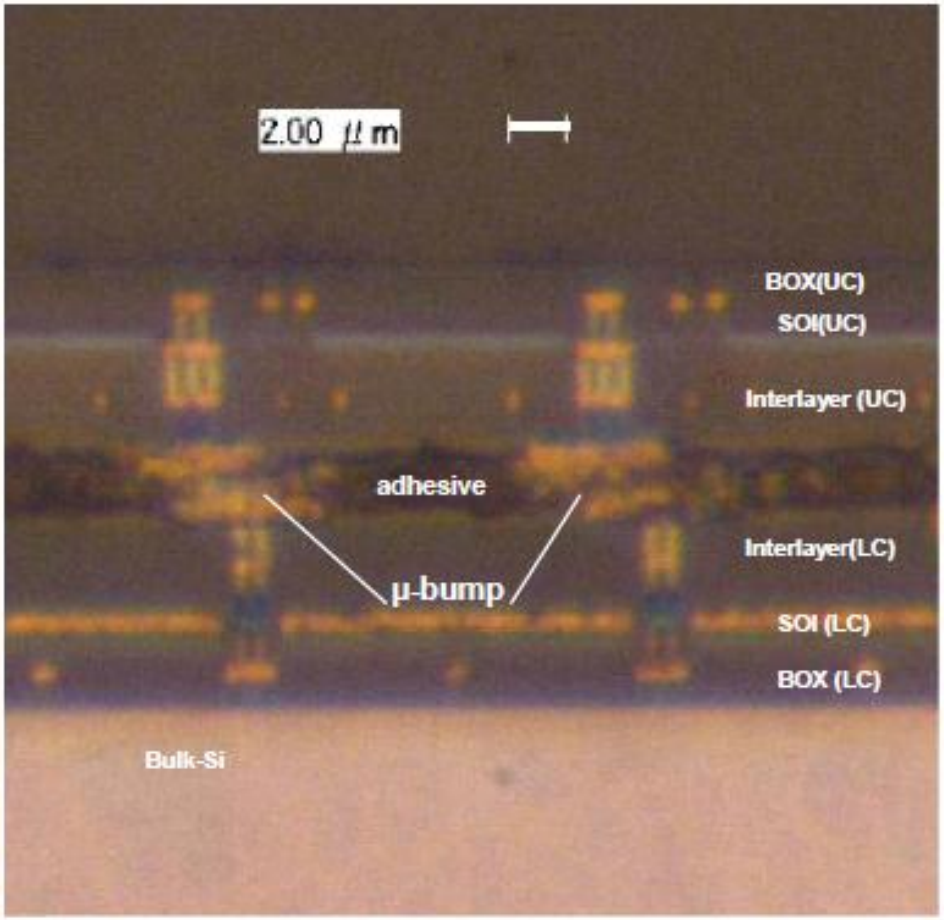


# µ-bump process



# Cross sectional view

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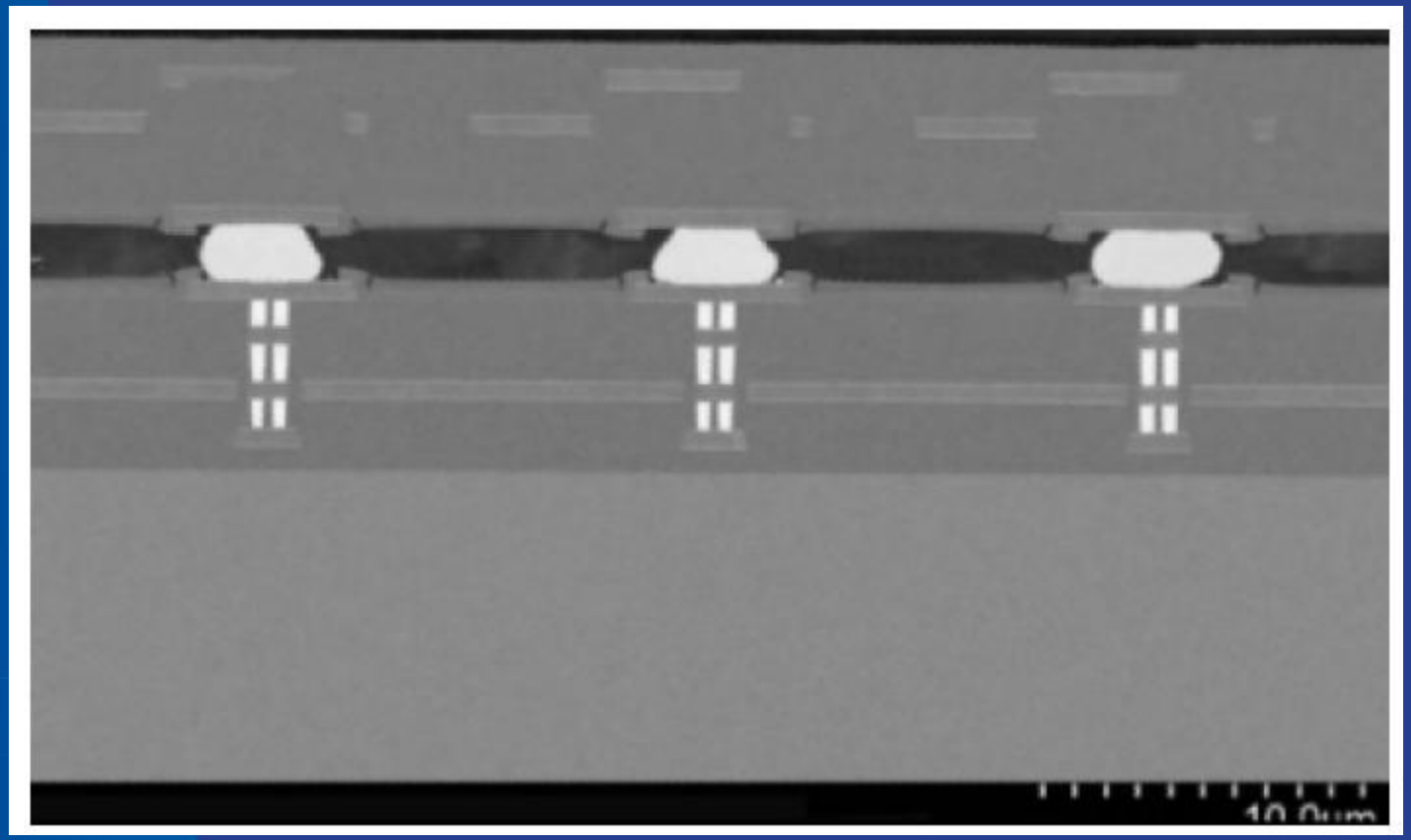
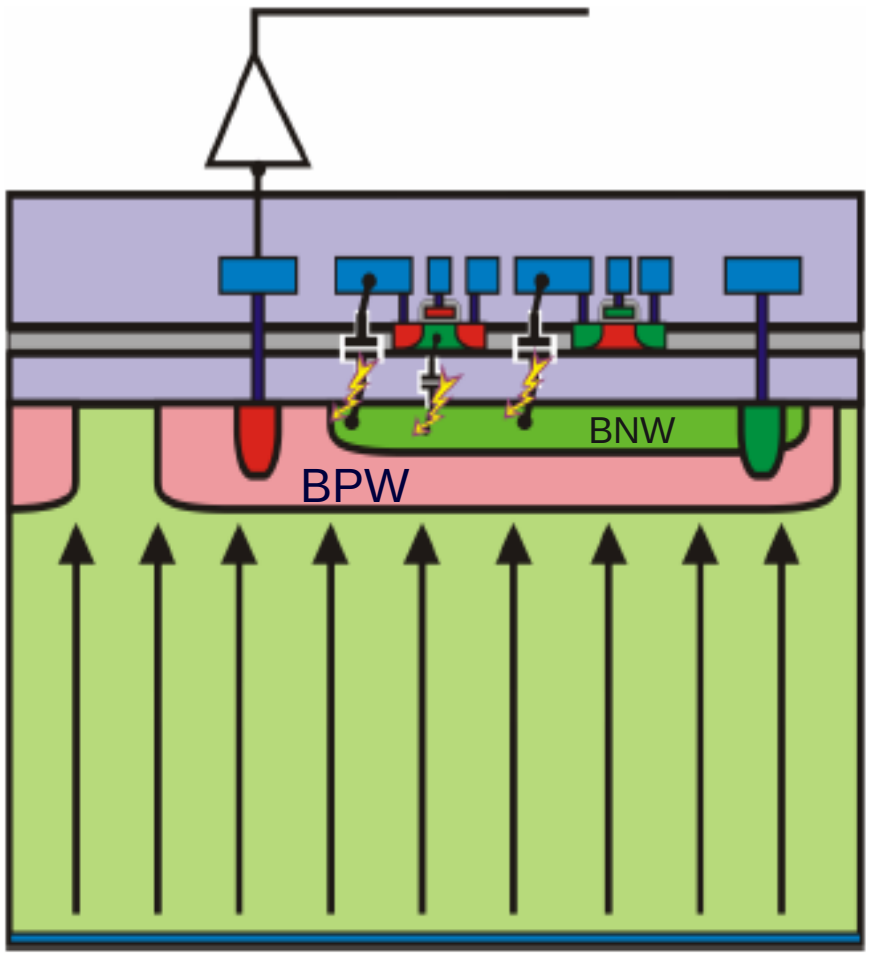
# Cross sectional view:

## Test chip with adhesive



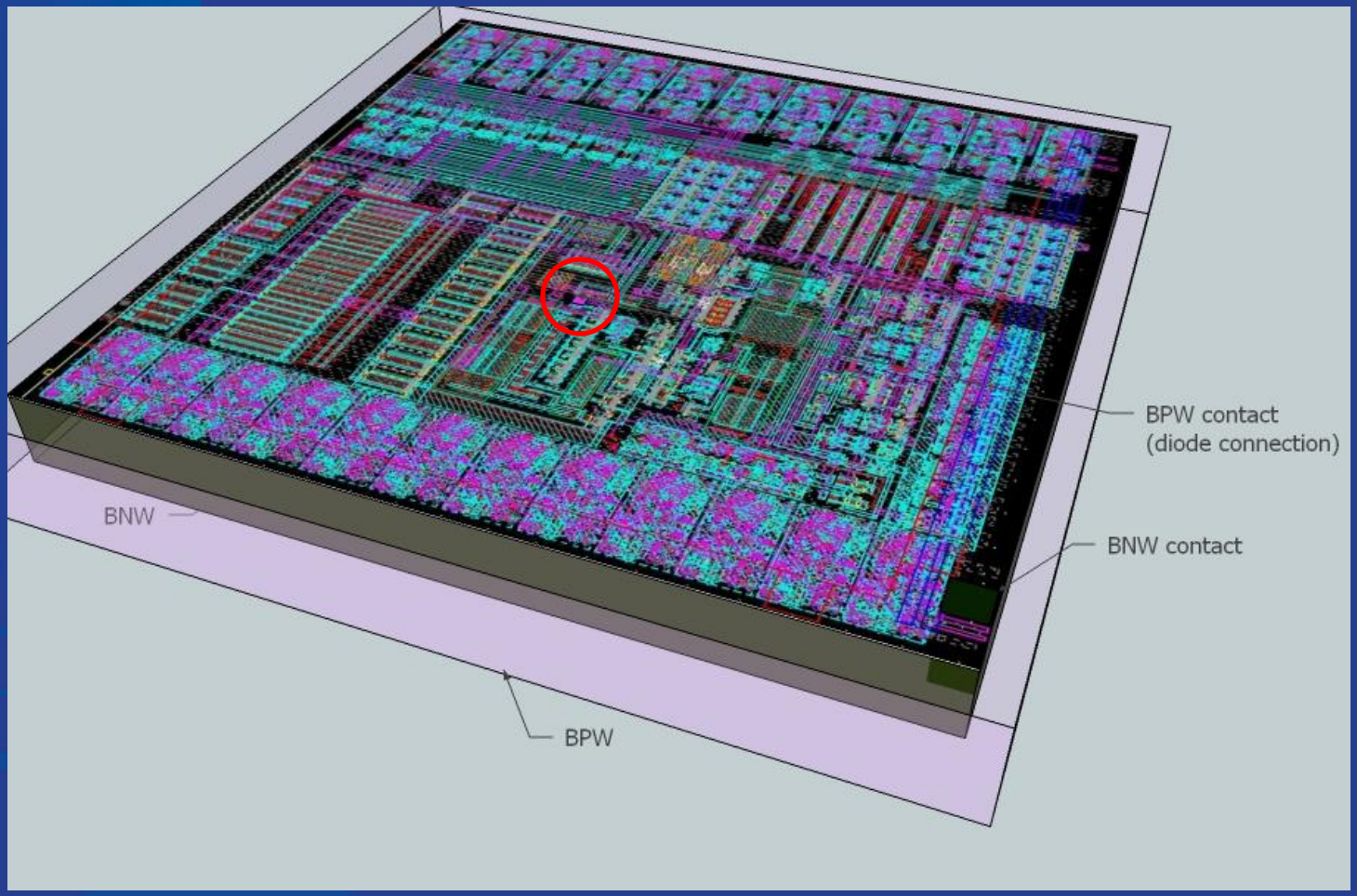
# MAMBO IV: FUTURE WORK

# Back to 2D

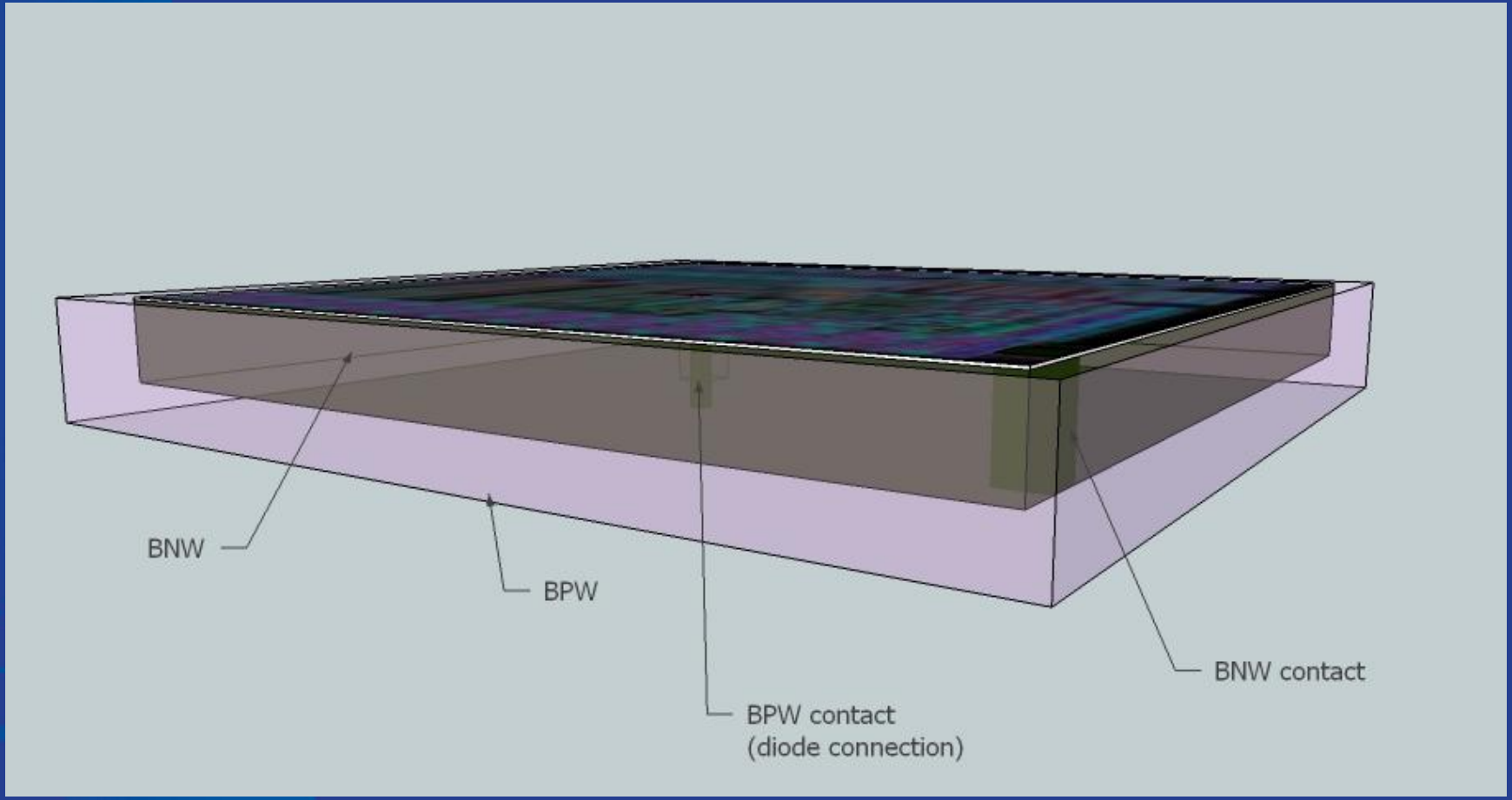



- Availability of nested well option
- BNW layer inside a deeper BPW implant
- Isolation of diode and electronics
- Increased parasitic junction capacitance (currently undetermined)

# MAMBO IV



# MAMBO IV



# Thank you