

New Concepts in Powering

for the LHC Upgrade

Mitch Newcomer

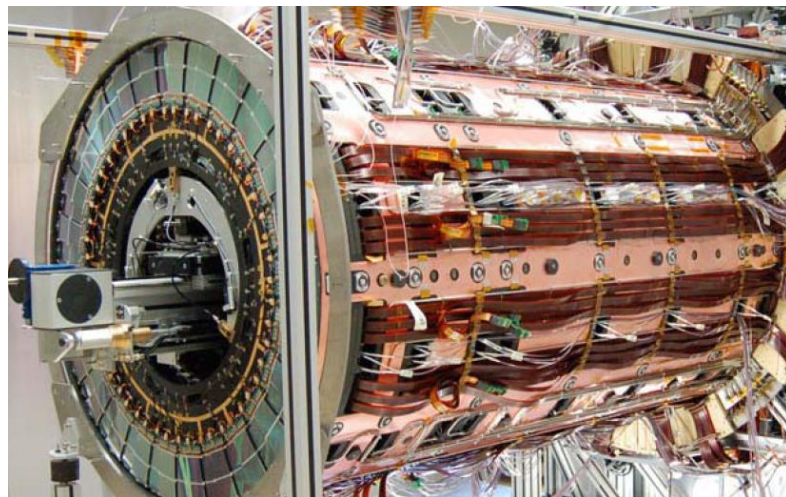
University of Pennsylvania

Trackers at the LHC

LHC Trackers wired in parallel.

Use all available cross section for cabling

Lose significant power as heat in cables.



ATLAS SCT



L. Gonella - ATLAS Upgrade Week - Apr. 2010

LHC ATLAS and CMS Silicon Trackers

ATLAS SCT

6.2M channels

3.5mW/ch

62m²

4088 Modules

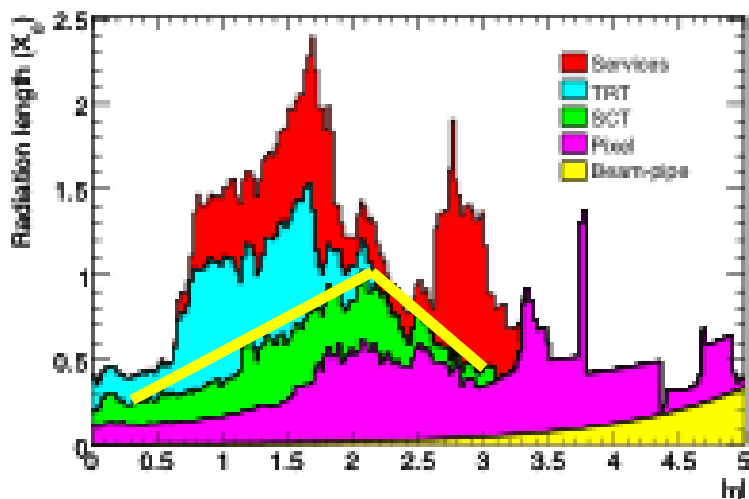
CMS Strips

10M channels

2.7mW

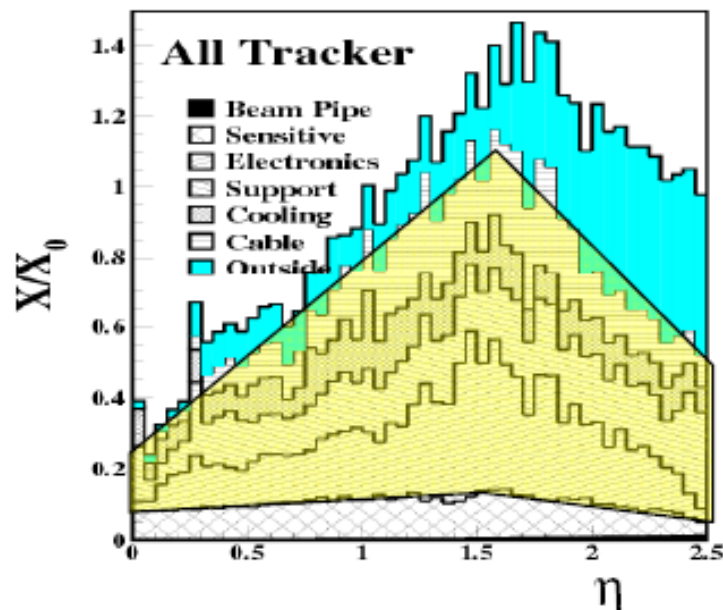
200m²

15000 Modules



ATLAS Inner Det. Material Distribution

CMS tracker material budget



Mark Raymond ACES '09
Vertex 2010

SLHC Silicon Strip Trackers

▶ **ATLAS**

6M Strips & 300k Straws → 42M Strips (150m²)

▶ **CMS** (layout proposals just beginning)

Silicon Analog RO → Digital Silicon & multiple Tracking Layers

- ▶ Higher Segmentation, more area → More channels
- ▶ Material Budget same or lower.
- ▶ Cross Section for cabling nearly Constant
- ▶ Re-use Services where possible
- ▶ Total Power the same as LHC where possible

Priorities for Upgraded Detector Power Services

- ▶ Radiation Hardness $\sim 10^{15}$ n/cm² , 50MRad
- ▶ Low Mass
- ▶ Small Additional Power dissipation
- ▶ High Reliability > 10 year operation
- ▶ Minimal Collateral loss due to failures.
- ▶ Maximum Operability - low probability of false trip, easy, low overhead restoration of power.

Powering

- ▶ **LHC** - Parallel powering voltage and current nearly the same as powered unit
- ▶ **S LHC** → FEWER POWER CABLES/MODULE
 - Higher Primary Supply Voltage
 - Lower current in cables
 - Use the same or similar cables as LHC
 - Lower fractional power loss in cables
 - Smaller cross sectional area/module for services

➔ Power reduction realized by higher density ASIC technologies (130 or 90nm) will be realized in lower **voltage**, not **current**. (Digital Power = $C_{gate} * V^2$). With more channels the current requirement may increase.

Powering Concepts

- ▶ **Serial Power** - One cable powers 'n' modules each with an equal current. (est. 80% efficiency)
 - $V_{in} = n \cdot (V_{module})$
 - Constant Current = maximum current required by any module in chain + excess for modulation contingency.
 - → Requires AC coupled Data & Control
 - → Protection Shut down Short Module (<100mV)
- ▶ **DC-DC** - $(V \cdot I)_{in} = (1/\epsilon)(V \cdot I)_{out}$ $\epsilon = efficiency$
 - V_{in} optimized as a multiple of V_{out} based on tradeoffs between reduced cable cross section and technology and other constraints. (Est 80% efficiency)
 - → Conventional DC Data & Control
 - → Protection Shut down = Open (no current)

Much of the material for this talk taken from: **The ATLAS – CMS Power Working Group Meeting March 2010**

<http://indico.cern.ch/conferenceDisplay.py?confId=85278>

ATLAS Pixel Optimization

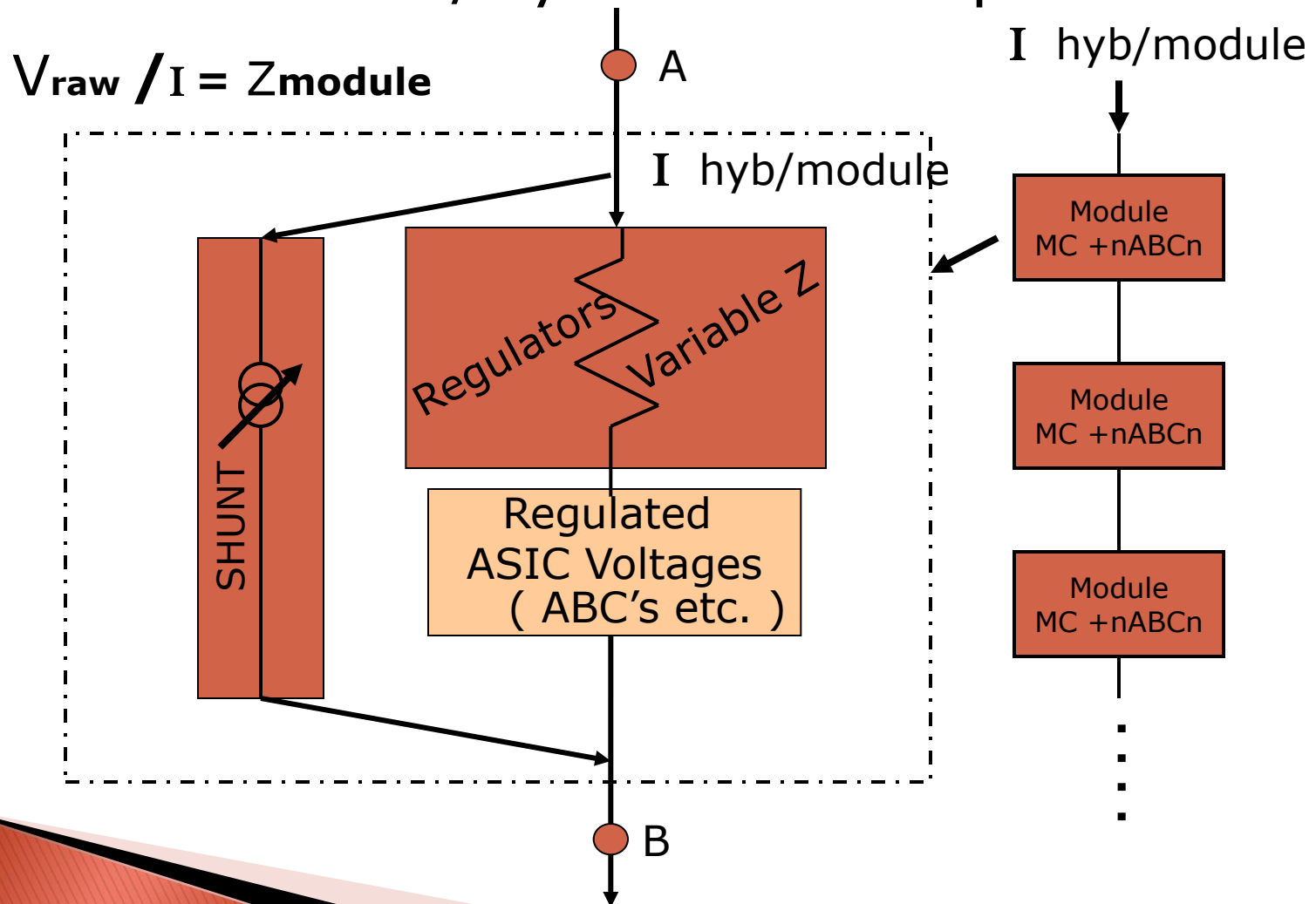
Regulators: on or off chip?

- ▶ Answer depends on the ratio of converter/detector Figure of Merits (FOM)
 - Gives the radiation thickness penalty for using converters in active areas
- ▶ FOM for silicon detectors: (load resistance) x (active area)
 - Of order of 10 $\Omega\cdot\text{cm}^2$ for pixel and 100 $\Omega\cdot\text{cm}^2$ for strip detectors
- ▶ FOM for converters: $\epsilon/(1-\epsilon)$ x (output resistance) x (rad. thickness) x (area)
 - Typical FOM of external converters are in the order of 1-5% $\text{RL}\cdot\Omega\cdot\text{cm}^2$ at 80% efficiency
- ▶ This gives a penalty of 0.5% RL per layer for pixels and $\sim 0.05\%$ RL for strips
- ▶ A penalty $>0.2\%$ RL per layer is regarded as too severe
- Only strips can use external converters
- ➡ Pixel detectors must use internal (on-chip regulators) which usually have a FOM of less than 0.5% $\text{RL}\cdot\Omega\cdot\text{cm}^2$ (just the external blocking capacities)

L. Gonella - ATLAS Upgrade Week - Apr. 2010

Serial Power

Module/Hybrid Current path



Serial Power

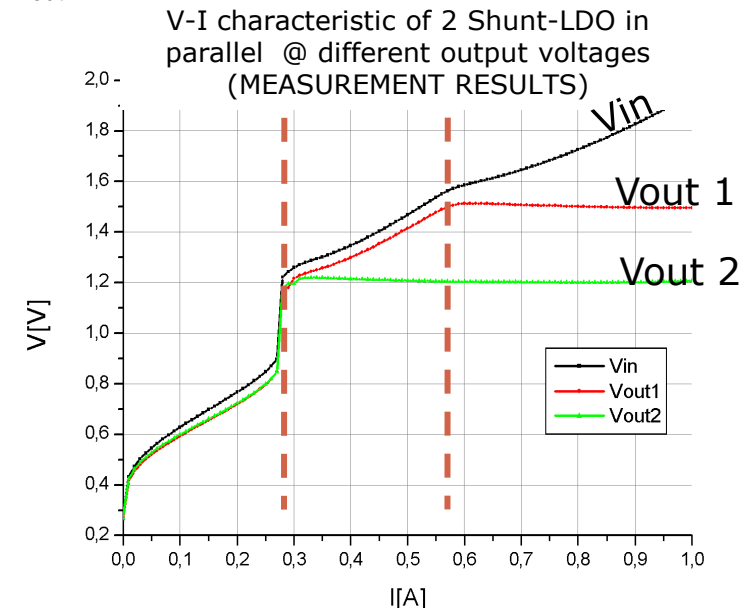
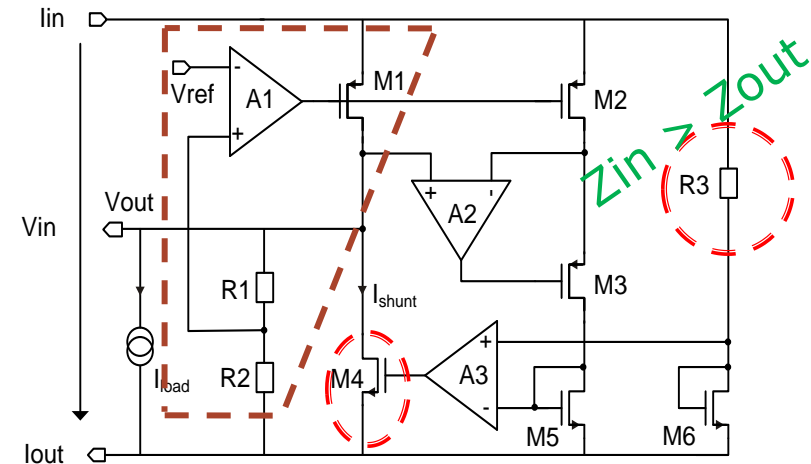
Several possible approaches have been implemented:
Available technology is sufficient for “at” scale prototyping.

- ▶ Bonn - SHUNT-LDO for ATLAS Pixels
- ▶ FNAL - SPI chip Self Contained Shunt ASIC
- ▶ Penn - Distributed Shunt (through FEIC's)
- ▶ Krakow - SCT Shunt Load Shared and regulated in each ABCn. Fabled in ABCn & Tested with SCT modules.

ATLAS Pixels

SP Shunt-LDO

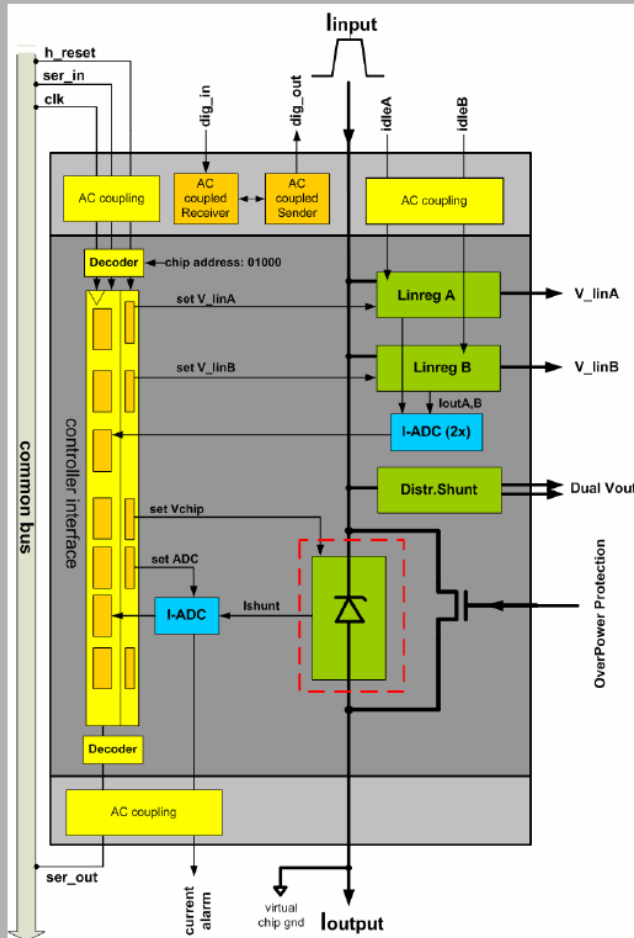
- ▶ Combination of a LDO and a shunt transistor
 - Shunt transistor is part of the LDO load
 - LDO power transistor works as an input series resistor for the shunt
- ▶ Advantages for Serial Power
 - **Shunt-LDO regulators can be placed in parallel without problems regarding mismatch & shunt current distribution**
 - Also, Shunt-LDO having different output voltages can be placed in parallel
 - Shunt-LDO can cope with an increased supply current if one FE-I4 does not contribute to the regulation
- ▶ Working principle and good performance demonstrated with 2 prototypes already
- ▶ **Nominal Power Efficiency** of 2 Shunt-LDO in parallel with different $V_{out} = 75\%$ (calc.)



Shunt - LDO Michael Koragonis

FNAL SPI (Serial Powering Ic)

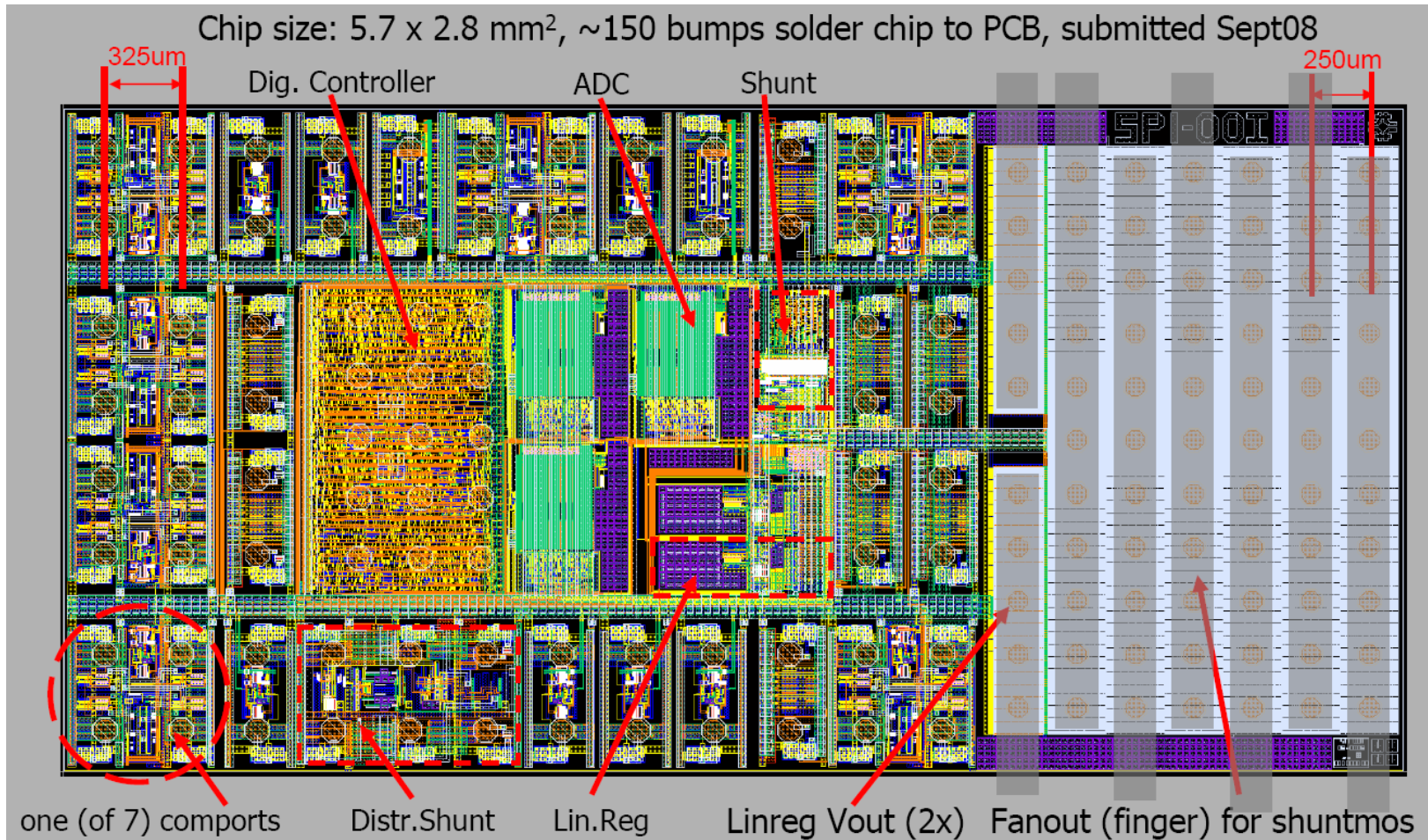
SPI - Architecture Overview



main focus on versatility - list of basic features:

- **shunt** creates V_{chip} 1.2...2.7V, 4A (scheme1), distr. shunt (scheme3)
- communication via **multi drop** bus (each SPI chip has 5bit address) reduces number of str.-lines for SPI to minimum of 2 (3)
- AC coupled LVDS, spare interface port (**comports**)
- **ADCs** to monitor shunt and LR current
- current alarm with programmable threshold and trigger delay
- **OverPower** protection: power FET to bypass module
- **2x LinReg**: separate analog / digital supply: 1.2 .. 2.5V optimal feature to hook up some chips (1-3) for tests
- **radtol. design** techniques, TSMC 025MM process

Layout of SPI Chip



SPI chip Tests

ABCn demonstrator stove

Module Controller Chip (MCC)

- Functions common to SP & DC-DC
 - multiplexes 2 data streams into 1
 - voltage monitoring
- Additional for SP
 - powered by SP
 - AC coupling of CLK & COM
 - Requires 4 capacitors
 - Everything else on chip

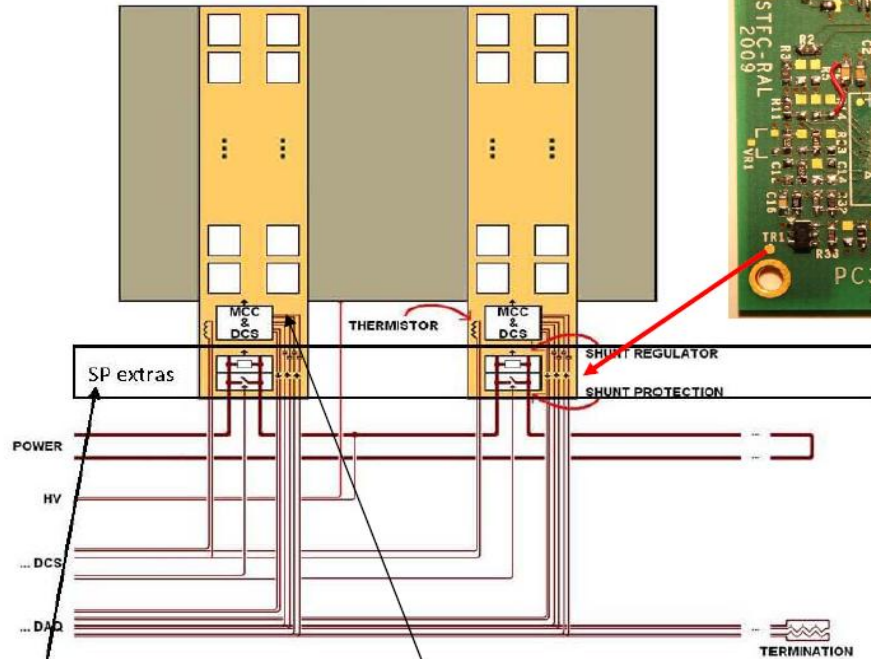
Temperature

- read by (stave end) DCS
 - Monitor T before power applied

Shunt protection

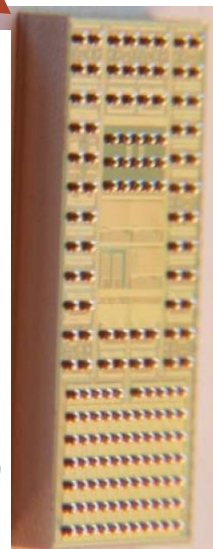
- under DCS control
 - Turn on modules independently

SP requires minimal extra circuitry at the module end



one module is already running SP using SPi at RAL

Bump Bonds for High current Shunt



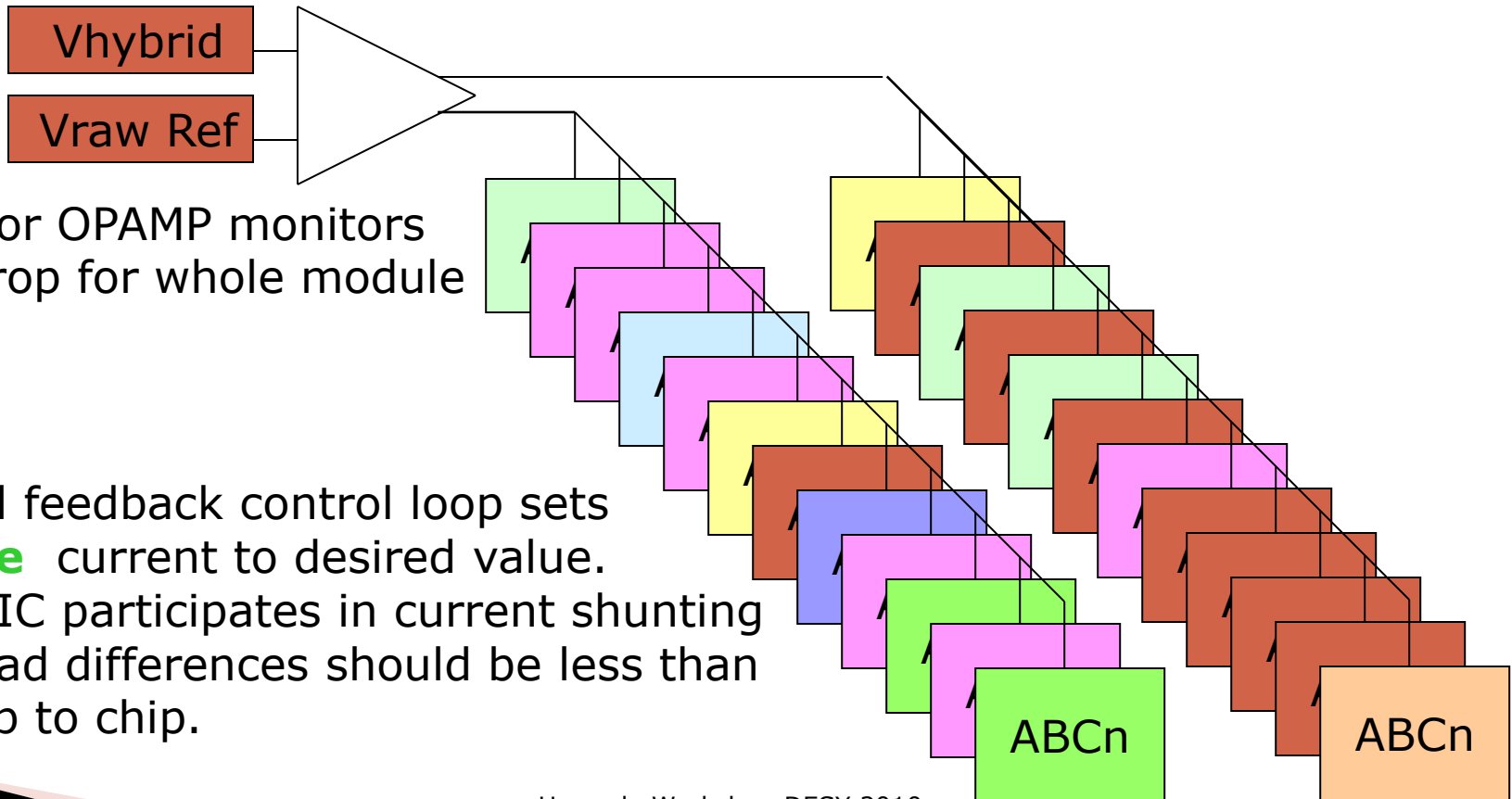
SPI under test for CMS Pixels see talk of Aida Todri, FNAL at PWG 2010 meeting.

SP Distributed Shunt

Module/Hybrid for ATLAS SCT

“Xtra material”
OP amp & traces & Protection

Power current path **distributed**
among ABCn chips. No interruption.



Regulator OPAMP monitors
Vraw Drop for whole module

External feedback control loop sets
Average current to desired value.
Each FEIC participates in current shunting
Heat load differences should be less than
2% chip to chip.

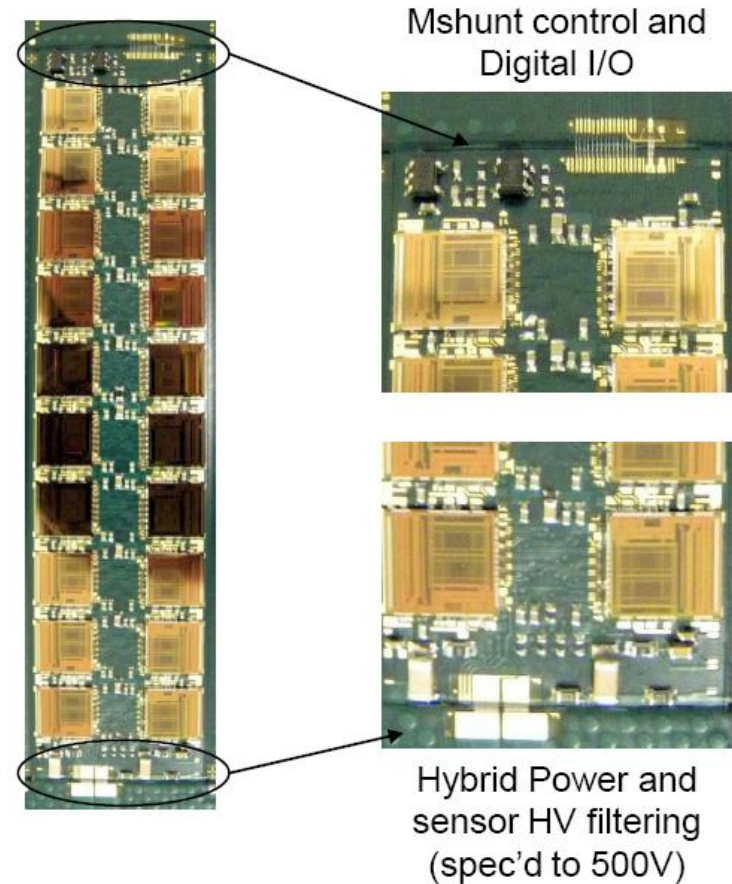
Upgrade Workshop DESY 2010

SP Distributed shunt Some Advantages

- **Existing Technology is sufficient.**
- **Largest FEIC shunt Current 200mA.**
- **Largest Power Diss $\sim 50\text{mW}/\text{FEIC}$**
- **Many Amps reserve Regulation.**
- **No Xtra Devices in Current Path**
- **Impact on Material Budget Minimal.**
- **No oscillators or RF components.**
- **200ns Response Time.**
- **AC communications not difficult to implement.**

Simplicity.

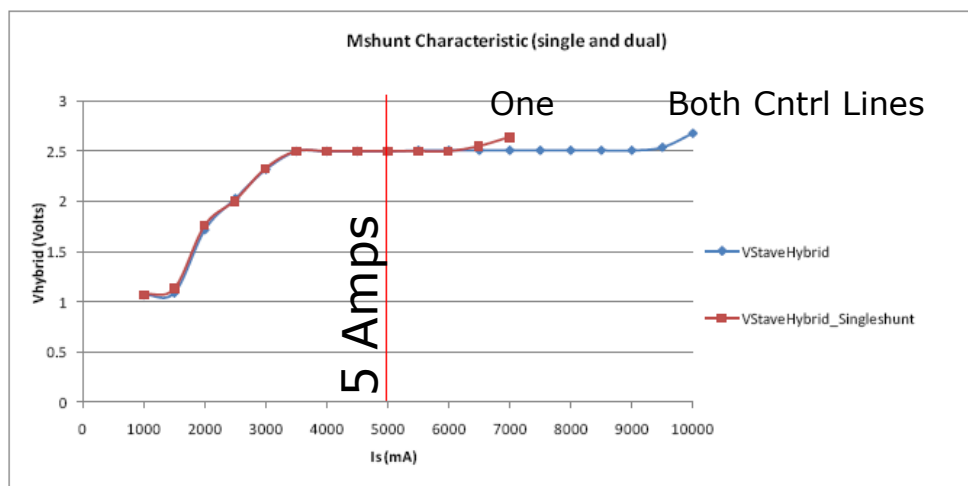
Default prototype power scheme



Hybrid powering

Hybrids are designed for two powering schemes:

1. Parallel power, which could be provided by DCDC converters
2. Shunt regulation, using the distributed shunt regulators integrated within the ABCN-25s
 - Required for serial powering – Mshunt is the default scheme



Mshunt characteristic for single and dual shunts enabled per ABCN-25 on a 20 ASIC hybrid (expect max. Hybrid shunted current to be $\leq 5A$)

Single Shunt transistor enabled per ABCN-25 (20 x shunt transistors)

Shunt regulates V_{hybrid} to 2.5V at $I_s > 3.5A$ and diverges at $I_s < 6.5A$ (cf $I_{hybrid} + I_{smax} (3.6 + (20 \times 0.14))) = 6.4A$

Dual Shunt transistors enabled per ABCN-25 (40 x shunt transistors)

Shunt regulates V_{hybrid} to 2.5V at $I_s > 3.5A$ and diverges at $I < 9.5A$ (cf $I_{hybrid} + I_{smax} (3.6 + (40 \times 0.14))) = 9.2A$

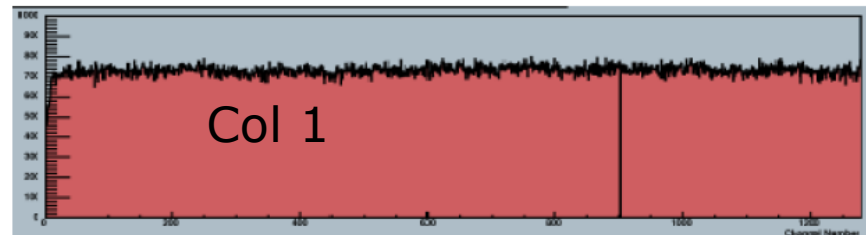
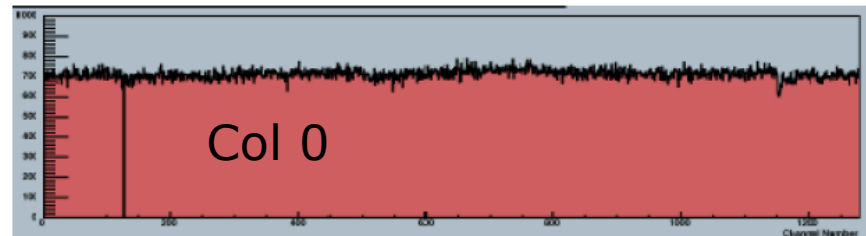
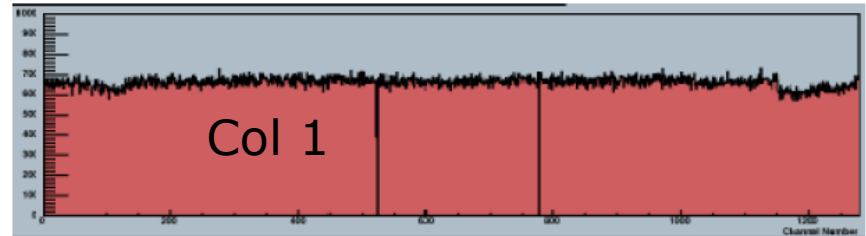
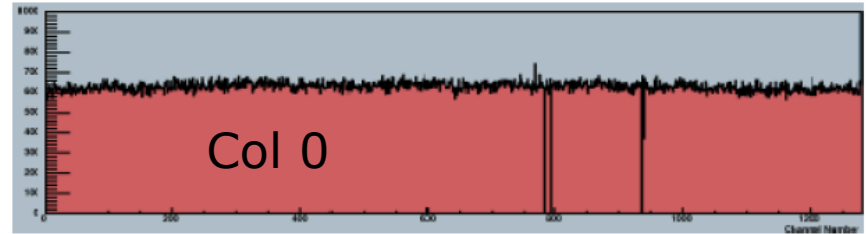
DC-coupled hybrid

- Input Noise, Column 0: 628e,
Column 1: 660e
 - Noise unchanged

Initial measurement AC-coupled hybrid

- Input Noise, Column 0: 712e,
Column 1: 728e
 - Noise increase of ~70e (due to AC-coupling of 3.3 V LVDS?)
 - System grounding could also still be improved
- Will see if BCC (2.5 V LVDS powered from hybrid is better)

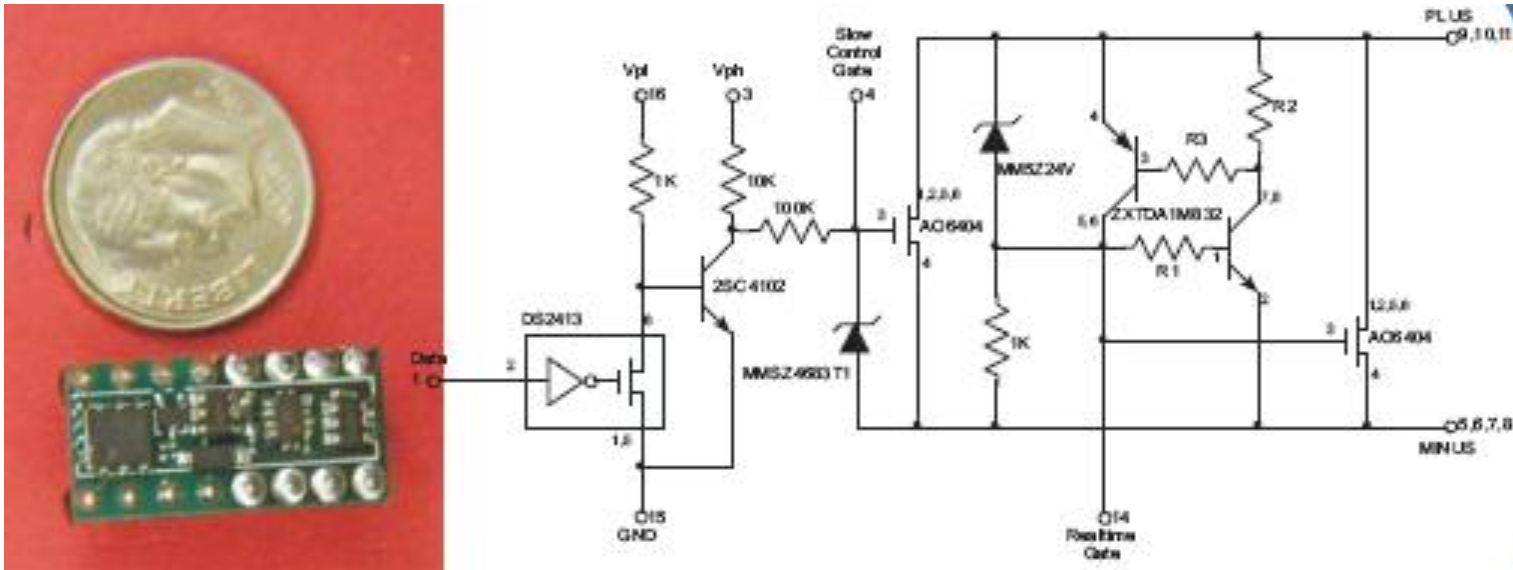
Serial Powered Module Works!



ATLAS SCT Serial Power Protection

Serial Powering near short across the module to shut it down.

BNL designed a PCB based protection board using commercially available parts that offers both addressable power on/off and an **autonomous shunt shut down**. It will be used for testing with stavelets, 8 serially connected hybrids and stave 09, 24 hybrids.



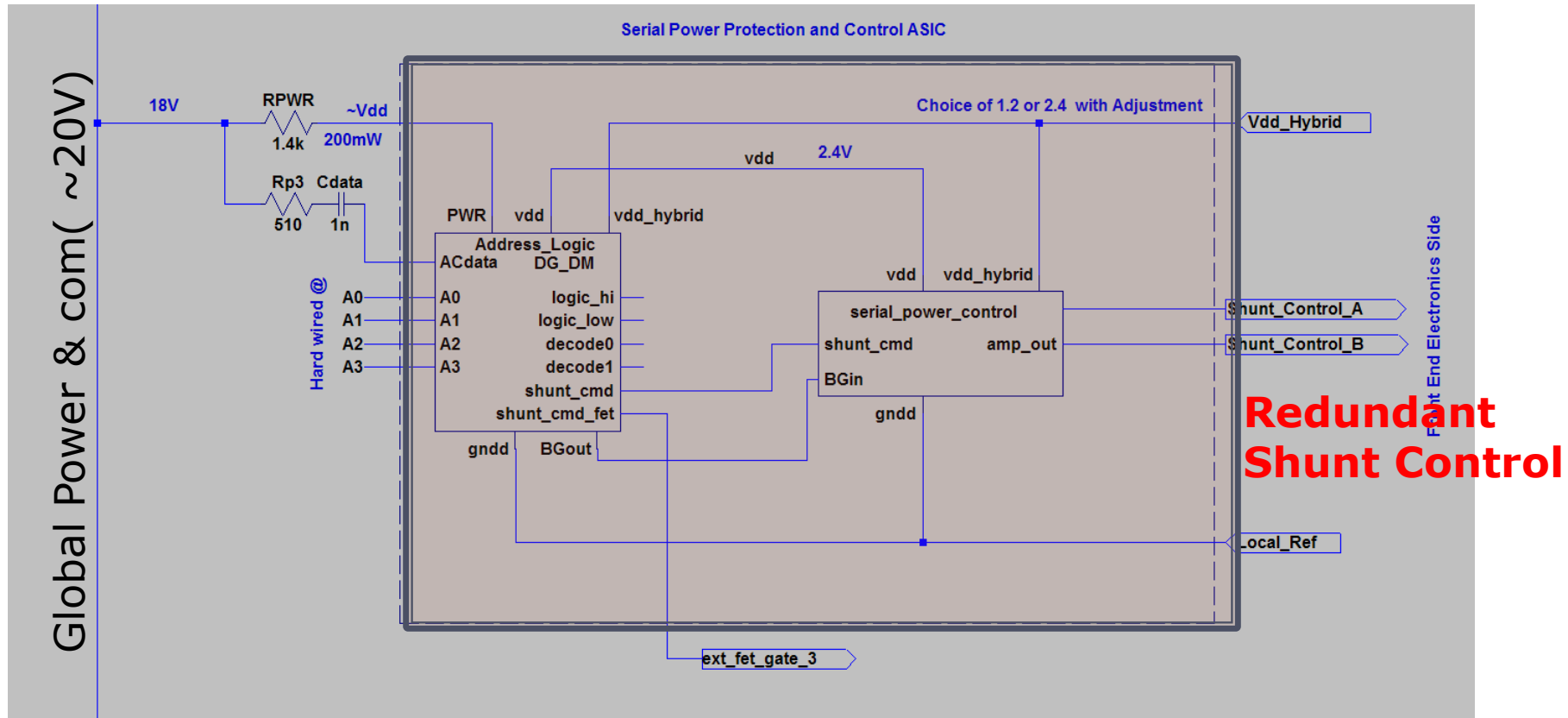
SPP- Serial Power (control) & Protection ASIC

→ One chip solution using the same 130nm technology as FEIC's.

- Separate power ,compatible with ABCn 2.4V & ABC130 1V
- Can satisfy radiation tolerance requirements.
- Offers Serial Power regulation.
- Autonomous fault detection and shut down.
- Individual addressable power control "on" and "off".
- Single additional line on stave bus for power and PWM addressing.

Serial Power & Protection ASIC

130nm DG transistors for 2.4V Analog and Digital logic on chip.
 ~ 6mA current draw → ~15mW for the ASIC.



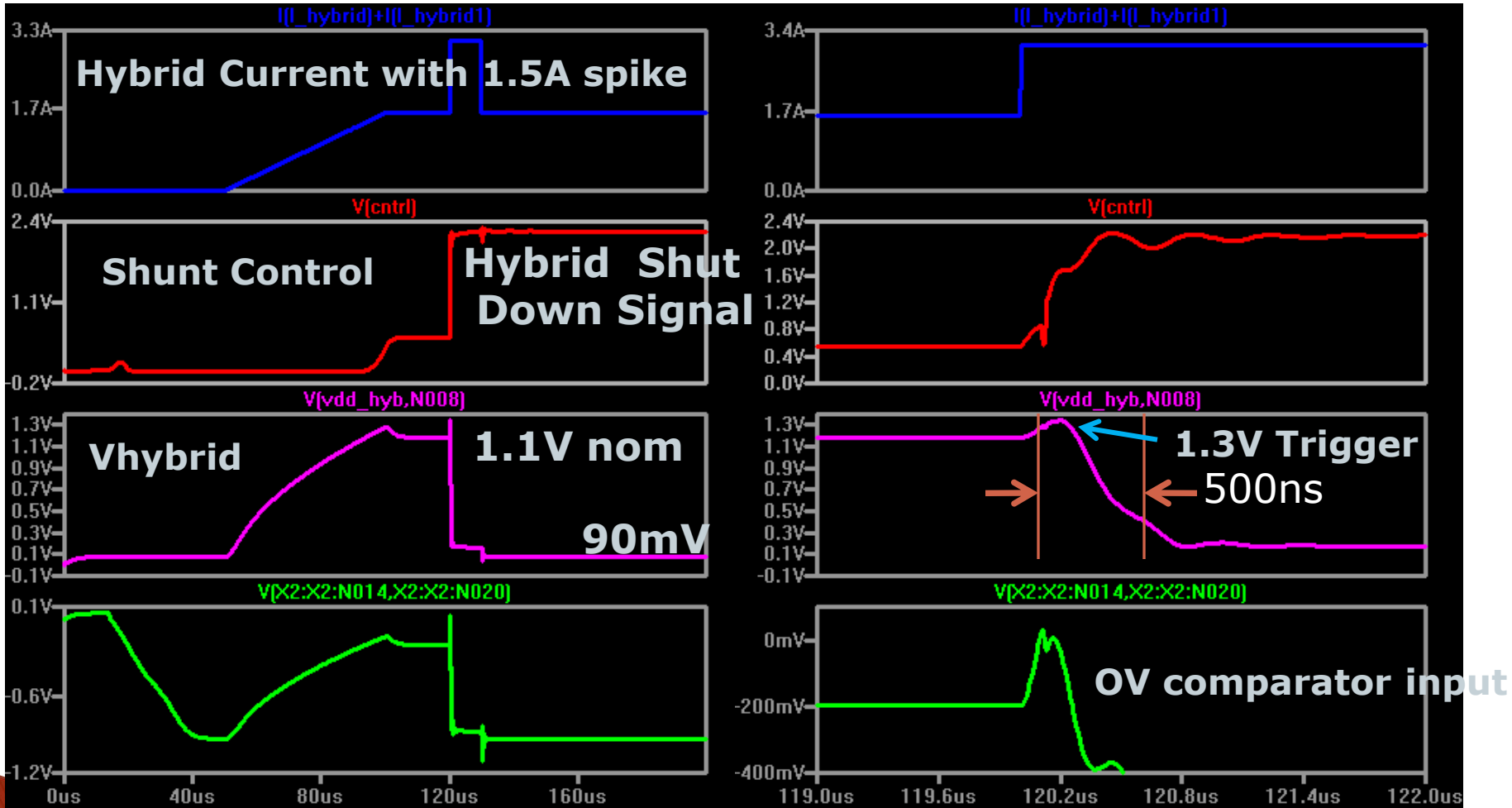
** "External FET gate" to accommodate Shutdown mode when used with ABCn

SPICE sims of shutdown

Fault condition → 1.5A spike

← 200μs →

← Zoom in 3μs →



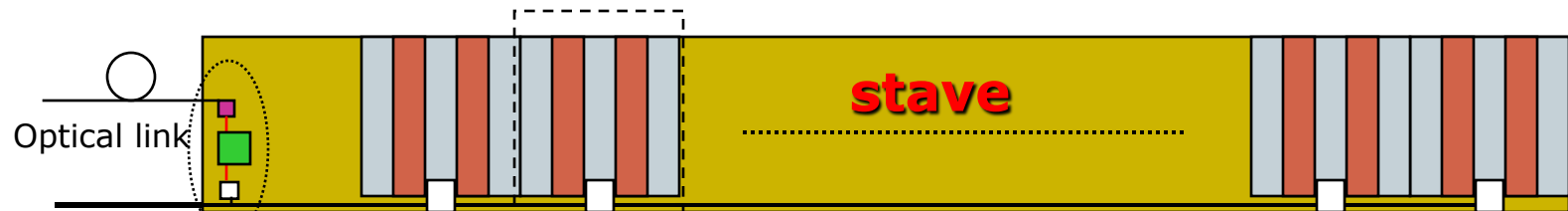
DC-DC converters

- ▶ Yale - Commercial Devices including some success with Rad Tolerant devices, Inductor Design
- ▶ CERN
 - RAD Hard custom ASIC Buck convertor
 - Switched Capacitor Convertors
 - EMI analysis and reduction
 - Miniaturized packages
- ▶ AACHEN Study of EMI emission implementation of CERN AMIS2 ASIC for CMS Pixel DCDC convertor.

DC – DC ATLAS SCT upgrade

Proposed distribution scheme based on 2 conversion stages

Example design shown for ATLAS short strip concept



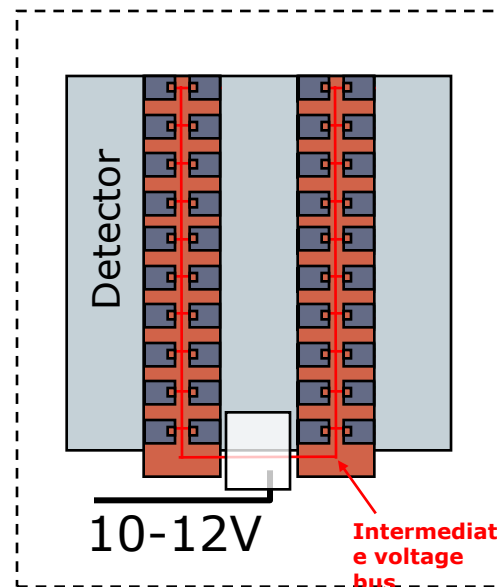
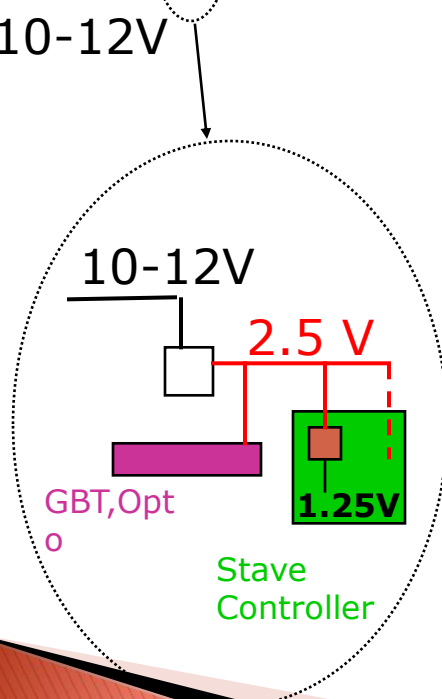
Building Blocks

Stage1:

- Inductor-based buck
- $V_{in} = 10-12\text{ V}$
- $V_{out} = 2.5-1.8\text{ V}$
- $P_{out} = 2-4\text{ W}$

Stage2:

- On-chip switched capacitor
- $V_{in} = 2.5-1.8\text{ V}$
- Conversion ratio $\frac{1}{2}$ or $\frac{2}{3}$
- $I_{out} = 20-100\text{ mA}$



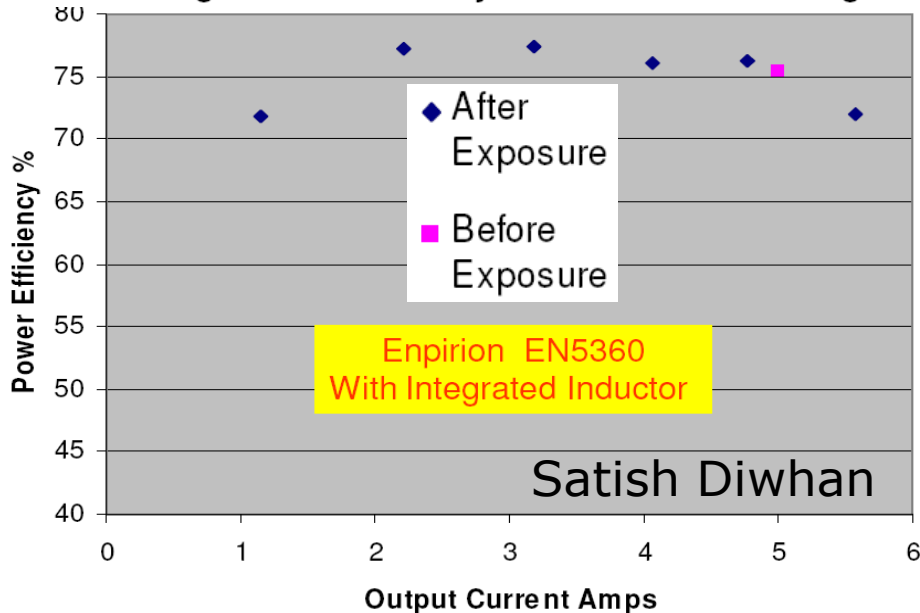
F.Faccio – CERN/PH/ESE

Same blocks can be combined differently to meet custom system requirements PWG meeting '10

DC - DC Stage 1

Commercial ASICs

Buck Regulator Efficiency after 100 Mrad dosage

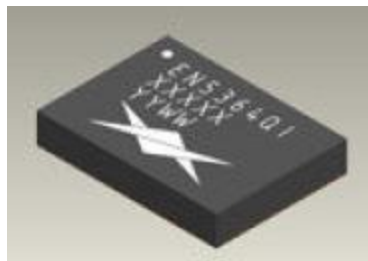


Enpirion EN5360
With Integrated Inductor

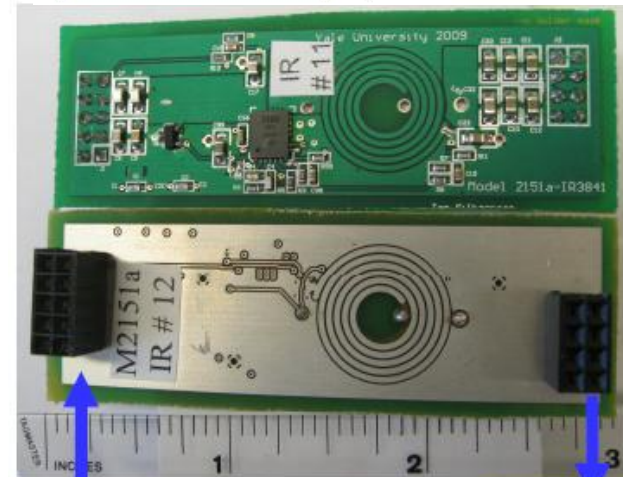
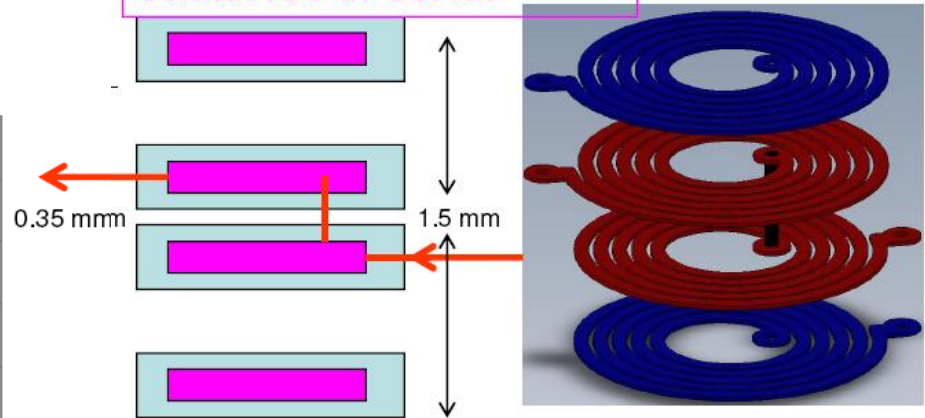
Satish Diwhan

reported @ TWEPP 2008 - IHP was foundry for EN5360

Enpirion OK Except for
Internal Inductor



Coupled Air Core Inductor
Connected in Series



Maxim
Buck
Converter
not
Rad Hard

12 V

2.5 V
@ 6 amps

Efficiency ~ 70% @ 4A

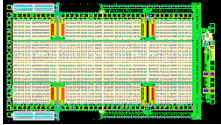
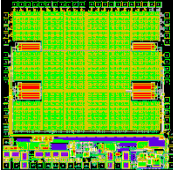
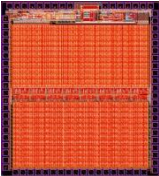


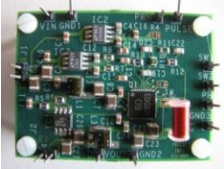
Design by Satish Diwhan, Yale

CERN WP2: On-detector power distribution

- ▶ ATLAS, CMS and “common” Working Groups on powering are an efficient communication and coordination tool
 - We contribute regularly to the meetings with large number of talks
- ▶ Direct collaboration with ATLAS and CMS
 - CMS tracker
 - Work in parallel on DCDC boards done in RWTH and CERN, with regular exchanges of results. We provide ASICs and our knowledge on board layout, converter functionality, filtering and shielding issues
 - Our results and contribution were fundamental to drive the choice of the CMS task force that selected DCDC option for powering their upgraded tracker
 - Our standardized test setup to measure conducted noise was cloned in other Institutes participating in CMS (we helped with information and documentation)
 - We will provide the IP block of the $\frac{1}{2}$ converter based on switched capacitors
 - ATLAS tracker
 - Characterization of prototype hybrids powered with DCDC converters is done in collaboration with Liverpool and Geneva Universities
 - We participate in the definition of the power distribution in the prototype supermodule developed at KEK and Geneva University. We collaborate with Liverpool University for integration of DCDC converters in the prototype stave developed in the UK-US
 - Design of an on-chip $\frac{1}{2}$ converter based on switched capacitors in collaboration with AGH Cracow
- ▶ Direct expressions of interest for the converter (other than silicon strip detectors for phase2)
 - CMS pixel detector for phase1 upgrade (PSI, RWTH, Fermilab)
 - CMS HCAL for phase1 upgrade (Minnesota, Fermilab,)
 - ATLAS TileCal (Argonne Nat. Labs)

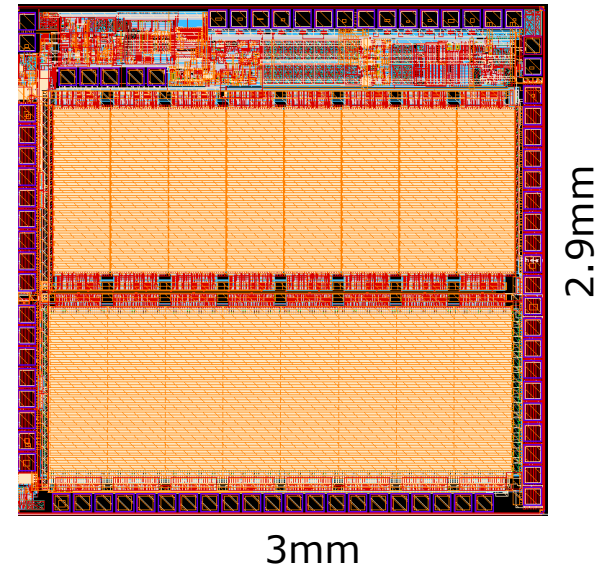
CERN Buck converter ASIC: prototypes fabbed to date

**Stage 1
DC-DC
Step down
going from
12-15V
down to
~2.5V**

Prototype	AMIS1	AMIS2	IHP1
ASIC			
Techno	On-semicond. 0.35	On-semicond. 0.35	IHP 0.25
Package	QFN48	QFN48 QFN32	QFN48 QFN32
PCB			
Vin	5V to 15V	5V-12V	5V to 12V
Vout	Programmable	Presets at 1.2/1.8/2.5/3/5V	Programmable
Iout	2A	3A	3A
Fsw	1 MHz	1 MHz	2.0 MHz
Efficiency	< 80%	82%	87%
Gate Delay	Fixed	Programmable	Adaptative
Comment	First Prototype. Required an external sawtooth generator and regulators.	Second Prototype. Programmable gate delay improves efficiency. Still requires external regulator. No protection features.	Third Prototype. Adaptative gate delay further improves efficiency. Requires external regulators and Vref. No protection features.

IHP2 prototype

- ▶ Second prototype in the IHP SGB25VGOD technology
- ▶ Design included in MPW run of Jan10
Expected back in May 2010
- ▶ Additional features integrated in the prototype:
 - Linear regulators
 - Bandgap
 - Overcurrent protection
 - Improvement in the adaptive logic
 - Triplication and logic against SEU
 - Enablers
 - Complete circuit
 - Over current protection
 - Dimension of the power transistors
- ▶ External components needed
 - Compensation network



Prototype for SCT Hybrid now

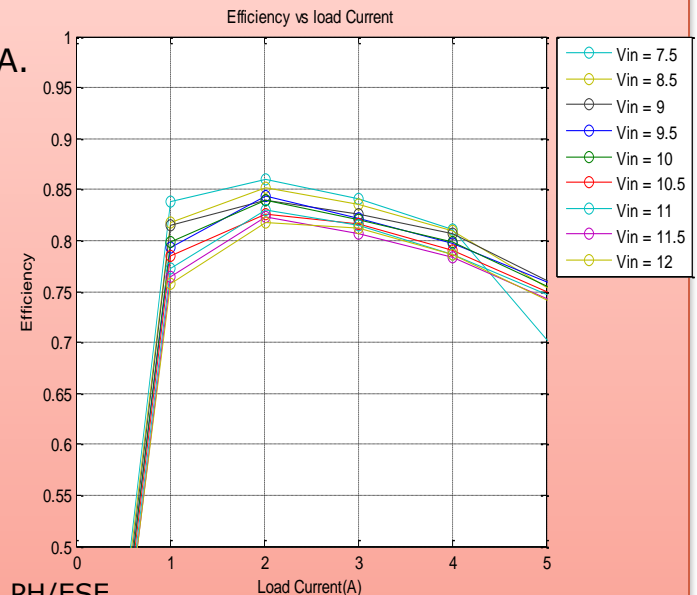
- The AMIS2-PIB can deliver 3.5A : insufficient for the ABCn hybrid.
- A compatible DCDC, with same geometry and connector has been designed using a commercially available controller.
- Results from first prototype:
 - Switches at 3 MHz, delivering 5A.
 - Can power one full hybrid.
 - Efficiency reaches 87% at 2A, and is around 80% at 4A.
 - Output stable up to 5A load.



ATLAS CMS PWG, March 2010

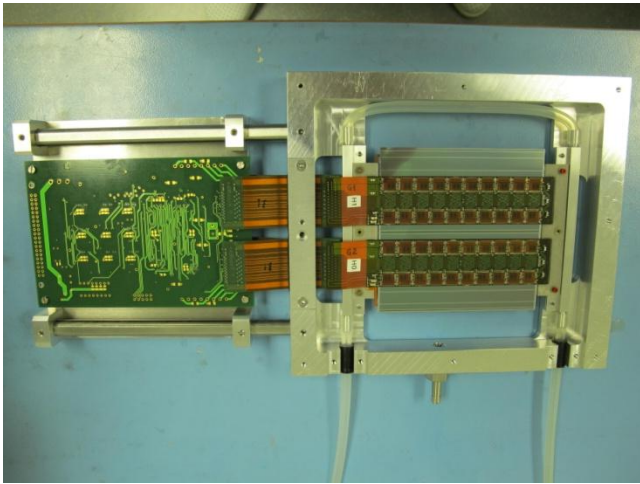


G. Blanchot, PH/ESE



UniGe Module

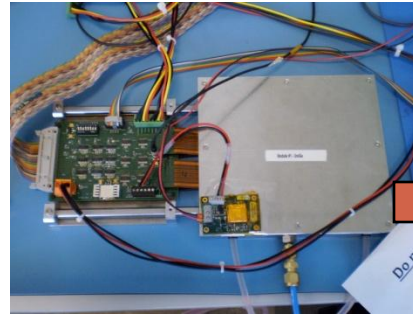
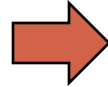
Position of hybrids



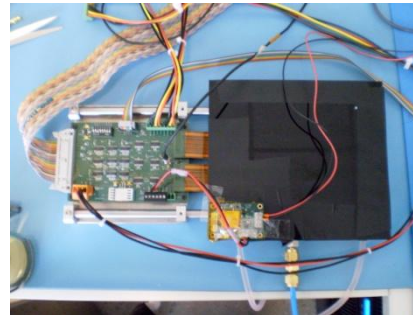
Measurements performed with the help of Sergio Gonzalez from University of Geneva.

DC - DC works on ABCn Prototype module!

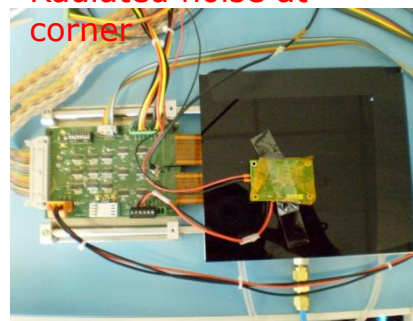
ATLAS CMS PWG, March 2010



Conducted noise test

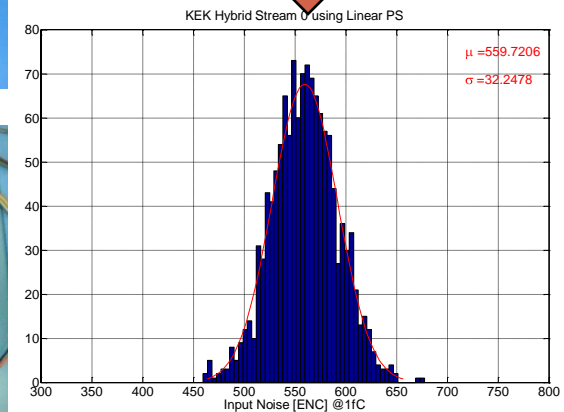
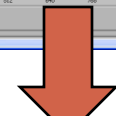
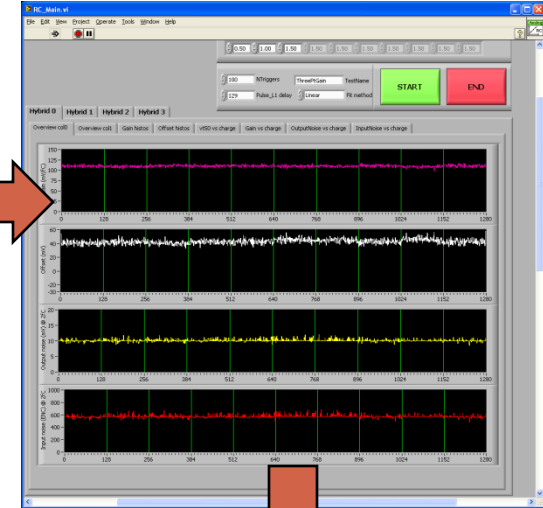


Radiated noise at corner



Radiated noise on top of hybrid

G. Blanchot, PH/ESE



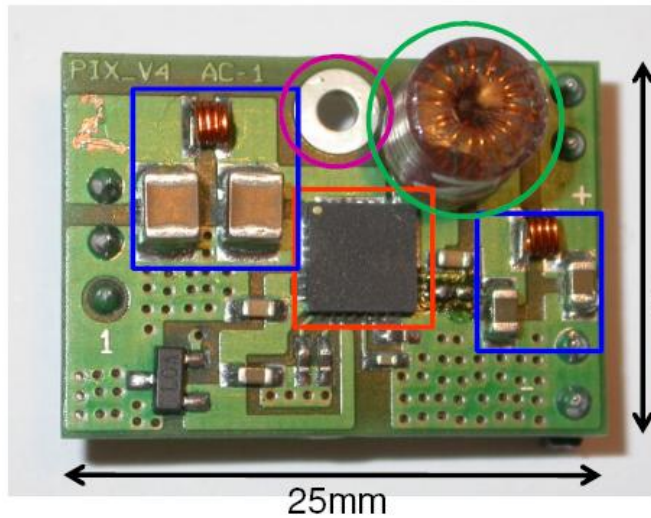
Reference noise:

ENC Average: 560

ENC Sigma: 32



Prototype: AC_PIX_V4 Buck Converter



$m = 2.7g$

18mm

25mm

PCB:

2 copper layers a $35\mu\text{m}$
FR4 1mm
A = 18mm x 25mm for QFN32

Chip: **AMIS2** by **CERN**

$V_{\text{IN}} < 12\text{V}$
 $I_{\text{OUT}} < 3\text{A}$
 $V_{\text{OUT}} = 3.3\text{V}$
 $f_s \approx 1.3\text{MHz}$

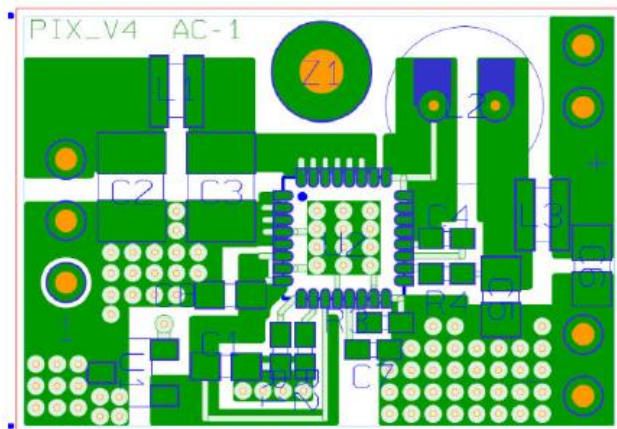
Air-core toroid:

Custom-made toroid, $\varnothing \approx 6\text{mm}$,
height = 7mm, $L = 600\text{nH}$, $R_{\text{DC}} = 80\text{m}\Omega$

Input and output π -filters

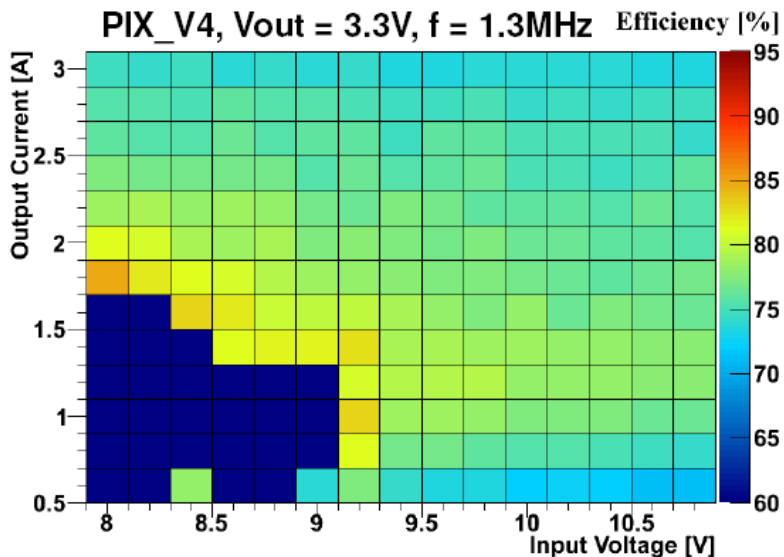
$L = 12.1\text{nH}$, $C = 22\mu\text{F}$

Cooling contact

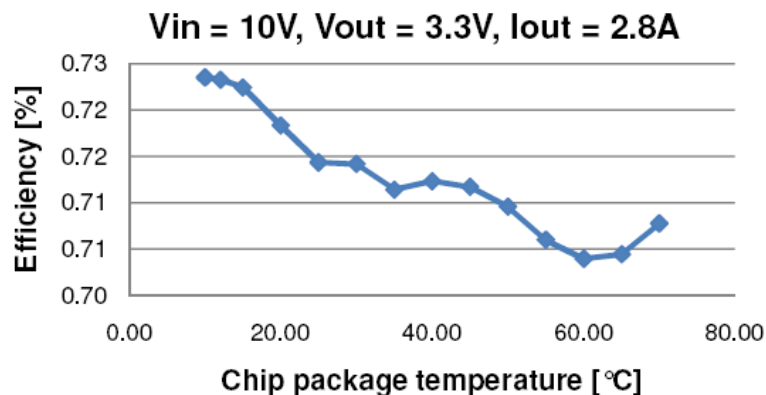
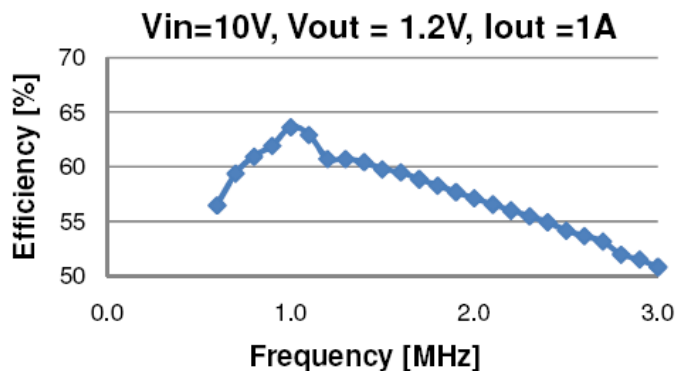




AC_PIX_V4 Efficiency



- ~ 75% for 3A and conv. ratio of 2-3
- Res. losses (R_{on} , wire bonds, coil) $\sim 1/f_s$; switching & driving losses $\sim f_s$
- Further improvements are expected:
 - Move from 1.3MHz to 1.0MHz
 - Gain few % with cooling
 - Move to flip-chip package
 - On-chip routing?
 - PCB layout, capacitors etc.?



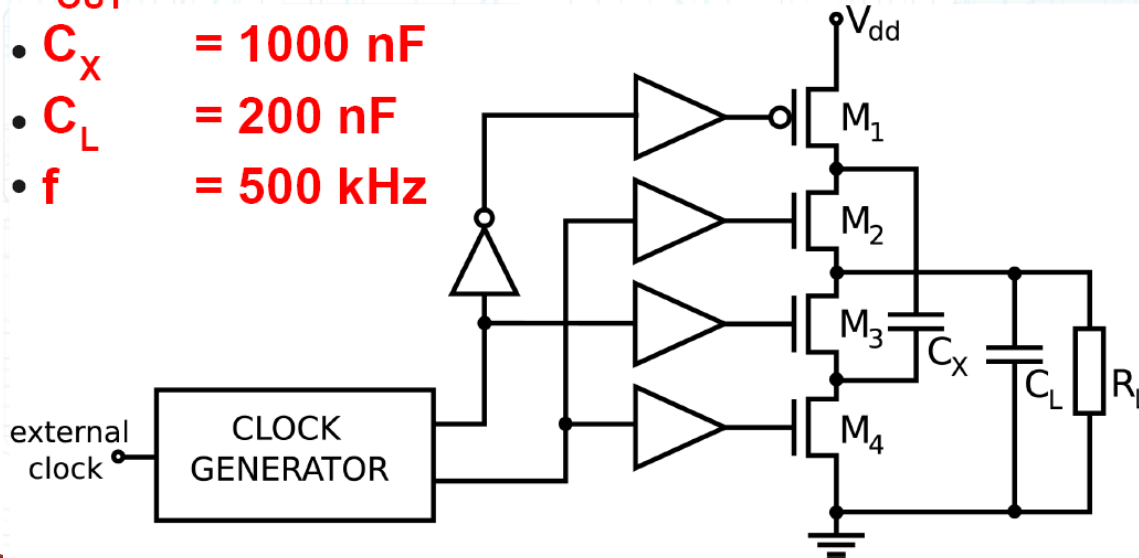
DC – DC (stage 2)

CERN submission in 130nm CMOS June 2010
Primary Designer Michal Bochenek

Practical solution for the DC-DC step-down converter

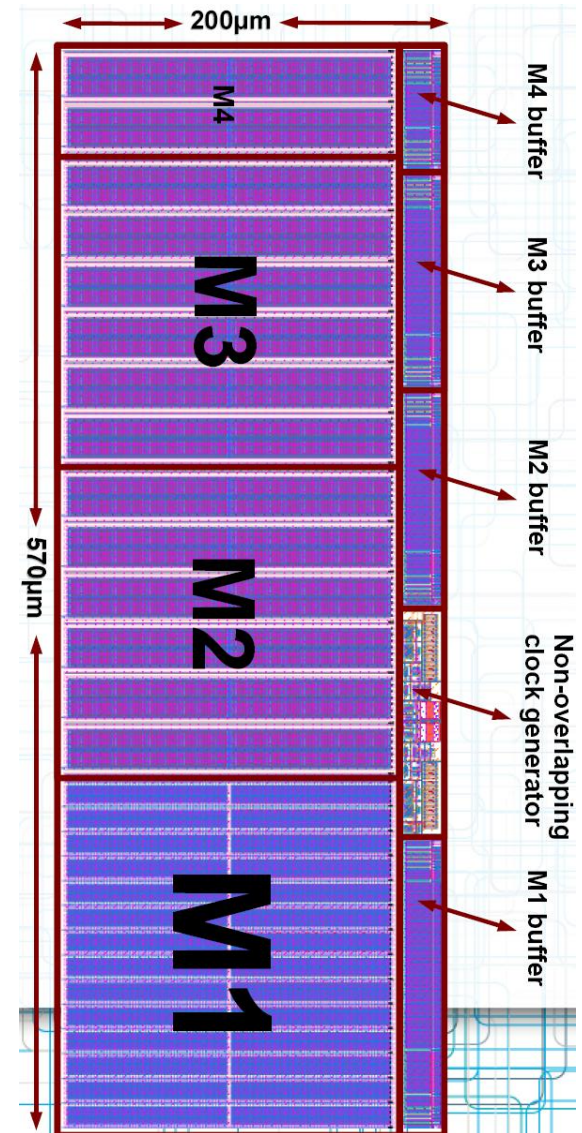
- $V_{DD} = 1.9 \text{ V}$
- $V_{OUT} = 926 \text{ mV}$
- $I_{OUT} = 60 \text{ mA}$
- $C_X = 1000 \text{ nF}$
- $C_L = 200 \text{ nF}$
- $f = 500 \text{ kHz}$

Power efficiency = 97%



ATLAS-CMS Power Working Group

31 March 2010



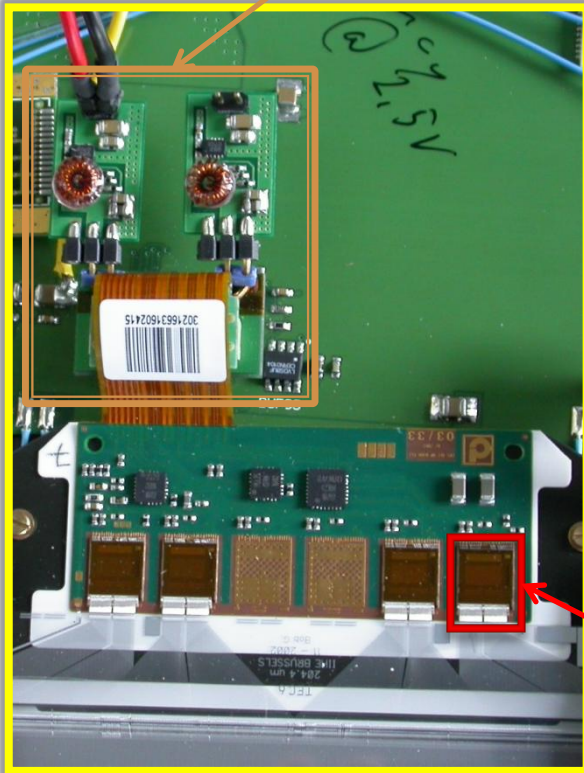
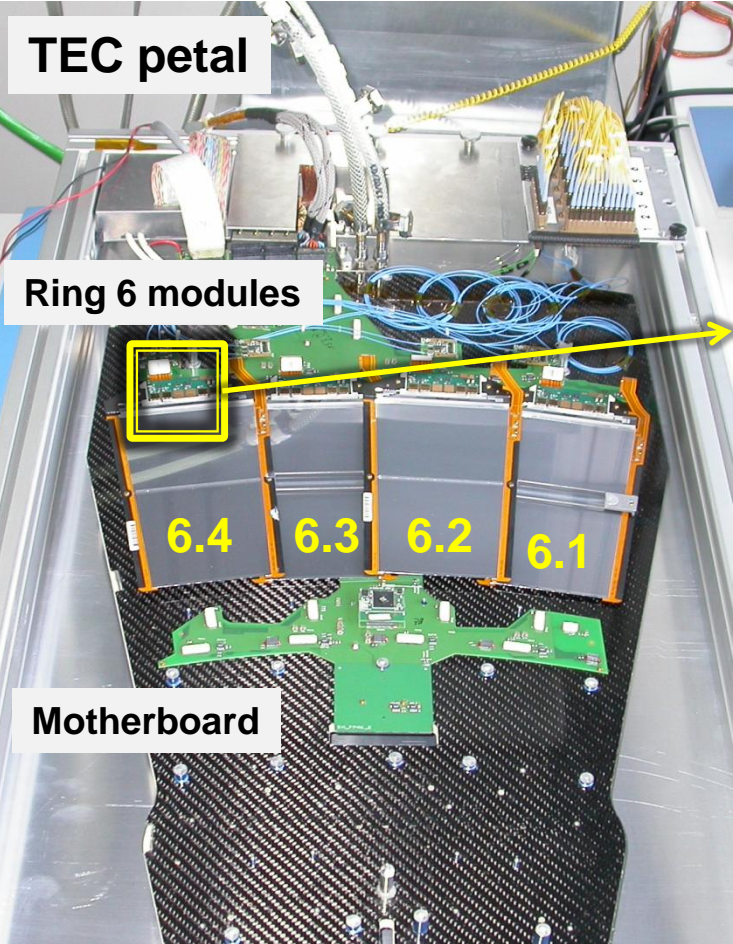
DC – DC Advantages

- ▶ Highly Developed by Commercial Vendors
- ▶ No requirement for constant current draw.
- ▶ Conventional DC data/control communications.

Development Initiatives

- ▶ CERN WP2 priority development
- ▶ Several groups pursuit of low mass, low EMI inductor designs.

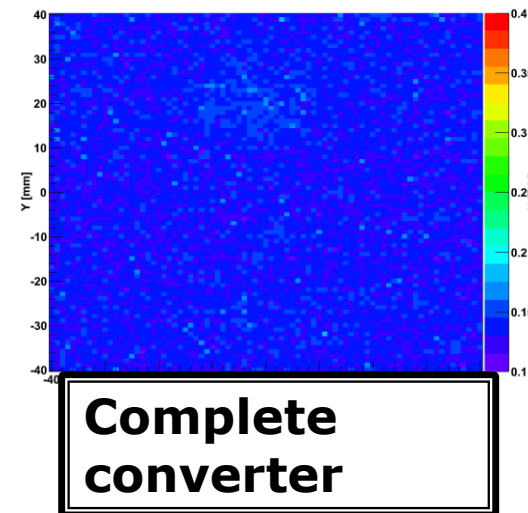
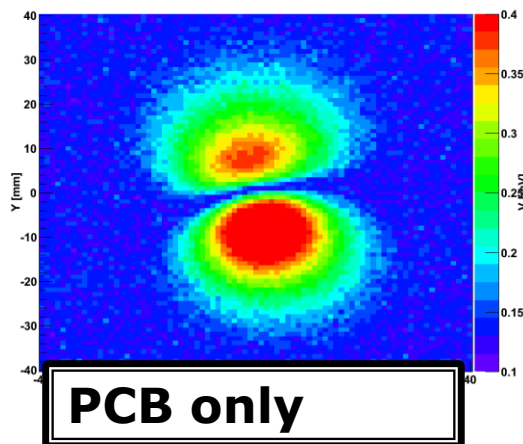
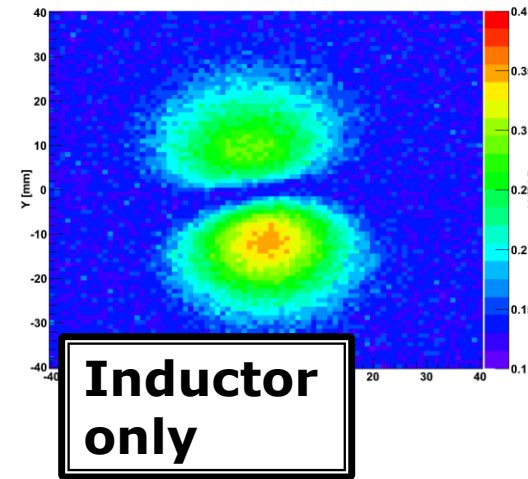
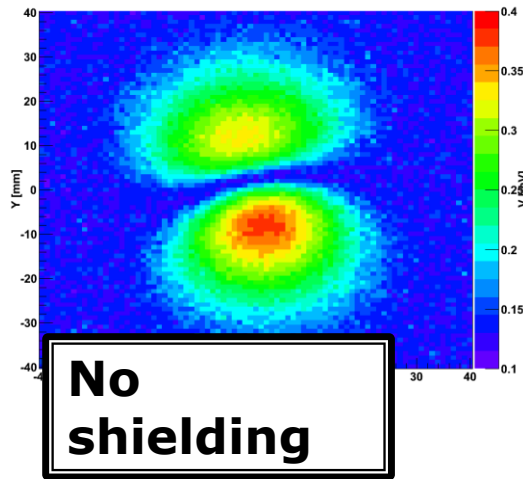
- Two DC-DC converters per module
- Integrated via additional adapter
- V_{in} from lab power supply



APV25 readout chip:

- 0.25 μm CMOS
- 128 channels
- **analogue readout**
- per channel: pre-amp., CR-RC shaper, pipeline
- $\tau = 50\text{ns}$
- 1.25V & 2.50V supply
- $I_{250} = 0.12\text{A}$, $I_{125} = 0.06\text{A}$

B_z -Field of AMIS2-V1, $V_{in}=8.5V$, $V_{out}=2.5V$, $f=1.3MHz$, $L=600nH$



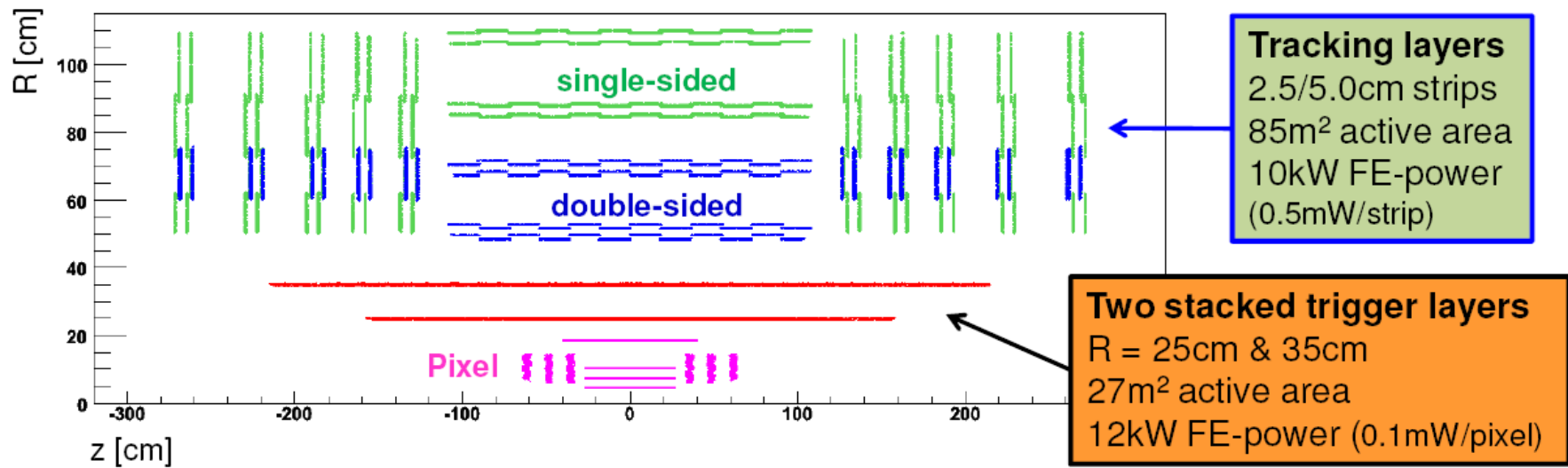
- Shielding only the inductor is not sufficient
- B-field not measurable when converter is completely encased



Outer Tracker Upgrade



- Some proposals combine a minimalistic trigger configuration with a “classical” outer strip tracker
- Successor of APV25, the **CMS Binary Chip (CBC)**, foreseen as readout ASIC (under development)
- 1 CBC (128 channels) needs $P = 64\text{mW}$ (for 1.2V supply voltage)

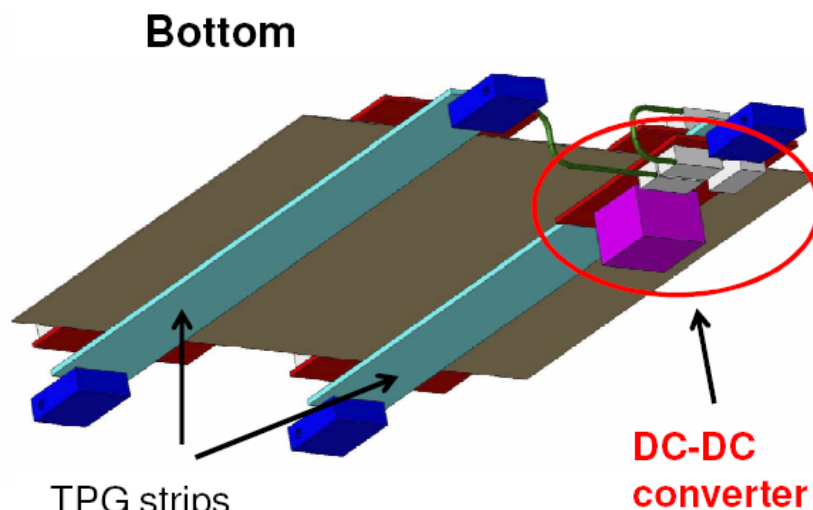
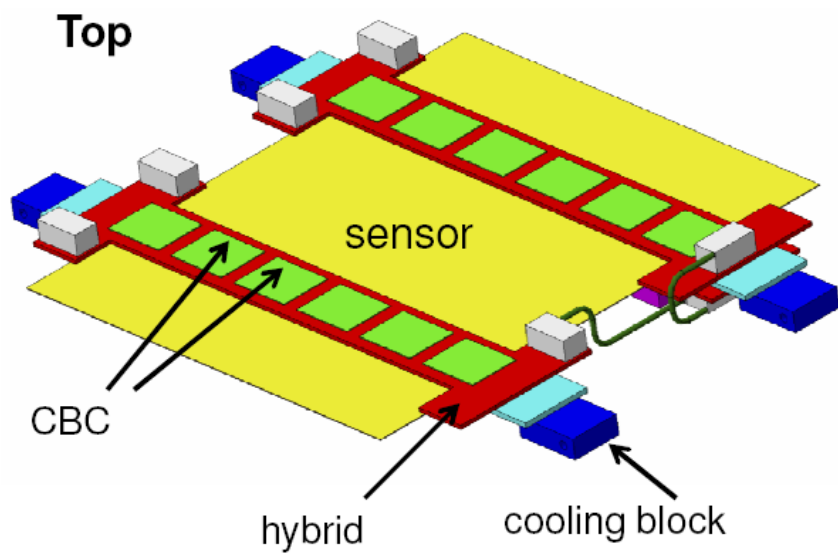
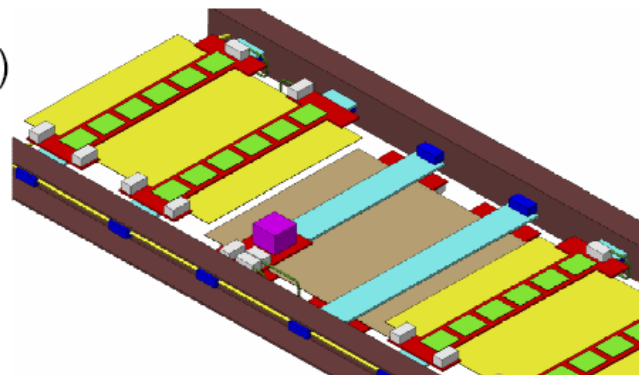




DC-DC Converters for Outer Tracker



- Power requirements: only 1.5W per module
- Idea: use 1.2V buck converter (requ. conv. ratio ~ 4) plus maybe on-chip charge pump (currents are low)
- Space is again tight – various ideas:
 - move into 3rd dimension
 - integrate into support structure
- Tests have to wait for CBC and module prototypes



Conclusions

Two Powering Approaches appear to be working both are projected to have similar efficiency

Serial Power -

Basic Pros - Lower Material, DC operation

Basic Cons - Modularity inconveniences
AC coupling

DC-DC -

Basic Pros - no modularity constraints,
conventional DC signaling.

Basic Cons - Two elements in current path
Technically challenging for remote high
rad environment.

Lots of excellent work in progress.