ALICE Silicon Pixel Detector operations and performance

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Summary

- Role of SPD
- Structure of the detector
- Description and operation of the cooling system
- Implementation of FastOR trigger
- General optimization
- Performance
- Conclusions
The Silicon Pixel Detector makes the 2 innermost layers of ALICE, providing:

- **impact parameter resolution**
  - makes the performance in the transverse plane
  - wide heavy-flavours based physics programme

- **vertexing capability**
  - secondary micro-vertexes
  - primary vertex

- **trigger**
  - fast detector
  - L0 trigger logic via FastOR: unique feature at LHC

- **charged particles pseudorapidity distribution**
The SPD in ALICE

- ALICE: 18 subsystems for a versatile detector!

<table>
<thead>
<tr>
<th>Layer</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radius cm</td>
<td>3.9</td>
<td>7.6</td>
</tr>
<tr>
<td>Length cm</td>
<td>28.2</td>
<td>28.2</td>
</tr>
<tr>
<td>Power W</td>
<td>&lt; 1500</td>
<td></td>
</tr>
<tr>
<td>Thickness $\chi_0$</td>
<td>2.28</td>
<td></td>
</tr>
<tr>
<td>Occupancy $% (dN/dy=6000)$</td>
<td>2.1</td>
<td>0.6</td>
</tr>
</tbody>
</table>
SPD structure

- SPD
  - 2 half-barrels

- Half-barrel
  - 5 sectors

- Sector
  - 12 half-staves
    - 1 multilayer bus
    - 1 MCM
    - 2 bump bonded ladders
    - 5 read-out chip
    - 1 sensor

Total of 120 half-staves
1200 chips
9.8 M channels
half-stave= smallest working element

R=3.9 & 7.6 cm
The half stave

- p⁺-n-type silicon sensor
- 200 µm thick
- cell size: 50 (rφ) × 425 (z) µm²
- 5 readout chips 150 µm thick
- 40960 bump bonds

- Mixed signal ASIC
- Produced in a commercial 0.25 µm CMOS process (8” wafers)
- Radiation tolerant design (enclosed gates, guard rings)
- 8192 pixel cells
- ~100 µW/channel
- ~3000 e⁻ mean threshold (~200 e⁻ RMS)
- ~120 e⁻ mean noise

[Diagram of the half stave setup with labels for pixel detector, readout chip, cooling tube, and SMD component.]
SPD DCS:

- SCADA system based on PVSS

- PVSS: link hardware – Finite State Machine (FSM)

- FED: Front End Driver, off-detector electronics / PVSS interface

4 PVSS projects running on 4 computers

PS control

Interlocks

Cooling

FED

Graphical UI
Cooling system: scheme

- **2-phase system**
  - Joule-Thomson cycle: sudden expansion + evaporation @ const. enthalpy

- **Fluid:** $\text{C}_4\text{F}_{10}$ dielectric, chemically stable, non-toxic
  - typical conditions: $p=1.92 \text{ bar}$, $T=15 \degree \text{C}$

- Tested up to $2.5 \times$ nominal power (SPD full power = 1.5 kW)

- **Controls:**
  - liquid pressure $\equiv$ flow
  - gas pressure $\equiv$ temperature
Evolution of efficiency

- Status before installation
  - 120 ON ≡ 100%

- Status in October 2008
  - 103 ON ≡ 86%

  ◆ Modification of services

- Status in August 2009
  - 85 ON ≡ 71%

  ◆ Counter-flow flushing of lines

- Status in October 2009
  - 101 ON ≡ 84%

  ◆ Installation of subcooling

- Status in November 2009
  - 110 ON ≡ 92%

  ◆ Best performance ever

  ◆ For stability sake, keep ~100 ON
Analysis performed on a one-year old filter.

Results and conclusions: “In the used filters several exogenous fragments were located clogging the filter. There were several fragments containing different composition elements. In addition to elements from the Stainless steel, the following traces of elements were found: O, Al, K, C, Sn, Cu, P, Ca, Cu, Na, Cl and Zn.”
Cooling: actions & conclusions

- New input lines installed
  - Path more straight and short
- Subcooling close to the detector
  - Lower temperature to cure possible bubbling
- Counter-flow flushing (w/ C₆F₁₄)
  - Remove bits and pieces that could have moved from the plant to the filters

- The main problem seems to be the clogging of filters (no access until long stop)
- There is a dependence of the running conditions on the way the system is started
  - maybe correlated to the previous issue

- Impact on tracking not negligible: efficiency reduced by 15% if single SPD-point required and ~40% if 2 points required
- The lack of flow has been partially cured. The big leap will hopefully happen when we’ll have access
- In the meantime, even if not at 100% efficiency, it works …
Current performance

- ON=97 (81%)  \( \langle T \rangle = 29^\circ C \)  \( \langle P \rangle = 9.8 \text{ W/hs} \)
  - a few kept off for stability (suffered of contingent heat-up)
FastOR trigger

- Each of the 1200 chips can issue a signal if a hit is present (every 100 ns)

- Possible AND/OR combinations of FastOR (10 of them implemented in the current FPGA release) with programmable thresholds
  
  \[ \text{e.g. min. bias} \equiv N_{(I+O)} \geq \text{th}_{I/O} \text{ AND } N_I \geq \text{th}_I \text{ AND } N_O \geq \text{th}_O \]
  
  \[ \text{cosmic} \equiv (\text{upper half}) \text{ AND } (\text{lower half}) \]
  
  \[ \text{centrality} \equiv N_I \geq \text{th}_I \text{ AND } N_O \geq \text{th}_O \text{ (for PbPb)} \]

- Read-out @ 10 MHz, included in the datastream

- Unique feature at LHC!
**FO trigger treatment**

- PiT (Pixel Trigger) designed to process FastOR and deliver a trigger signal to Central Trigger Processor at Level 0
- Latency min-max: 735 - 845 ± 17.5 ns
- Deserialization and FO extraction:
  - optical receivers + FPGA on 10 OPTIN boards (one for 12 SPD modules)
  - processing in large FPGA (9U BRAIN board) with up to 10 algorithms at the same time (in 25 ns!)

![Diagram of FO trigger treatment process](image)
Aligning clock phases

Alignment of the internal phases of the SPD clock at 10 MHz

Relative phases of 120 clocks of control units: $\sigma = 0.63$ ns
Propagation delays due to 120 optical fibers: $\sigma = 0.90$ ns

Clock phases at SPD inputs without correction: $\sigma = 1.10$ ns

✔ Individual delays added to the clock transmitters to compensate differences

Clock phases at SPD inputs with correction: $\sigma = 0.08$ ns
FastOR tuning

- Needed for max efficiency and min noise on each of the 1200 chips
- Makes use of internal pulser:
  - every single pixel can be addressed
  - pulse is sent to: none, one or more pixels (within 12%, i.e. maximum occupancy) to check noise and efficiency in all conditions
- Tuning possible by 4 (out of 42) 8-bit DAC in each chip + global chip threshold
- Automatic procedure can go in parallel on all 1200 chips, time required (with optimization) ~4 h (manual procedure: 10×)

![Graph showing FO counts, Efficiency, Noise, convpol, fopol]
Trigger efficiency

- From lab tests 100% efficiency expected
- Slightly lower observed during run
  - 4 bunches running, 2 bunch crossings (BC) in ALICE
- Look for a hit and check presence of FO from the corresponding chip
- Do it in different BC modes: BCmod4 = 0,1,2,3

SPD 10MHz clock phase relations with 40MHz LHC clock: BCmod4 = 0,1,2,3

- 4x4b $\rightarrow$ BCmod4 = 0 and 3
- 4x4c $\rightarrow$ BCmod4 = 1 and 3
- 2x2a $\rightarrow$ BCmod4 = 2
From the lab to ‘real life’:

- Three main parameters to tune:
  - thresholds
  - charge-preamplifier current
  - reference I-V

- Power consumption
  - Reduced by cutting charge-preamplifier current: efficiency is conserved, a couple of “compromises” at low current
Optimization - 2

- uniformity
  - maps obtained by internal pulser & bump-bonding tested with tracks
  - noisy: < $10^{-4}$
  - dead: 1.2% (in working chips)
  - was $10^4$ (on $10^7$ total channels) in the lab (tests with Sr$^{90}$ source)

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92.6 $\leftarrow \varepsilon \rightarrow$ 98.6
threshold

- use internal pulser (variable amplitude) to determine threshold on single pixel – 3000 e⁻ average

After
67% with prevth=200

Before
48% with prevth=190
Data taking @ 7 TeV

- ~5\times10^6 events recorded to date
- ~2.4 nb\(^{-1}\) integrated luminosity
- MB trigger using SPD FO capability

**Integrated triggers**

- Total recorded events
- Total CINT1B triggers
- Total CMUS1B triggers (x30)

**Recorded Integrated Luminosity**

- Only 7TeV data
- \(\sigma = 72 \text{ mb}\)
- Minimum bias (CINT1B)
Resolution on primary vertex

- Impact parameter resolution
  - track refit in ITS w/vertex
  - 2 points required in SPD
  - with and without beam constraint
  - track analysed excluded by vertex finding

- Vertex spread
  - 7 TeV data
  - SPD tracklets compared to full tracking: faster, no need for reconstruction
  - Tracking includes SPD points

More details in the talk of Andrea Rossi on …
First event...

- At 900 GeV...

- ...and 7 TeV
First LHC paper shows pseudorapidity density at 900 GeV, based on SPD data
Data from SPD also key of the next 2 papers, presenting data from 0.9, 2.36 and 7 TeV
...and many more to come
Conclusions

- The Silicon Pixel Detector is designed to deliver outstanding vertexing performance in ALICE.

- It has the feature, unique among LHC vertex detectors, to deliver the L0 trigger.

- The commissioning of the detector has gone through the main stages of FastOR calibration, timing, thresholds tuning, power optimization. Analysis of dead/noisy pixels still ongoing.

- Cooling is performing worse than expected, while we’re keeping efficiency above 85%. Intervention is foreseen for the long shutdown to improve the performance.

- The detector has a key role in the physics reach of ALICE and has successfully started showing it!

My personal thanks (for pictures, comments, etc.) to:
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R. Ferretti, V. Manzari, R. Santoro.
Detector configuration 2010

- ITS, TPC, TOF, HMPID, MUON, V0, T0, FMD, PMD, ZDC (100%)
- TRD (7/18)
- EMCAL (4/12)
- PHOS (3/5)
- HLT (60%)

Full hadron and muon capabilities
Partial electron and photon
No change with respect to 2009 run
Tracking

- robust, redundant tracking from 100 MeV to 100 GeV
  - modest soleniodal field (0.5 T) => easy pattern recognition
  - long lever arm => good momentum resolution
    (BL² : Alice ~ CMS > Atlas !)
  - small material budget: ~ 10% X₀ vertex -> end of TPC (r = 2.6 m)

- full GEANT simulation: central Pb-Pb, dN_ch/dy = 6000
  - very little dependence on dN_ch/dy up to 8000 (important for systematics !)

Momentum resolution ~ 5% @ 100 GeV

Impact parameter < 50 μm for p_t > 1.5 GeV
Installation in ALICE experiment

Optical splitters

Clk Serial

C side

203.3 ± 1.7 ns
(41.5 ± 0.36 m)

Data

A side

214.25 ± 1.5 ns
(43.7 ± 0.31 m)

Switch Board

PIT main outputs

30 ± 5 ns

Central Trigger Processor

L0 in

LTU

TTC

680.2 ns

TTC

70.1 ns

C.R.

60
Tracking efficiency

pp 7 TeV, pass1 reconstruction

ALICE work in progress

20/05/2010

 ITS prolongation efficiency

- at least 2 ITS hits (Data)
- at least 1 SPD hit (Data)
- at least 2 ITS hits (MC)
- at least 1 SPD hit (MC)
Cooling controls

![Diagram showing cooling controls with various temperature and flow readings.]

- **Temp Side C**: Various values ranging from 9.30 to 12.54
- **Temp Side A**: Various values ranging from 11.54 to 19.97
- **Heaters**: Various temperatures ranging from 97.04 to 106.06
- **Press Side C**: Various values ranging from 3.43 to 4.34
- **Press Side A**: Various values ranging from 1.76 to 1.74
- **Flow**: Various values ranging from 2.22 to 1.16
- **Loop ON/OFF**: Several loops are indicated with green circles.