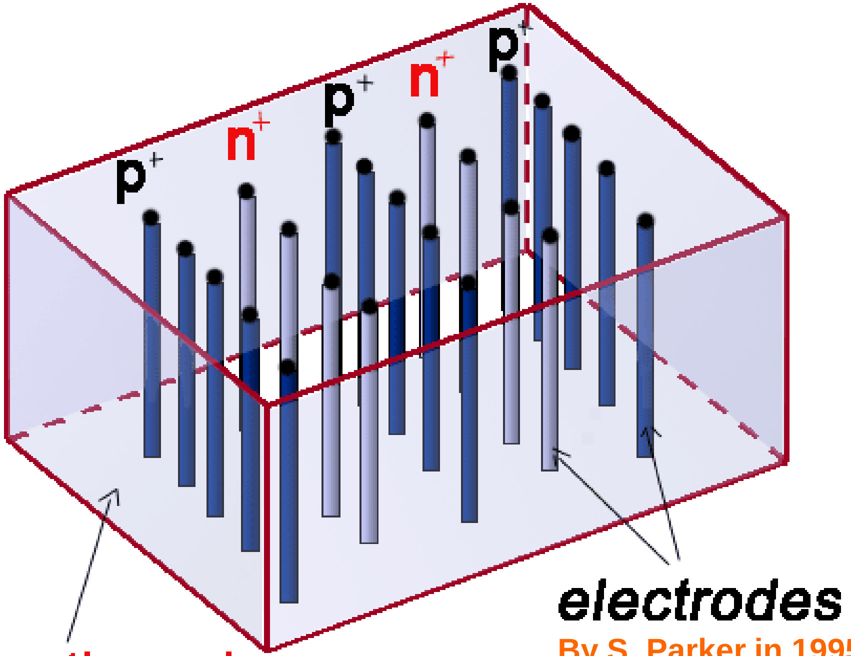
Fabrication of 3D Silicon Detectors



By S. Parker in 1995

n+-active edge

By C. Kenney in 1997

3DC

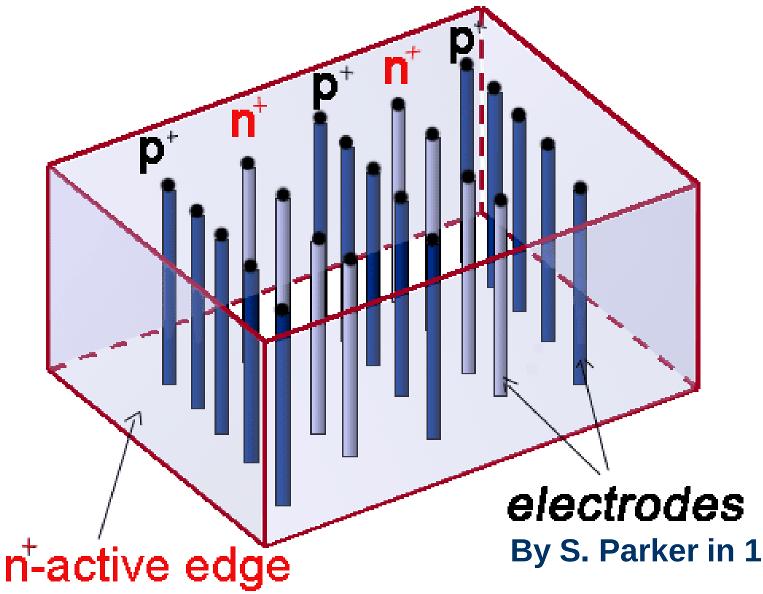
Angela Kok

SINTEF - Oslo, Norway

Fabrication of 3D Silicon Detectors

- Introduction
- Collaboration members
- Deep Reactive Ion Etching (DRIE)
- Wafer bonding
- Double sided processing by FBK and CNM
- SINTEF/ Stanford process
- Fabrication issues at SINTEF/ Stanford
- Improvements in the second SINTEF/ Stanford run
- Yield and test results – SINTEF/ Stanford
  - Wafer level
  - Post bump bonding
  - ATLAS
  - CMS
  - Preliminary beam test results
- Current fabrication status and future plans

3D - Introduction



By S. Parker in 1995

By C. Kenney in 1997

1. NIMA 395 (1997) 328
2. IEEE Trans Nucl Sci 464 (1999) 1224
3. IEEE Trans Nucl Sci 482 (2001) 189
4. IEEE Trans Nucl Sci 485 (2001) 1629
5. IEEE Trans Nucl Sci 48 6 (2001) 2405
6. CERN Courier, Vol 43, Jan 2003, pp 23-26
7. NIM A 509 (2003) 86-91
8. NIM A 524 (2004) 236-244
9. NIM A 549 (2006) 127
10. NIM A 560 (2006) 272
11. IEEE TNS 53 (2006) 1676
12. NIM A 587 (2008) 243-249

3D silicon detectors

- by S. Parker in 1995

Combination of traditional **VLSI** processing and **MEMS** (Micro Electro Mechanical Systems) technology

Electrodes are processed inside the detector bulk instead of being implanted on the wafer's surface.

Active edges

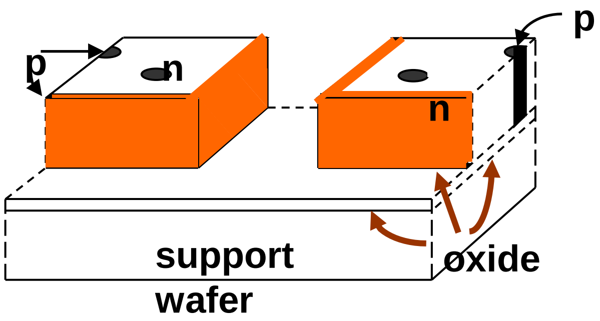
- by C. Kenney in 1997

The edge is an electrode!

Dead volume at the Edge < 2 microns! Essential for

-Large area coverage

-Forward physics



ATLAS 3D SILICON SENSORS R&D COLLABORATION

B. Stugu, H. Sandaker, K. Helle, (Bergen University), M. Barbero, F. Hügging, M. Karagounis, V. Kostyukhin, H. Krüger, J-W Tsung, N. Wermes (Bonn University), M. Capua; S. Fazio, A. Mastroberardino; G. Susinno (Calabria University), B. Di Girolamo; D. Dobos, A. La Rosa, H. Pernegger, S. Roe (CERN), T. Slavicek, S. Pospisil (Czech Technical University), K. Jakobs, M. Köhler, U. Parzefall (Freiburg University), N. Darbo, G. Gariano, C. Gemme, A. Rovani, E. Ruscino (University and INFN of Genova), C. Butter, R. Bates, V. Oshea (Glasgow University), S. Parker (The University of Hawaii), M. Cavalli-Sforza, S. Grinstein, I. Korokolov, C. Pradilla (IFAE Barcelona), K. Einsweiler, M. Garcia-Sciveres (Lawrence Berkeley National Laboratory), M. Borri, C. Da Vià, J. Freestone, S. Kolya, C. Li, C. Nellist, J. Pater, R. Thompson, S.J. Watts (The University of Manchester), M. Hoeferkamp, S. Seidel (The University of New Mexico), E. Bolle, H. Gjersdal, K-N Sjoebaek, S. Stapnes, O. Rohne, (Oslo University) D. Su, C. Young, P. Hansson, P. Grenier, J. Hasi, C. Kenney, M. Kocian, P. Jackson, D. Silverstein (SLAC), H. Davetak, B. DeWilde, D. Tsybychev (Stony Brook University). G-F Dalla Betta, P. Gabos, M. Povoli (University and INFN of Trento) , M. Cobal, M-P Giordani, Luca Selmi, Andrea Cristofoli, David Esseni, Andrea Micelli, Pierpaolo Palestri (University of Udine)

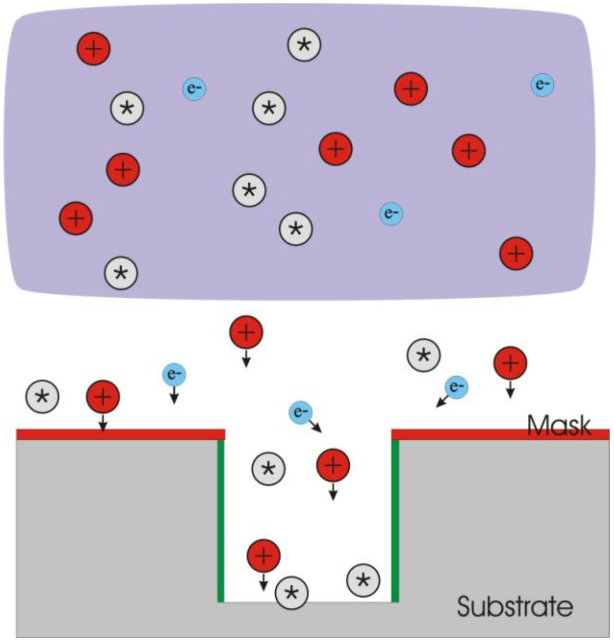
Processing Facilities: C. Fleta, M. Lozano G. Pellegrini, (CNM Barcelona, Spain); (M. Boscardin, A. Bagolini, P. Conci, C. Piemonte, S. Ronchin, N. Zorzi (FBK-Trento, Italy) , (T-E. Hansen, T. Hansen, A. Kok, N. Lietaer (SINTEF Norway), J. Hasi, C. Kenney (Stanford). J. Kalliopuska, A. Oja (VTT , Finland)*

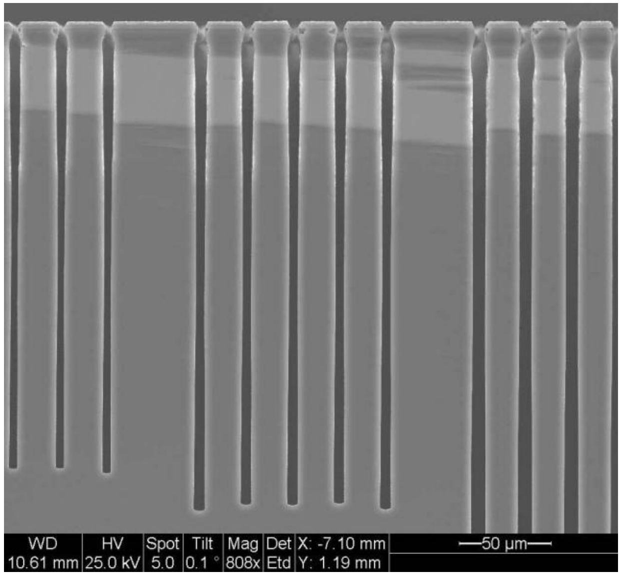
18 institutions and 5 processing facilities

3DC

Czech Technical University, Fermilab, Purdue University, SINTEF, SLAC, University of Hawaii, University of Manchester

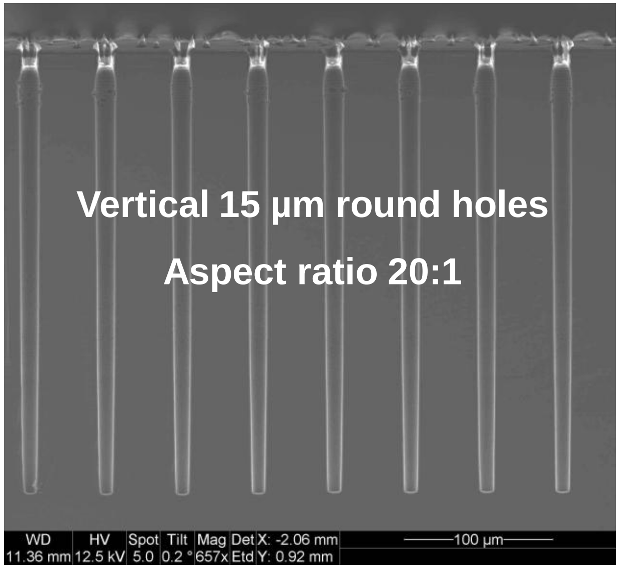
Deep Reactive Ion Etching





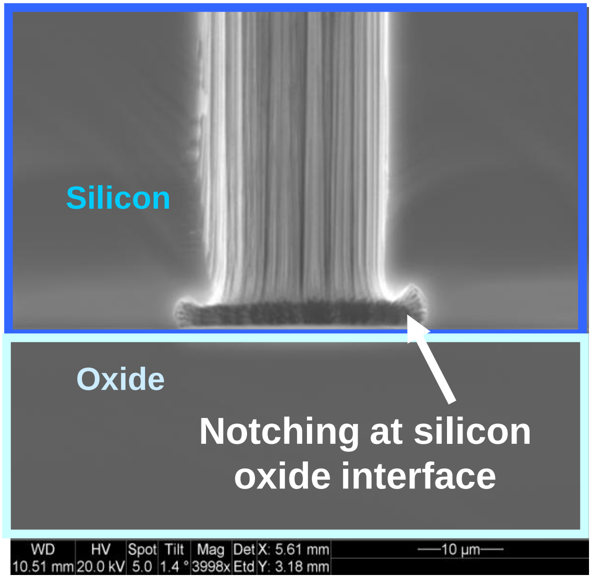
- Alcatel AMS-200
  - Key technology for 3D silicon
  - Vertical sidewalls passivated by polymer(C_4F_8)
  - Radicals etch exposed substrate (SF_6)
  - Aluminium has excellent selectivity
  - Aspect ratio up to 50:1 (depending on size of openings)

Deep Reactive Ion Etching

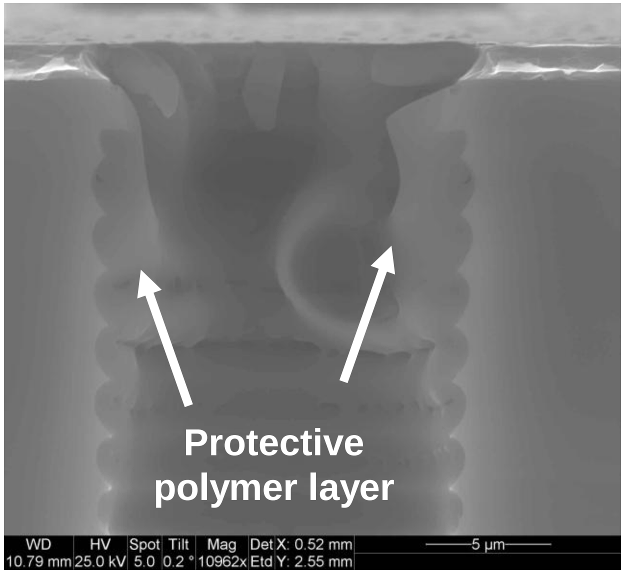


Vertical 15 µm round holes

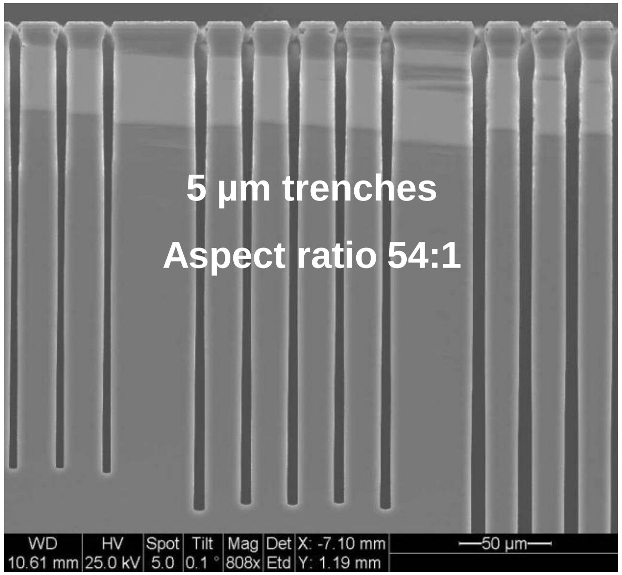
Aspect ratio 20:1



Notching at silicon oxide interface

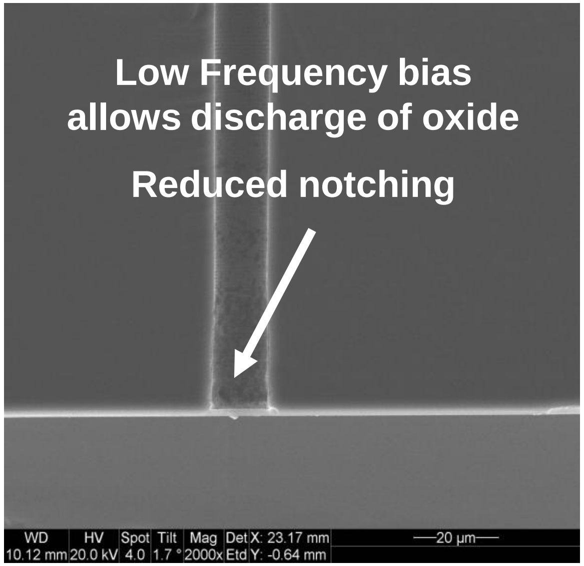


Protective polymer layer



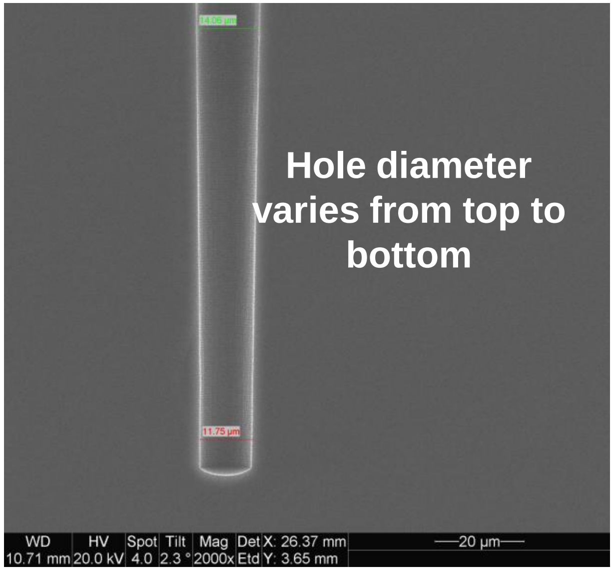
5 µm trenches

Aspect ratio 54:1



Low Frequency bias allows discharge of oxide

Reduced notching

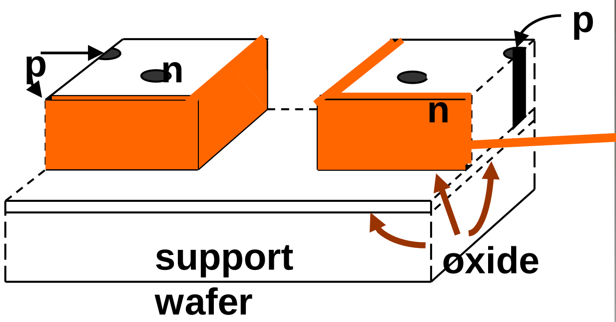


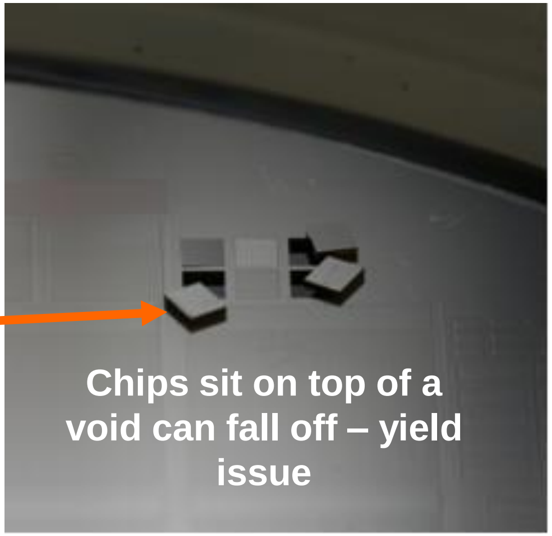
Hole diameter varies from top to bottom

*IEEE Nuclear Science Syposium 2009 N25-164

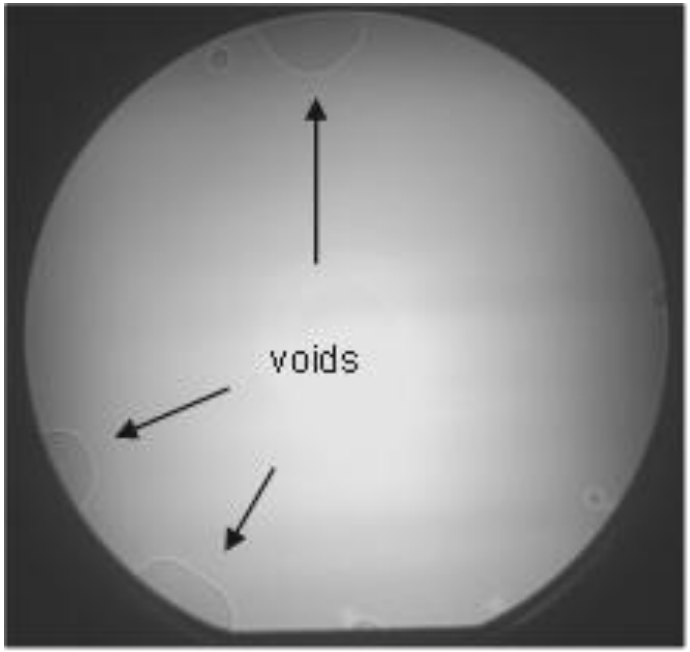
Wafer bonding

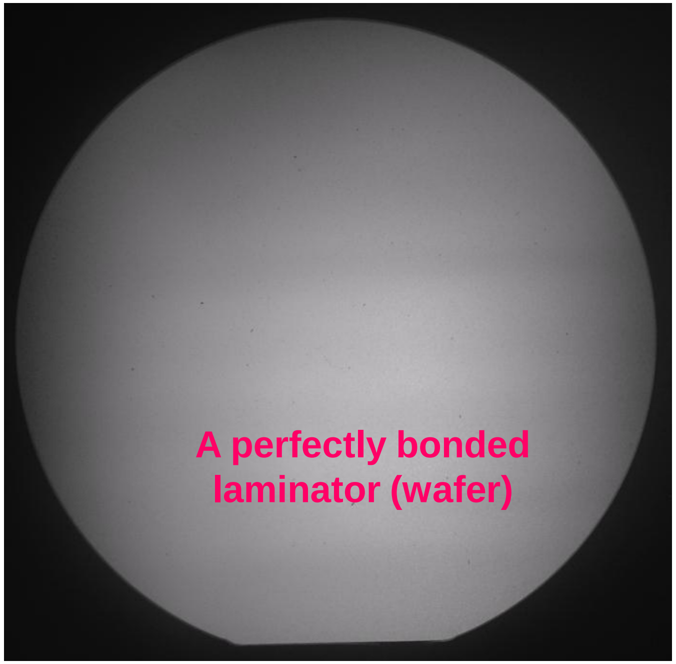
- Support wafer essential to fabricate active edge
- Relieve stress and provide support
- Fusion boding
- Oxide to oxide bonding



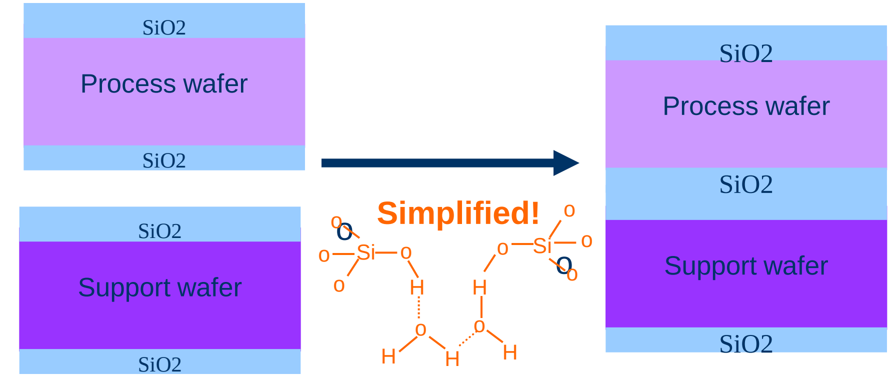


Chips sit on top of a void can fall off – yield issue





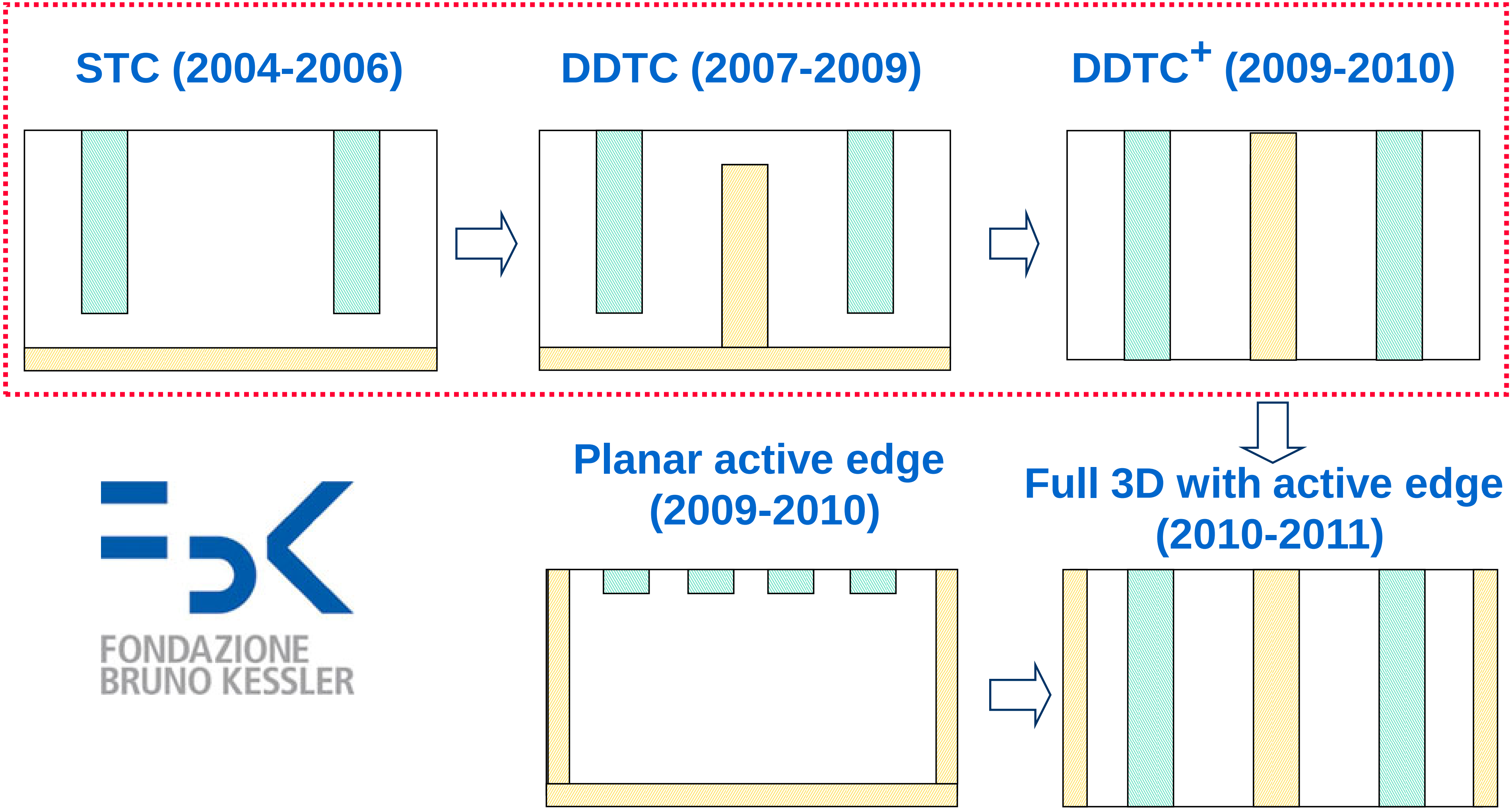
A perfectly bonded laminator (wafer)



Hydrophilic surfaces prepared by a RCA and a piranha rinse

Pre-bonding in a SUSS bonder SB6 at 50ºC, follow by high temp annealing

3D detector technology developments in Trento



STC (2004-2006)

DDTC (2007-2009)

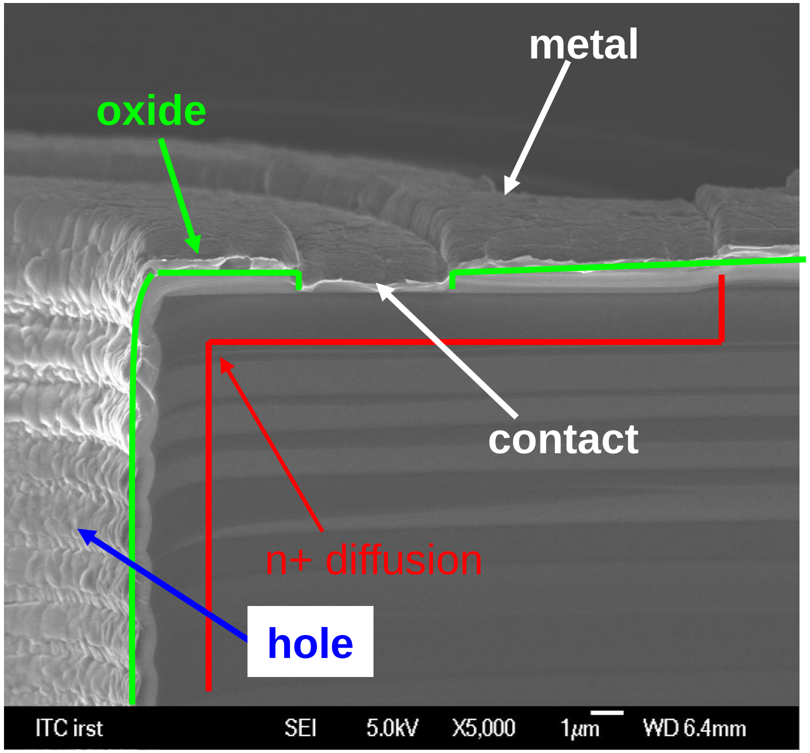
DDTC$^+$ (2009-2010)

Planar active edge (2009-2010)

Full 3D with active edge (2010-2011)

FONDAZIONE
BRUNO KESSLER

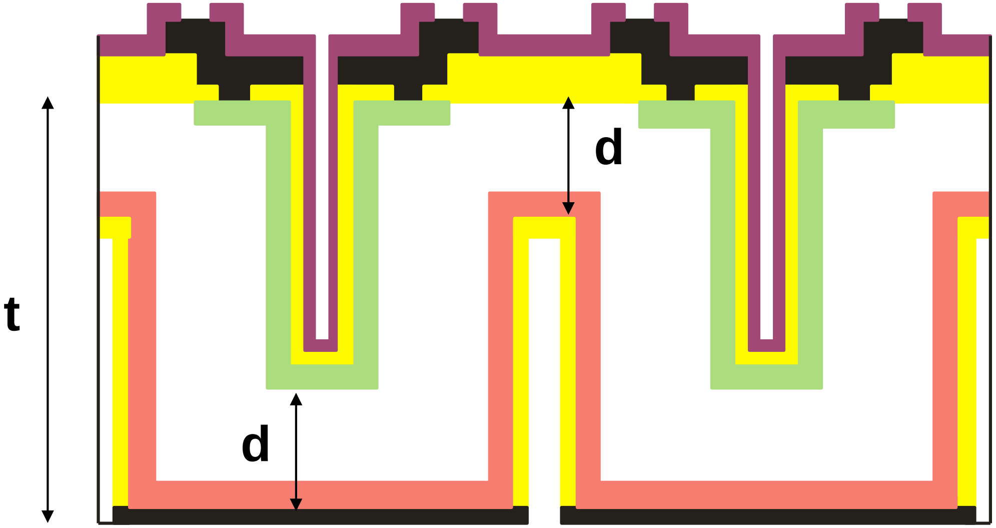
Key process features



- Hole etching by DRIE
- Wide superficial diffusions around holes
  - Contacts at surface only
- Passivation of holes with oxide:
  - Holes are empty (dead regions)

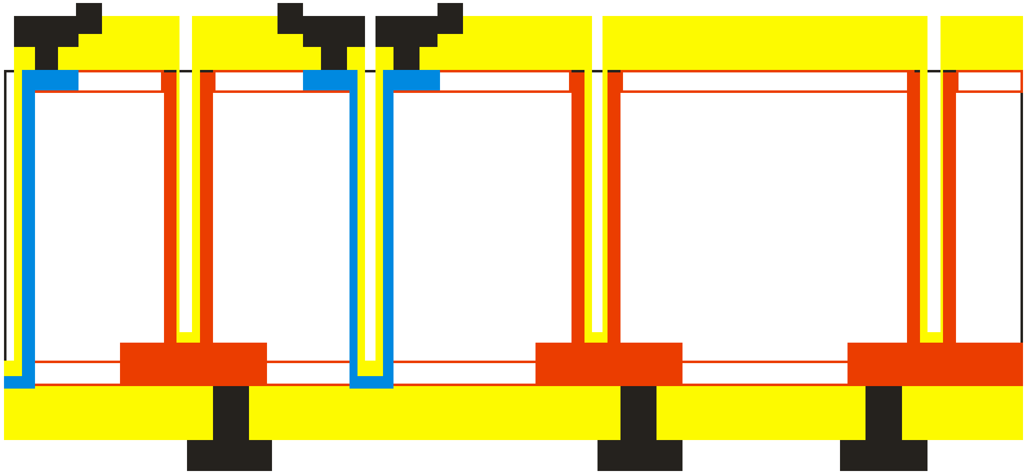
- No support wafer:
  - special care to prevent wafer breakage (edge protection)

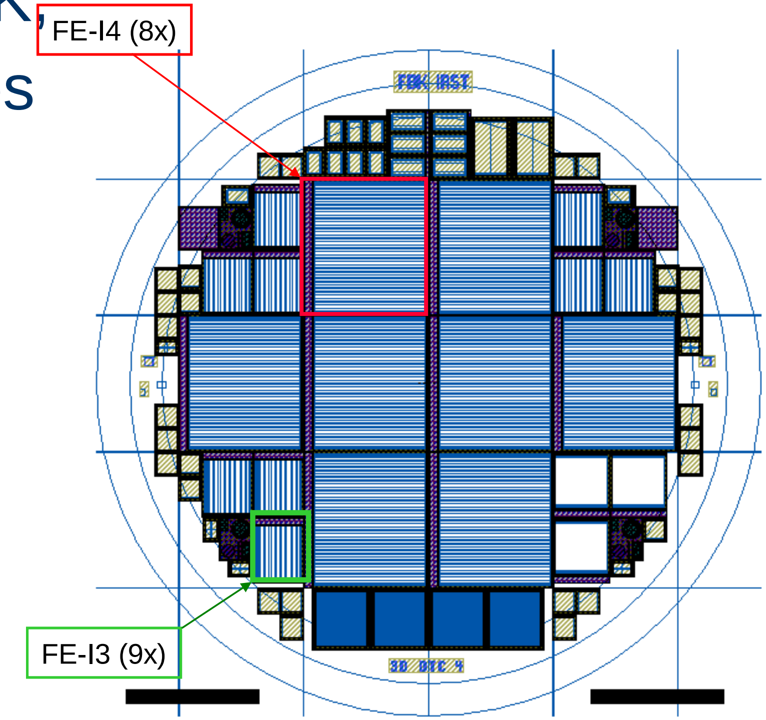
Double-sided approach (3D-DDTC)



3D-DDTC$^+$: passing through columns

- Modified 3D-DDTC technology approach
- No support wafer, back-side accessible:
  (also suitable for dual-readout pixel/strip sensors)
- Allows for “slim-edge” (~200 μm) detectors
- Two batches under fabrication at FBK, one of them for ATLAS IBL prototypes





Double-sided 3D at CNM

- **Columns etched from opposite sides of substrate and don't pass through full thickness**
- **All fabrication done in-house**
- **ICP is a <u>reliable and repeatable</u> process (many successful runs)**

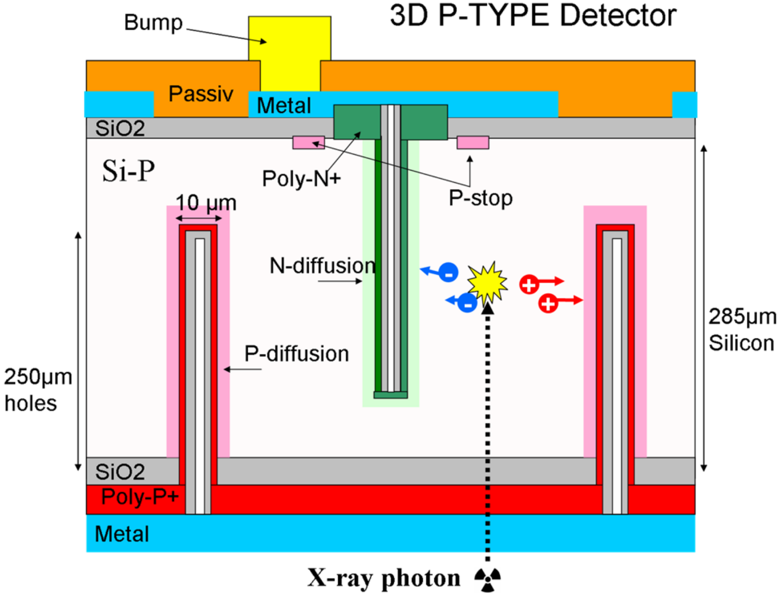
Electrode fabrication:

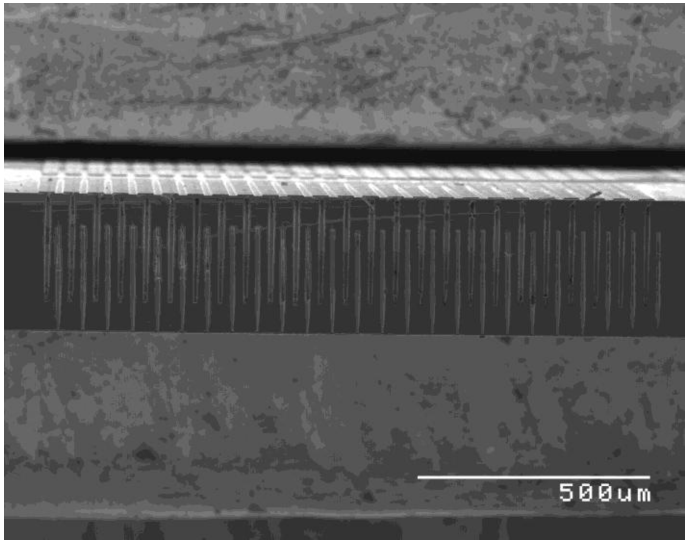
1. **ICP etching of the holes: Bosch process, ALCATEL 601-E**
2. **Holes partially filled with 3 µm LPCVD poly**
3. **Doping with P or B**
4. **Holes passivated with TEOS SiO_2**

Hole aspect ratio 25:1
10µm diameter, 250µm deep
P- and N-type substrates, 285µm thick

See C. Fleta Corral's talk

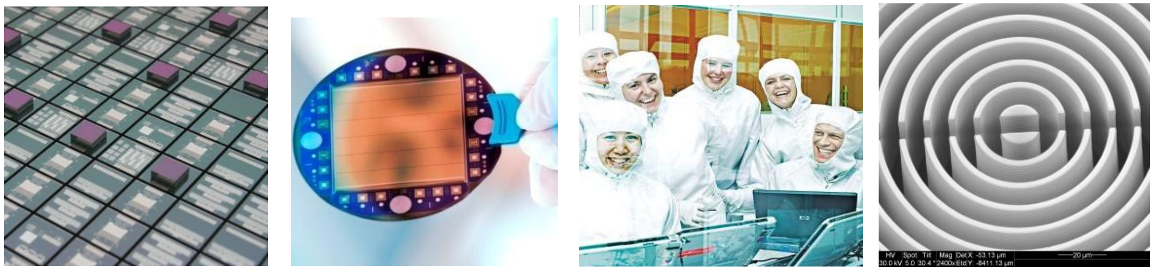
3D P-TYPE Detector



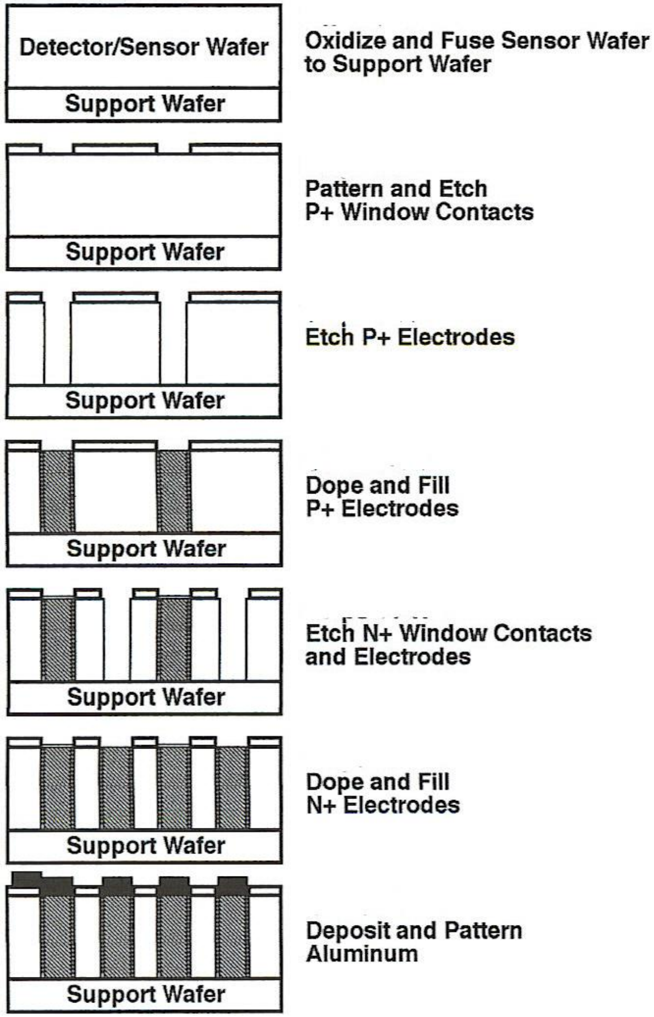


SINTEF MiNaLab (Micro- and Nanotechnology Laboratory)

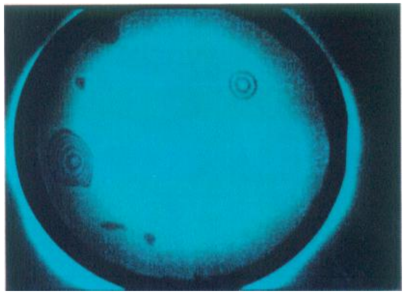
- Shared facility for the University of Oslo and SINTEF with two separate clean room floors:
  SINTEF: 800 m^2
  University of Oslo: 600 m^2
- SINTEF:
  - **Silicon production line with capacity of 10.000 150 mm wafers**
  - **100 mm and 150 mm wafers**
  - **Microenvironments with class 10**
- The most advanced laboratory in Norway for micro- and nanotechnology, situated on the campus of UiO
- 3D Consortium formed in 2006 primarily with Chris Kenney et al. to transfer 3D to a more production environment



KEY STAGES THAT MAKE THIS TECHNOLOGY POSSIBLE



1. WAFER BONDING (mechanical stability). After complete processing this support wafer will be removed.



2. PHOTOLITHOGRAPHY

3. MAKING THE HOLES

4. FILLING THE HOLES

5. DOPING THE HOLES AND ANNEALING

6. METAL DEPOSITION

* C. Kenney, J. Hasi (SLAC)

FILLING AND DOPING THE HOLES

The holes can be filled with doped gas molecules at low pressure and moderate temperatures to form p & n electrodes within the detector.

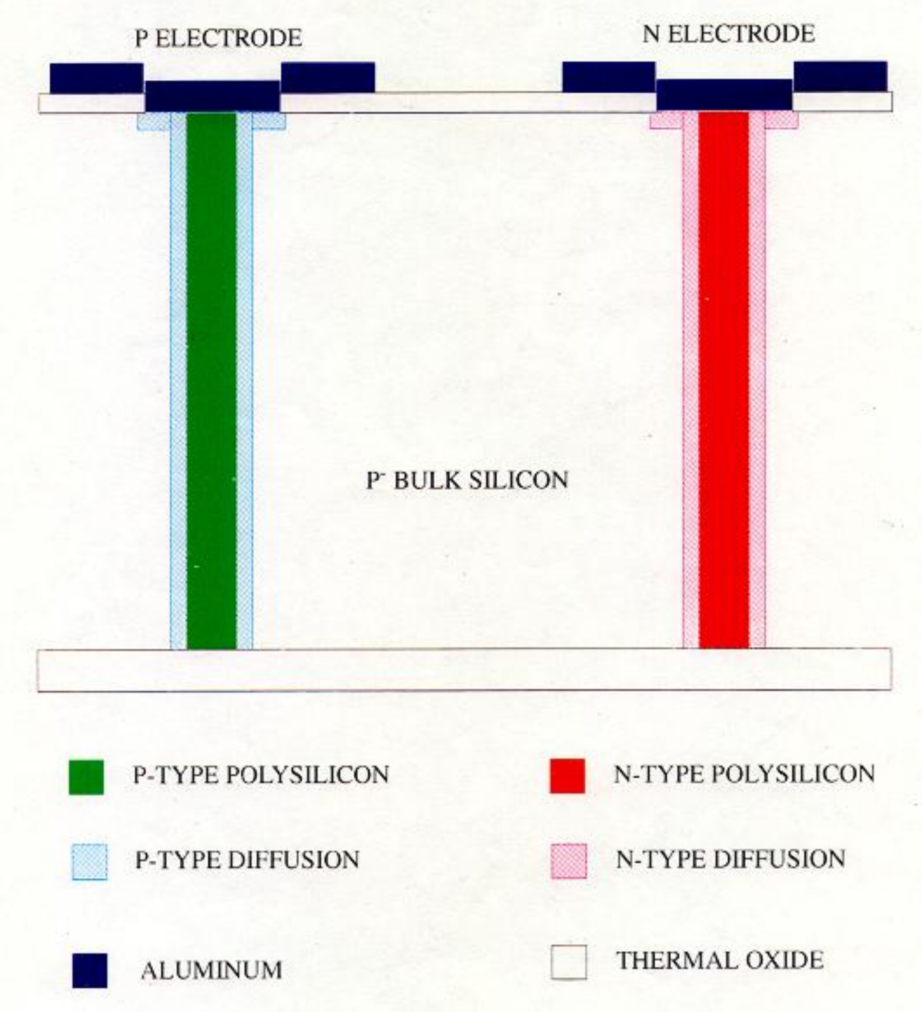
- **POLYCRYSTALLINE SILICON** IS DEPOSITED IN A LOW PRESSURE CHEMICAL VAPOUR DEPOSITION (LPCVD) USING A THERMAL DECOMPOSITION OF SILANE.

$$SiH_4 \xrightarrow{600^\circ C} Si + 2H_2$$

- **DOPED** WITH EITHER BORON OR PHOSPHOROUS TO PRODUCE EITHER N OR P-TYPE ELECTRODES

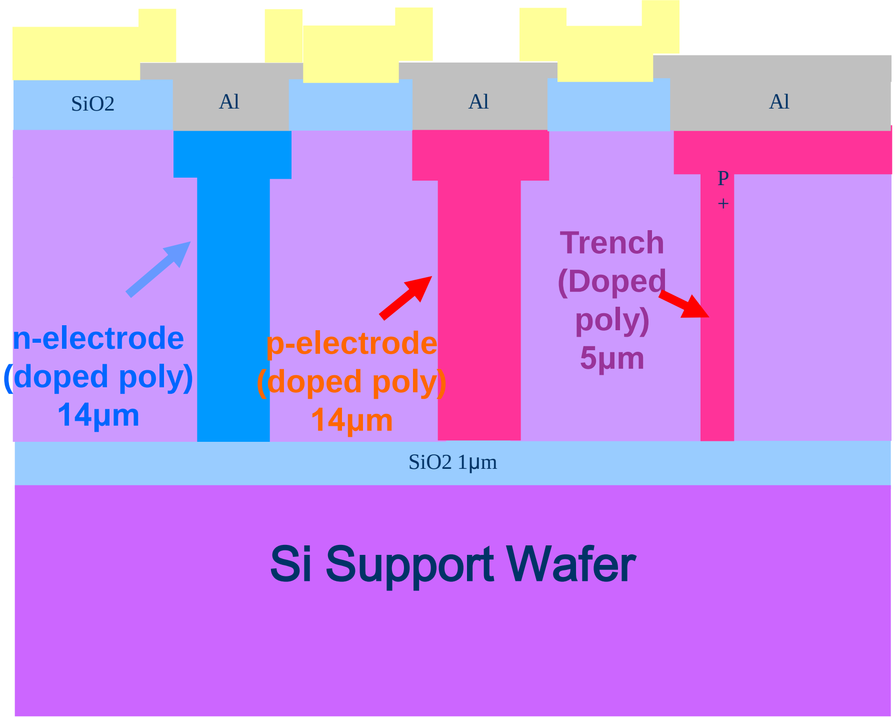
$2P_2O_5 + 5\,Si \rightarrow 4P + 5\,SiO_2$
$2B_2O_3 + 3Si \rightarrow 4\,B + 3\,SiO_2$

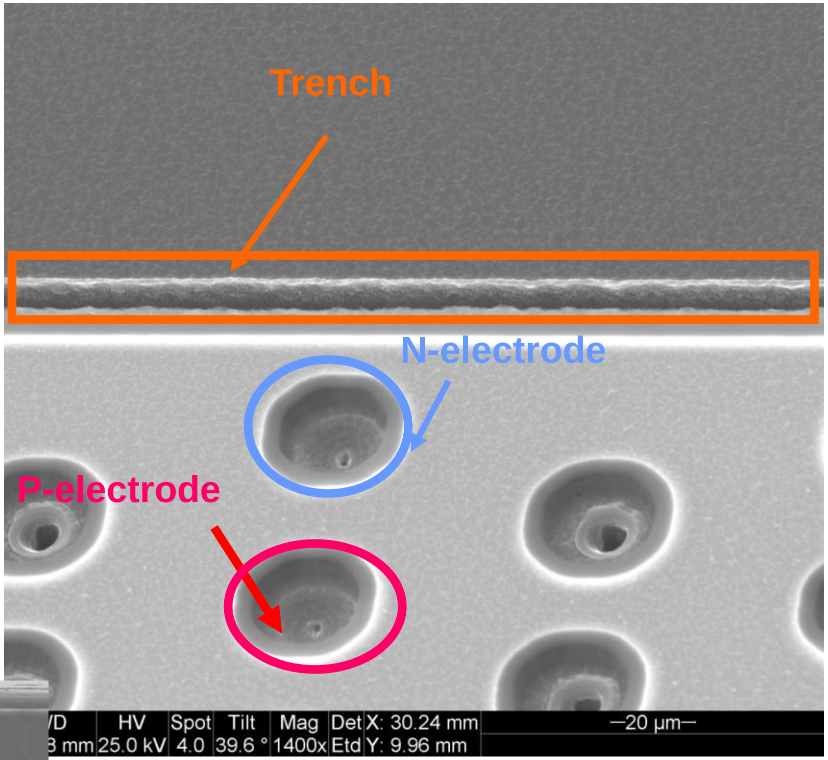
- **ANNEALING** FOLLOWS, IN WHICH THE DOPANTS ARE DIFFUSED INTO THE SURROUNDING SINGLE CRYSTAL SILICON FORMING PN JUNCTIONS

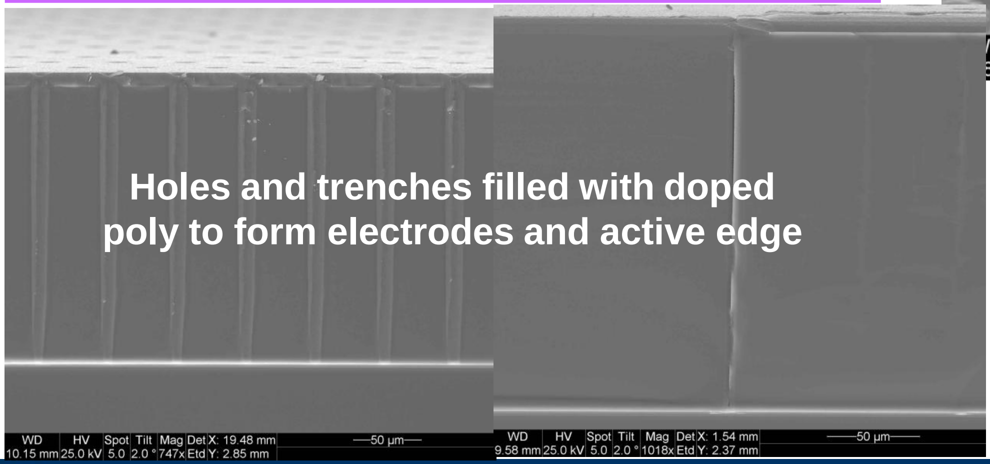


* C. Kenney, J. Hasi (SLAC)

SINTEF/Stanford process



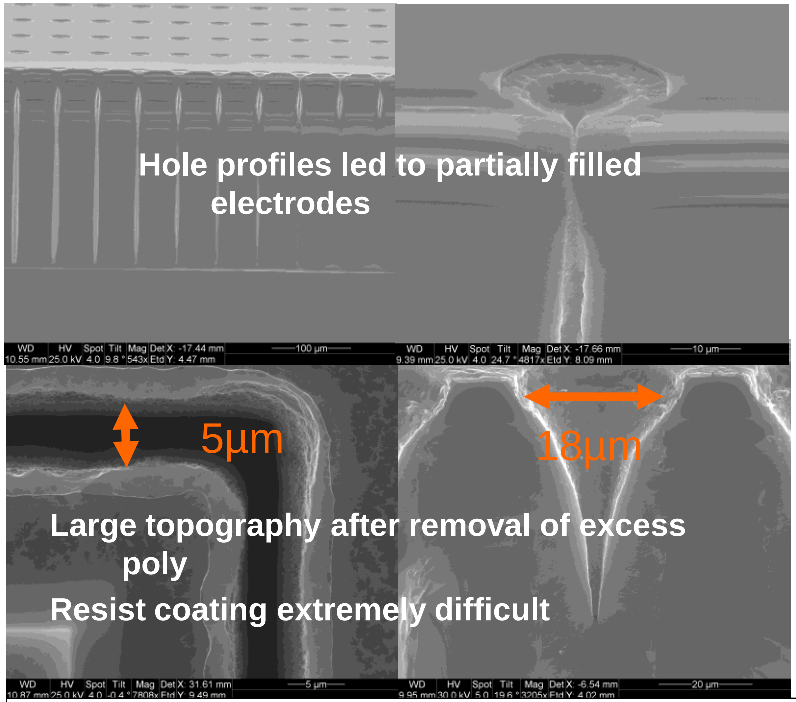




Holes and trenches filled with doped poly to form electrodes and active edge

- Support wafer required
- Through wafer electrode
- Active electrodes and active edges
- Electrodes filled with poly

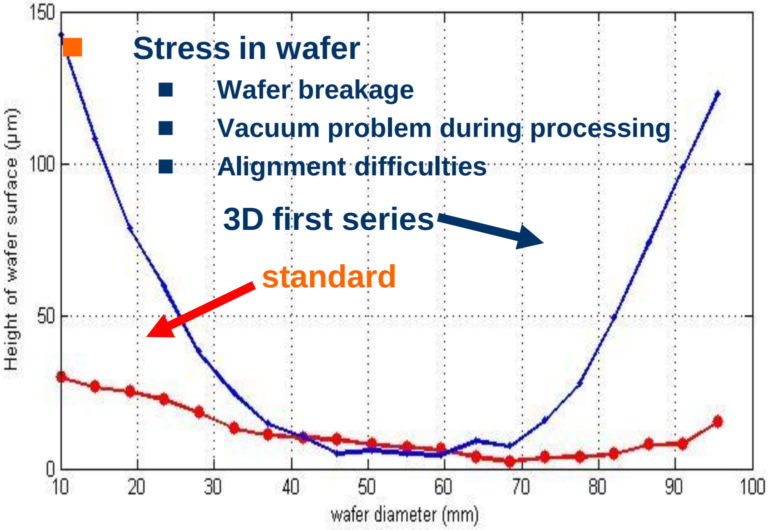
Issues in the first SINTEF fabrication



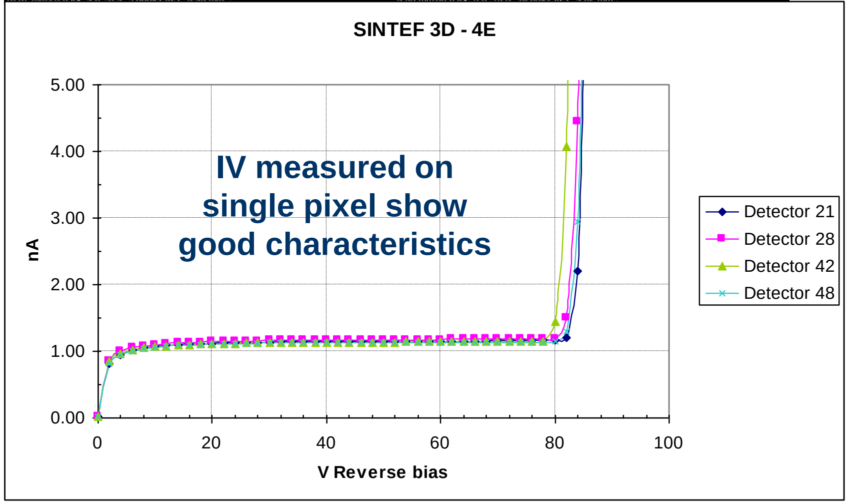
Hole profiles led to partially filled electrodes

Large topography after removal of excess poly

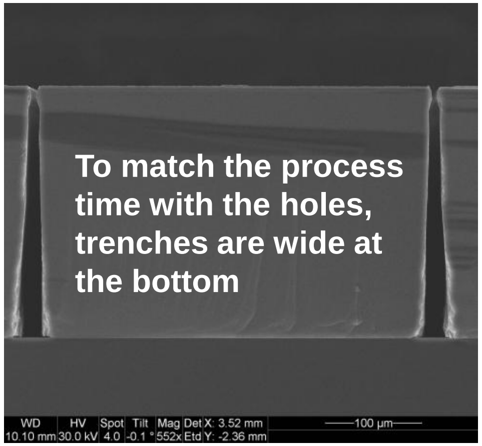
Resist coating extremely difficult



- **Stress in wafer**
  - **Wafer breakage**
  - **Vacuum problem during processing**
  - **Alignment difficulties**



IV measured on single pixel show good characteristics

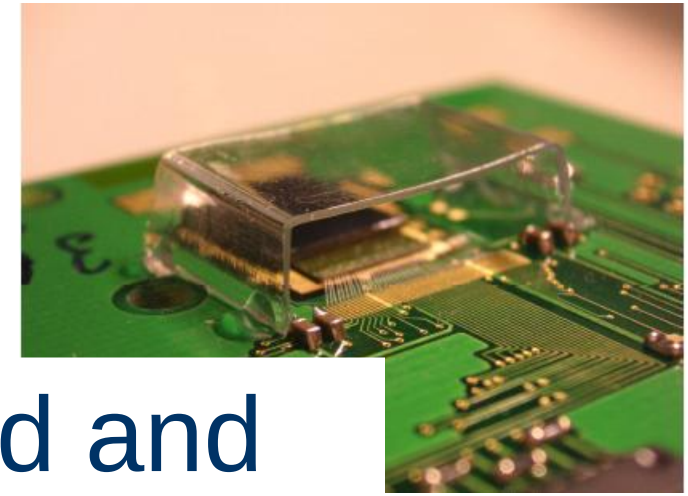


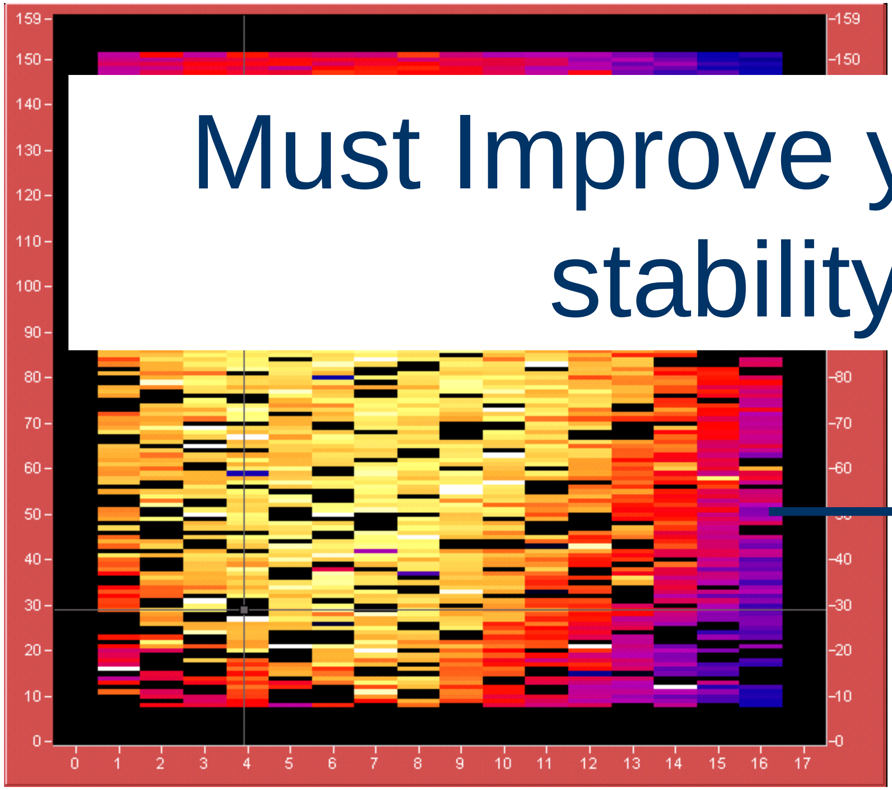
To match the process time with the holes, trenches are wide at the bottom

- **Wafer breakage**
- **Difficult lithography**
- **Unfilled electrodes**
- **Wide trenches**
- **Extremely low yield**

Issues in the first SINTEF fabrication

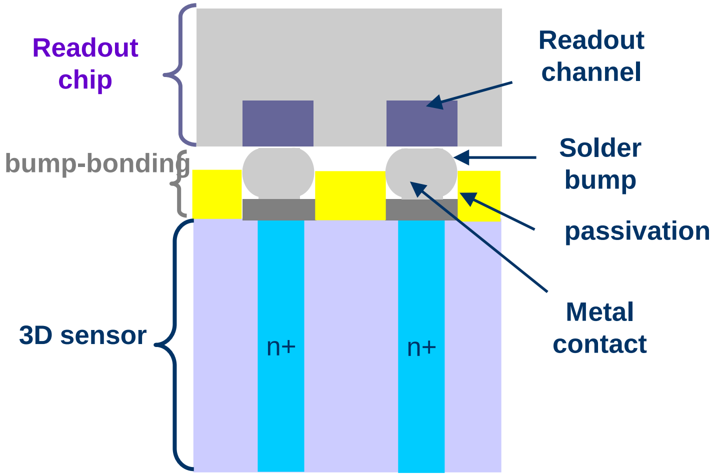
- Noise was too high for a good convergence
- All modules suffered from irreversible breakdown after some hours of operation
- Dicing through a p-n junction could cause the breakdown since substrates are n-type and active edge is p-type





Must Improve yield and stability!

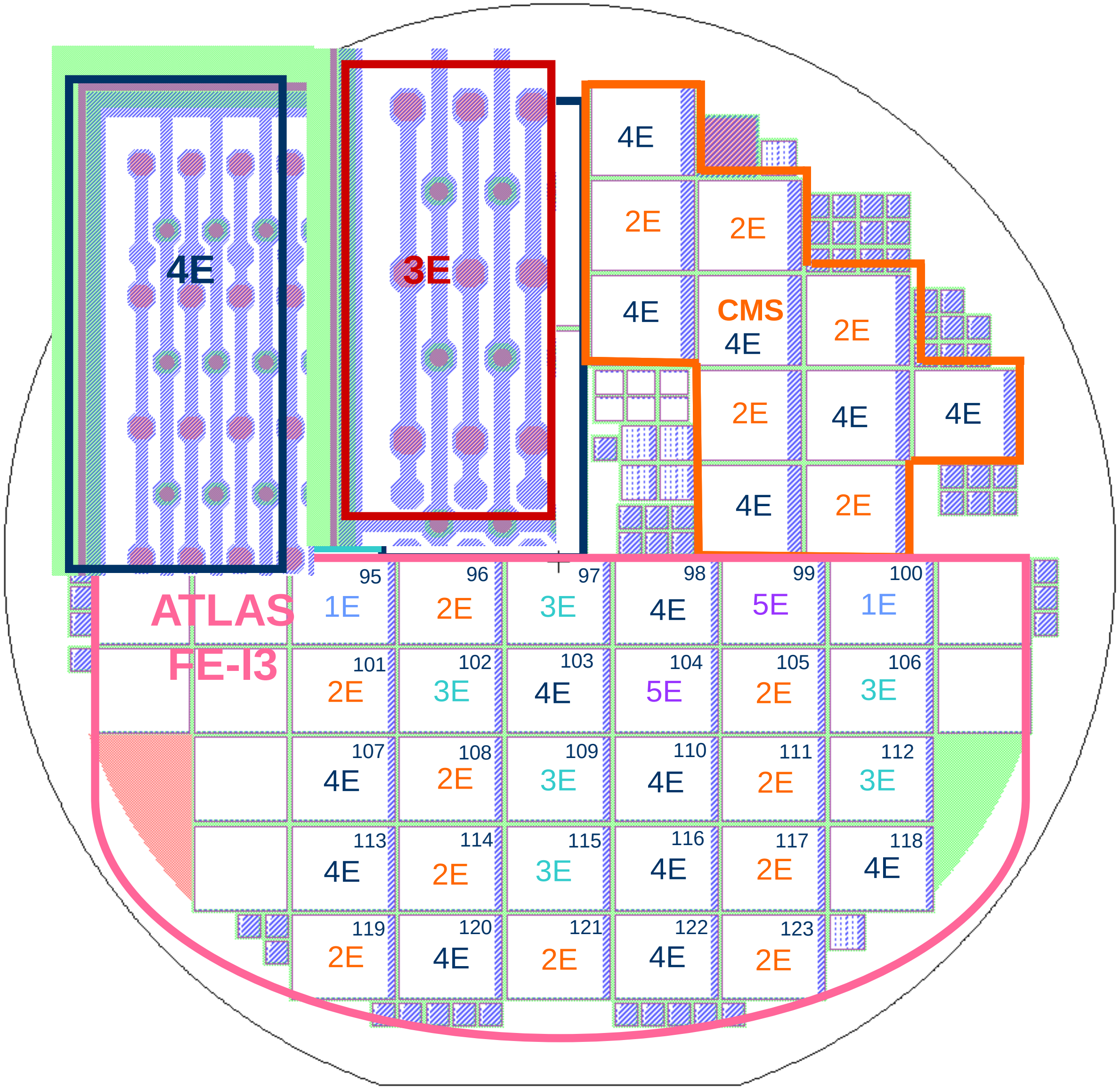
ssfully
rom an Am-
241 source



Each square corresponds to the number of hits per pixel

*data taken by E. Bolle, H.Gjersdal and O. Rohne at the University of Oslo

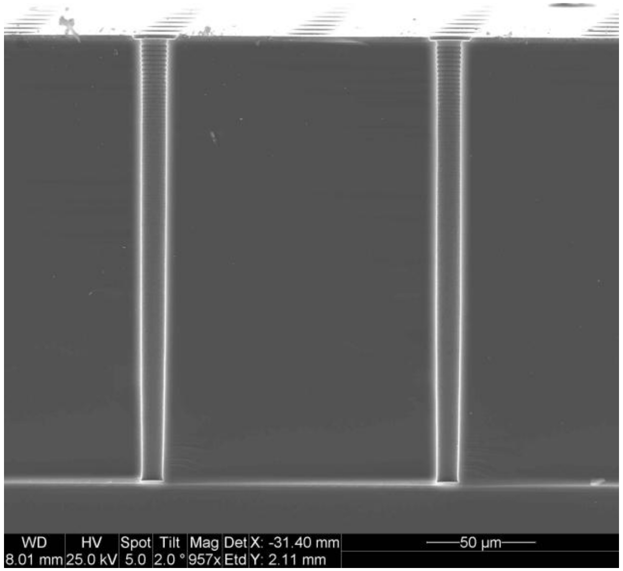
Improvements in second run

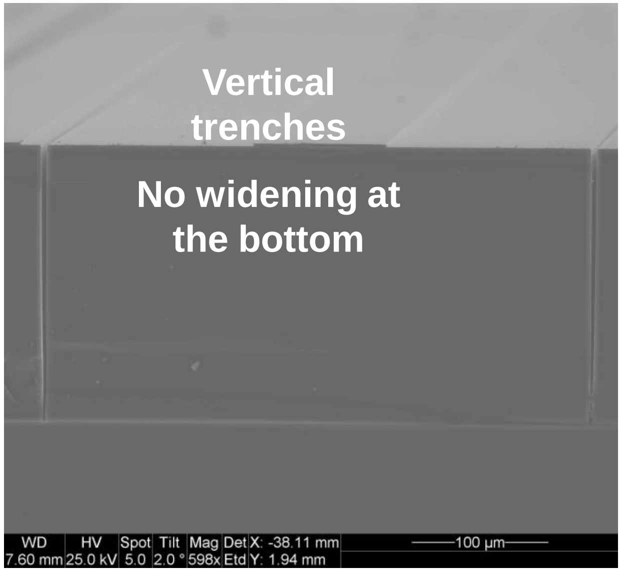


- To improve yield and stability
- P-type wafers were used
  - Active edge will be of the same type as the bulk
  - No fragile pn-junction
  - No irreversible breakdown (hopefully)
- Narrower trenches
- Different hole profiles
- Extra nitride layer
  - A better doping barrier
  - Protects the field oxide
  - keeps symmetry on both back and front side
- Polyfilling at Stanford
- Oxygen free (diborane doping) at Stanford to improve electrode efficiency

Improvements in second run

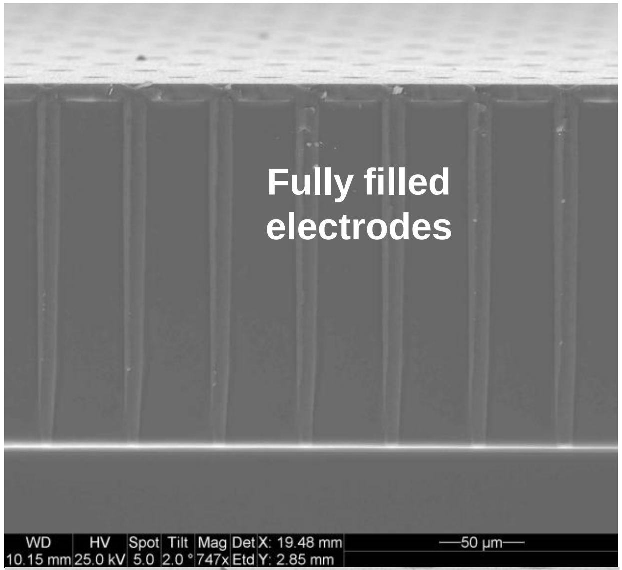
After DRIE

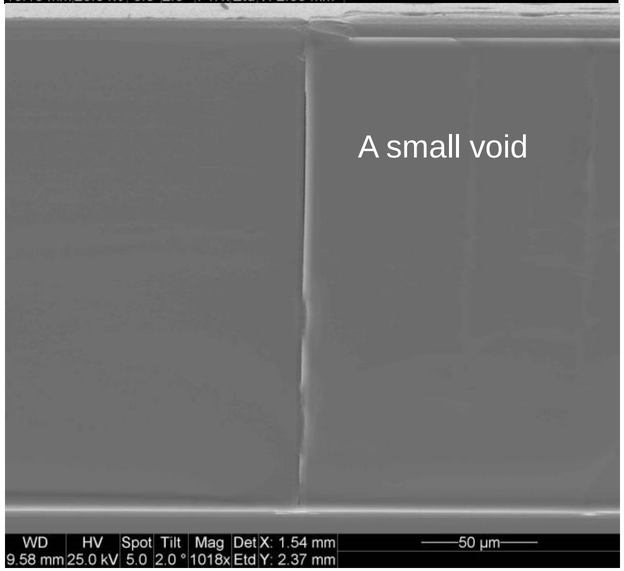



Vertical trenches

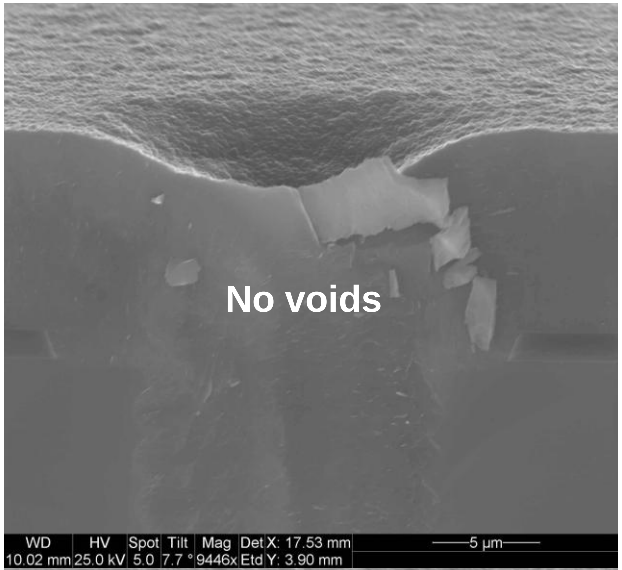
No widening at the bottom

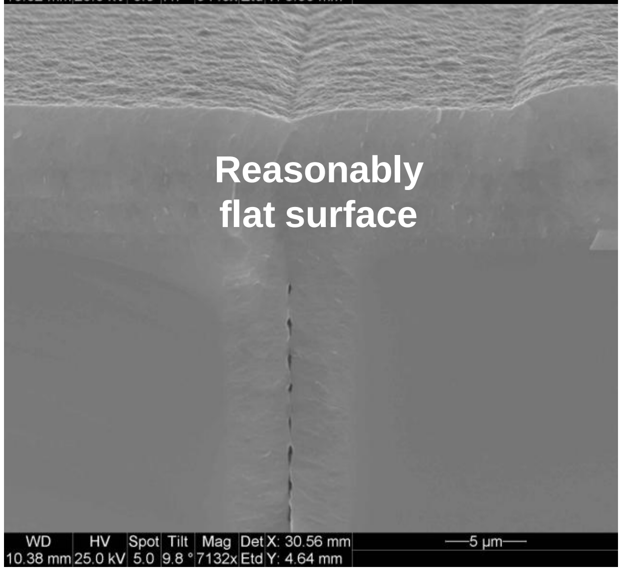
After polyfilling


Fully filled electrodes


A small void

After polyfilling


No voids

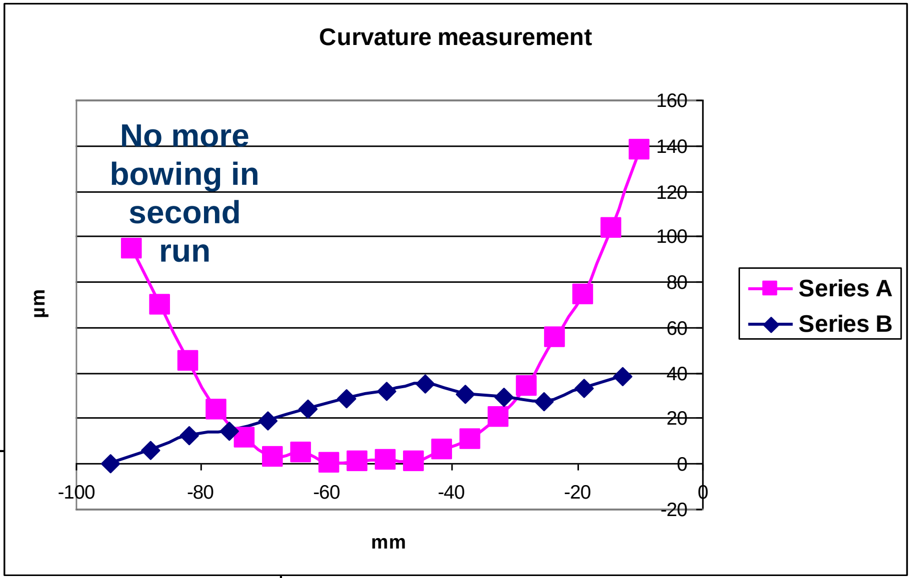

Reasonably flat surface

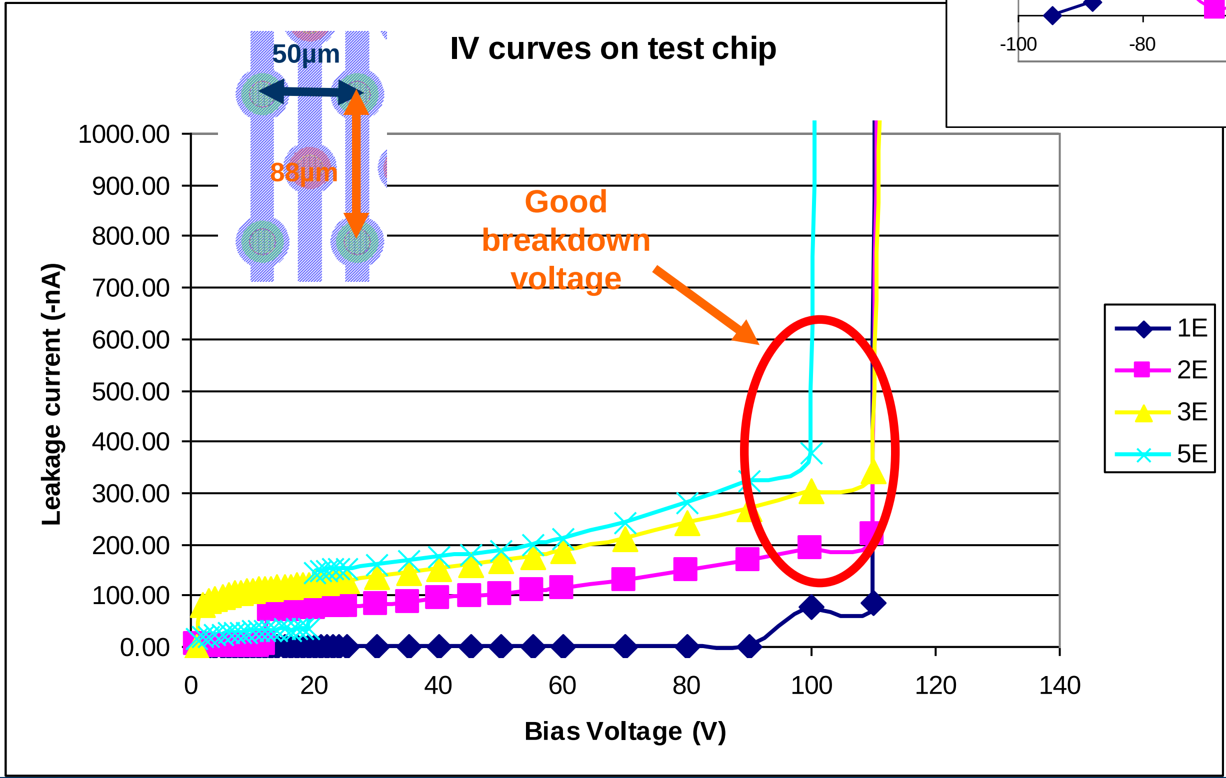
Improvements in second run

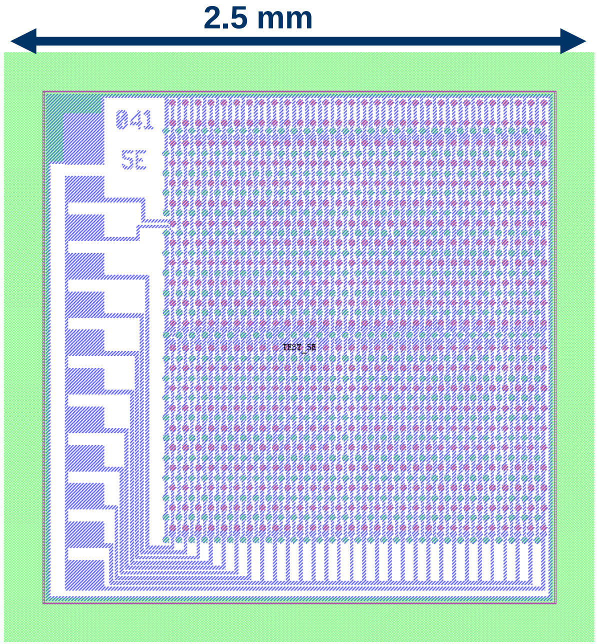
No more bowing in wafers

18 out of 24 wafers survived the process!

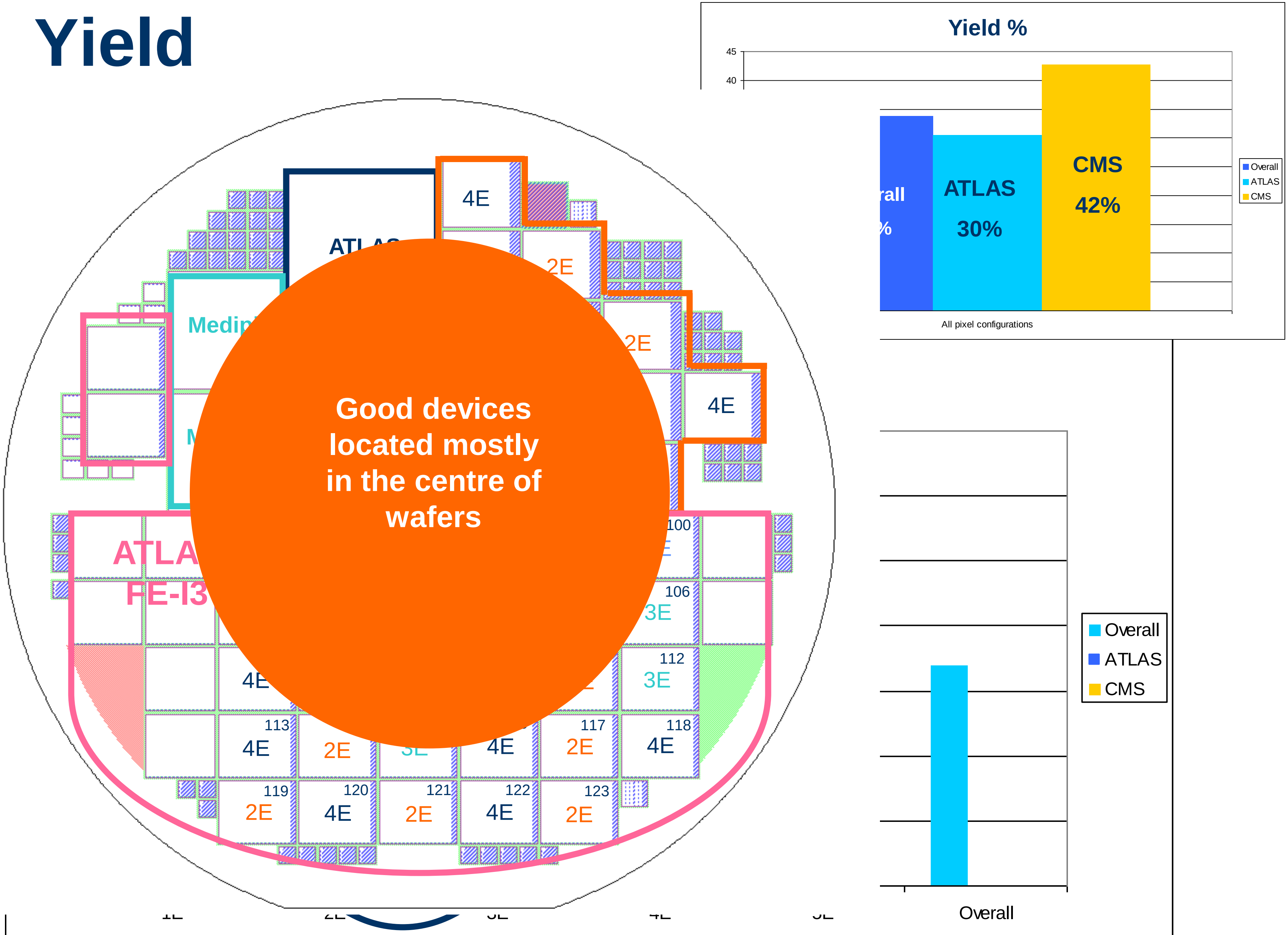
Better filled electrodes also allow easier lithography





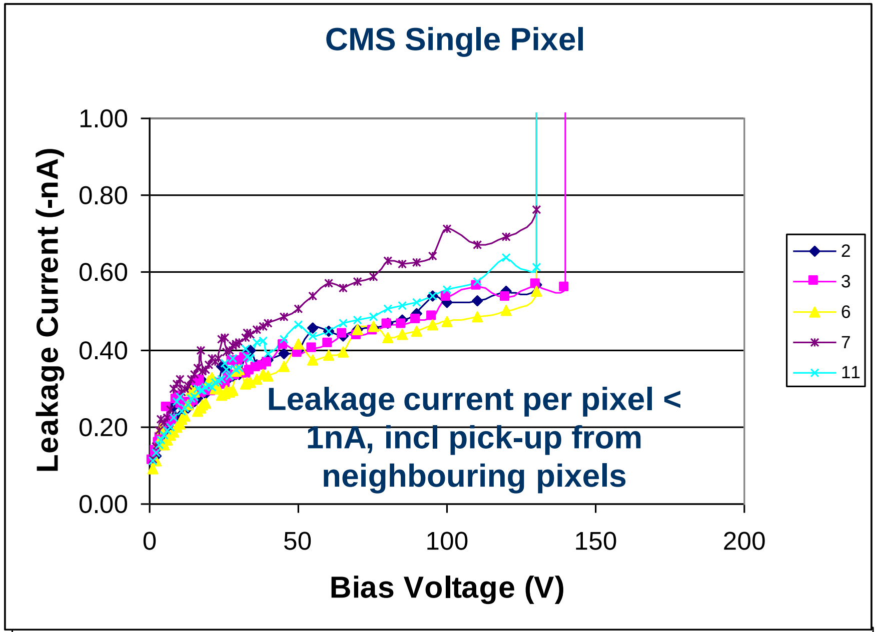


Yield

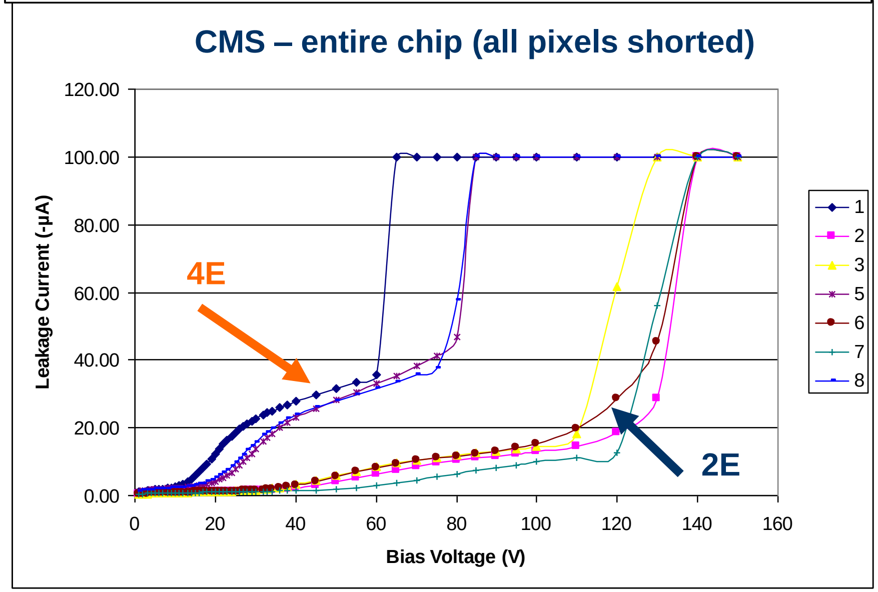


Good devices located mostly in the centre of wafers

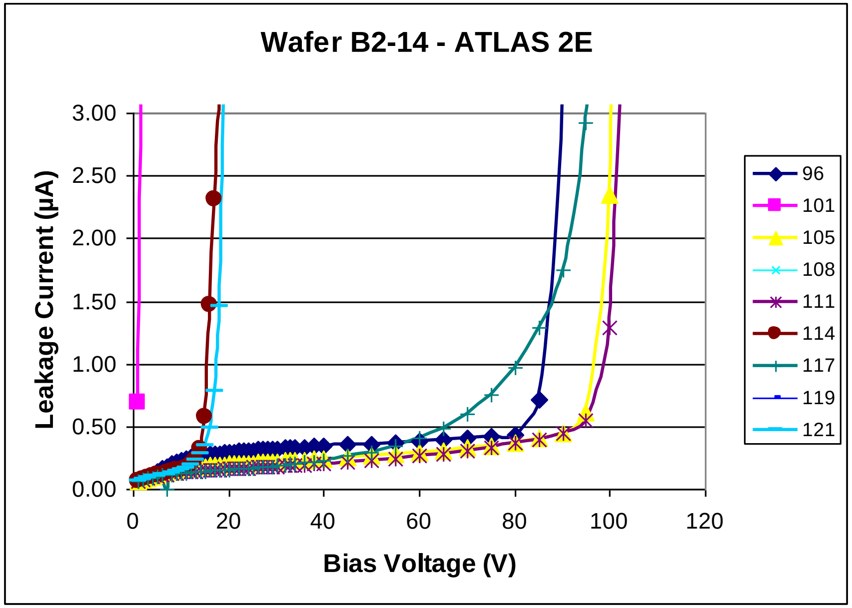
Tests - IV Measurement


CMS Single Pixel

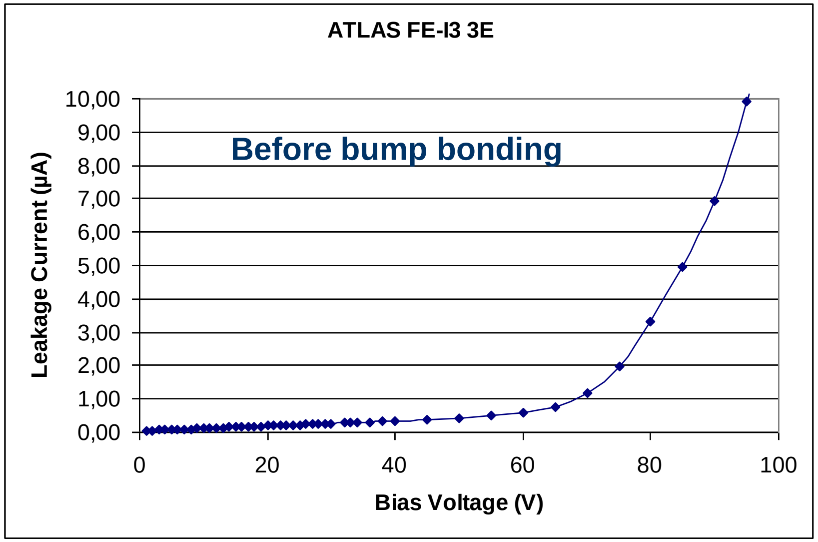
Leakage current per pixel < 1nA, incl pick-up from neighbouring pixels


CMS – entire chip (all pixels shorted)

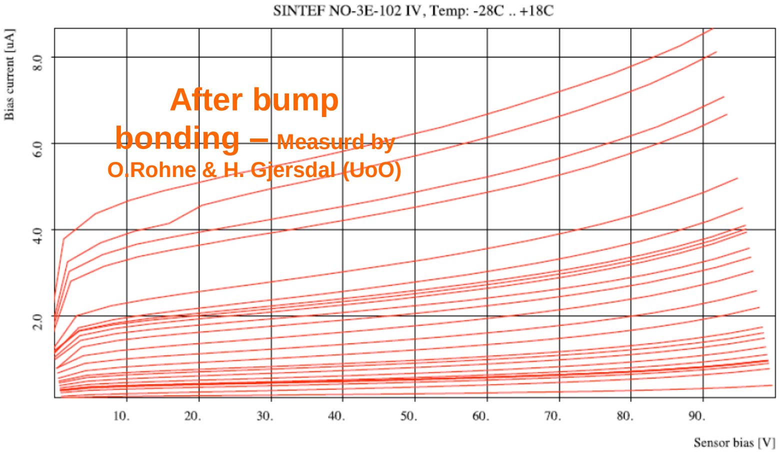
- 4E devices have a higher leakage current and lower breakdown voltage
- But some have characteristics as good as the 2Es
- Same for both ATLAS and CMS
- Breakdown voltage about 100 V
- Good sensors from wafer look promising


Wafer B2-14 - ATLAS 2E

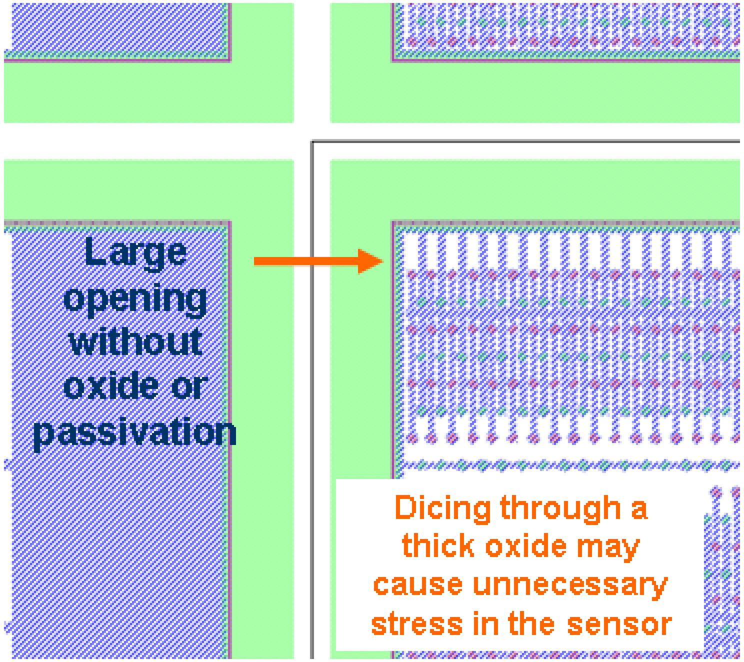
Tests - IV Measurement (ATLAS)



- 2 wafers were bump-bonded – ATLAS devices
- Degradation of IV after bump bonding
- Cooling helps and data was recorded at CERN test beam
- Possible copper/metal contamination through the large openings
- Surface related issues/ humidity
- More tests required



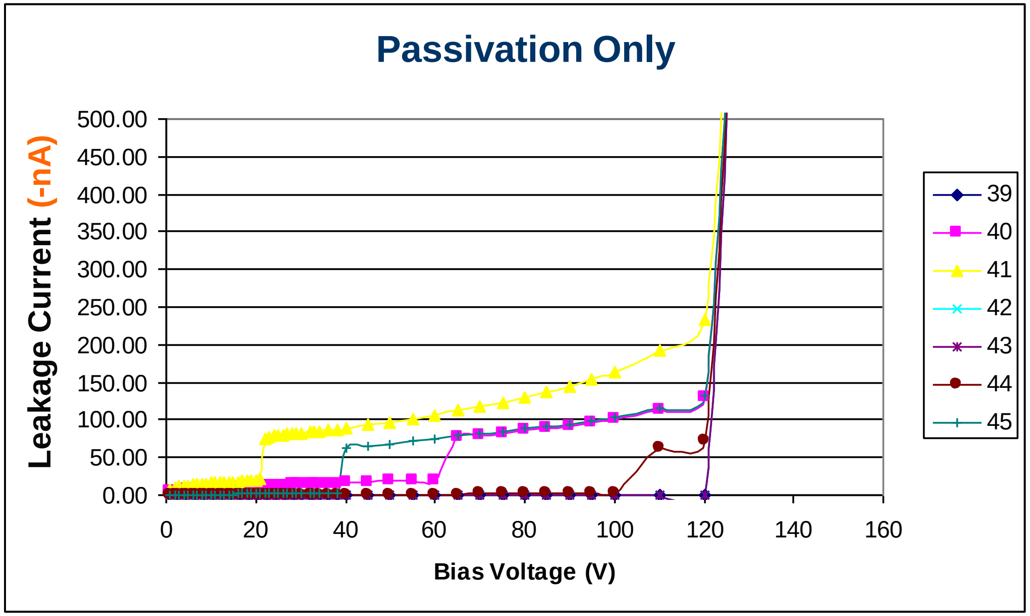
Post test beam IV curves at different temperatures :O. Rohne and H. Giersdal

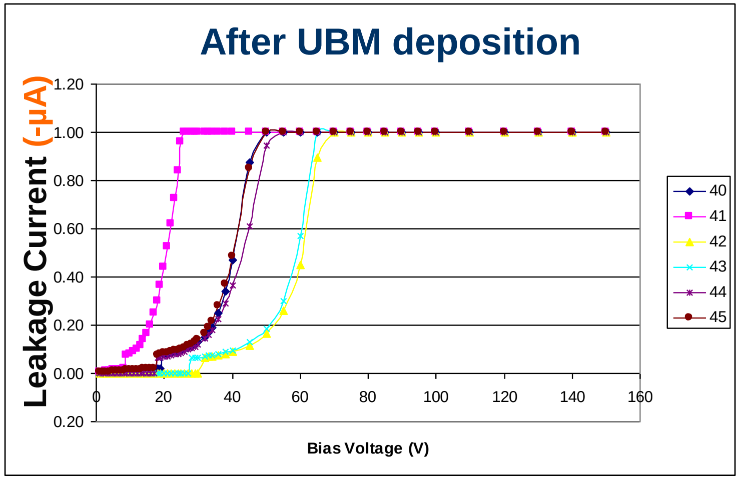


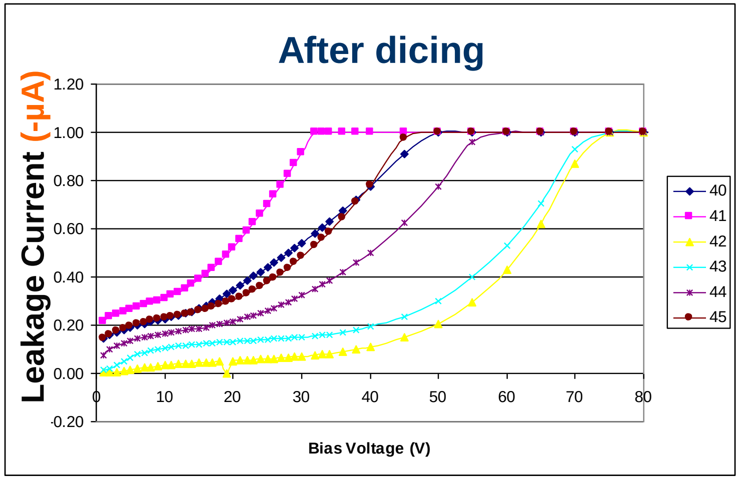
Large opening without oxide or passivation

Dicing through a thick oxide may cause unnecessary stress in the sensor

Tests - IV Measurement (Test diodes - Post UBM)

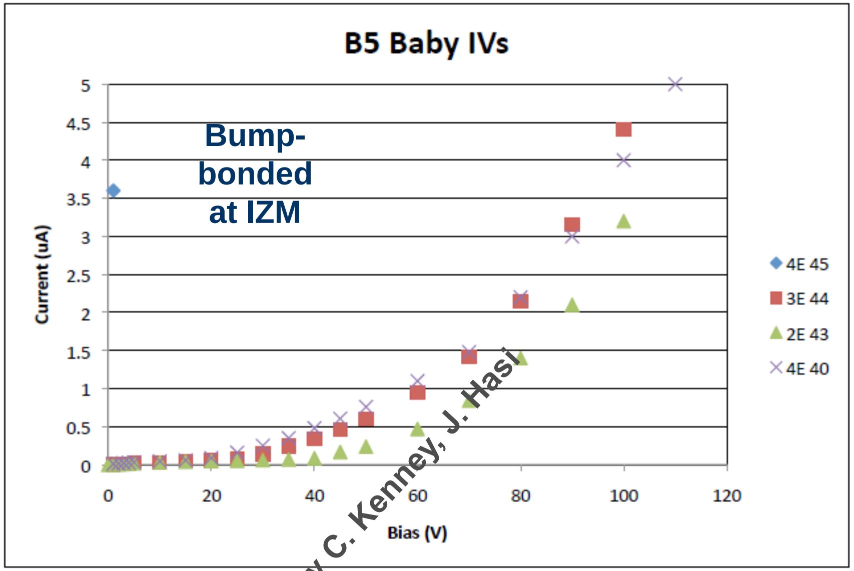






- IV measured on various wafers
  - Before bump-bonding (with passivation only)
  - With UBM
  - With UBM and diced
- Results show IV degradation occurred already after UBM deposition

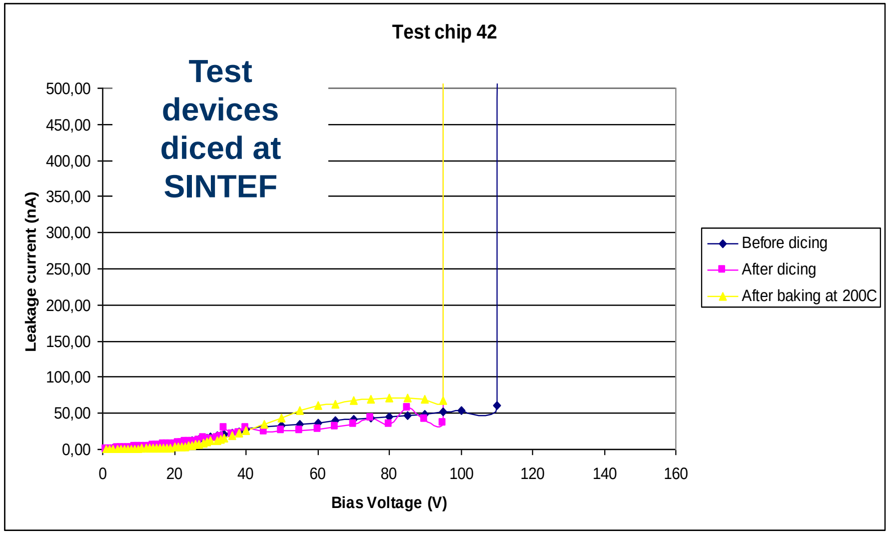
Tests – IV (Test diodes - Post UMB: Indium & Cu, Ni, Au)



B5 Baby IVs

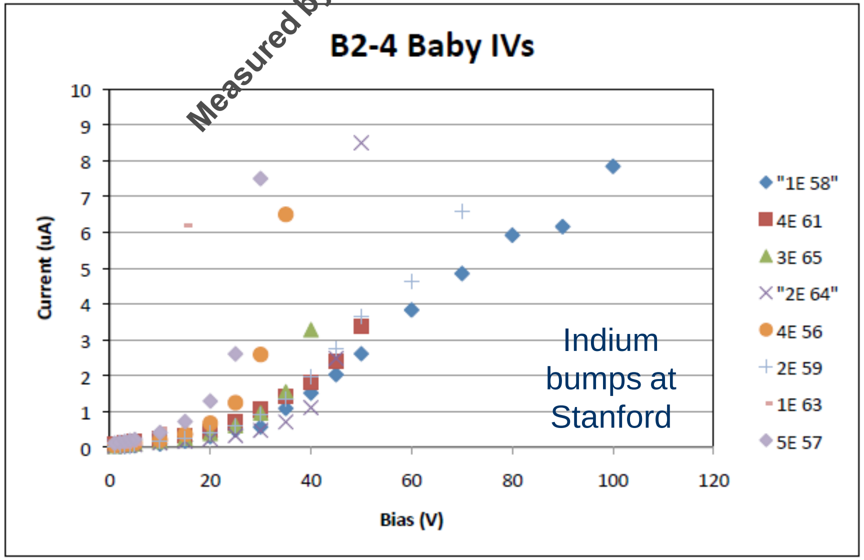
Bump-bonded at IZM

Measured by C. Kenney, J. Hasi



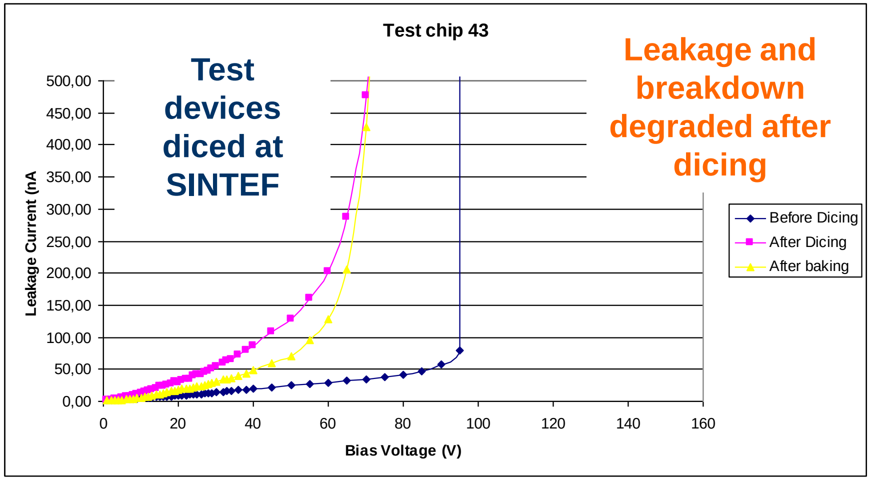
Test chip 42

Test devices diced at SINTEF



B2-4 Baby IVs

Indium bumps at Stanford

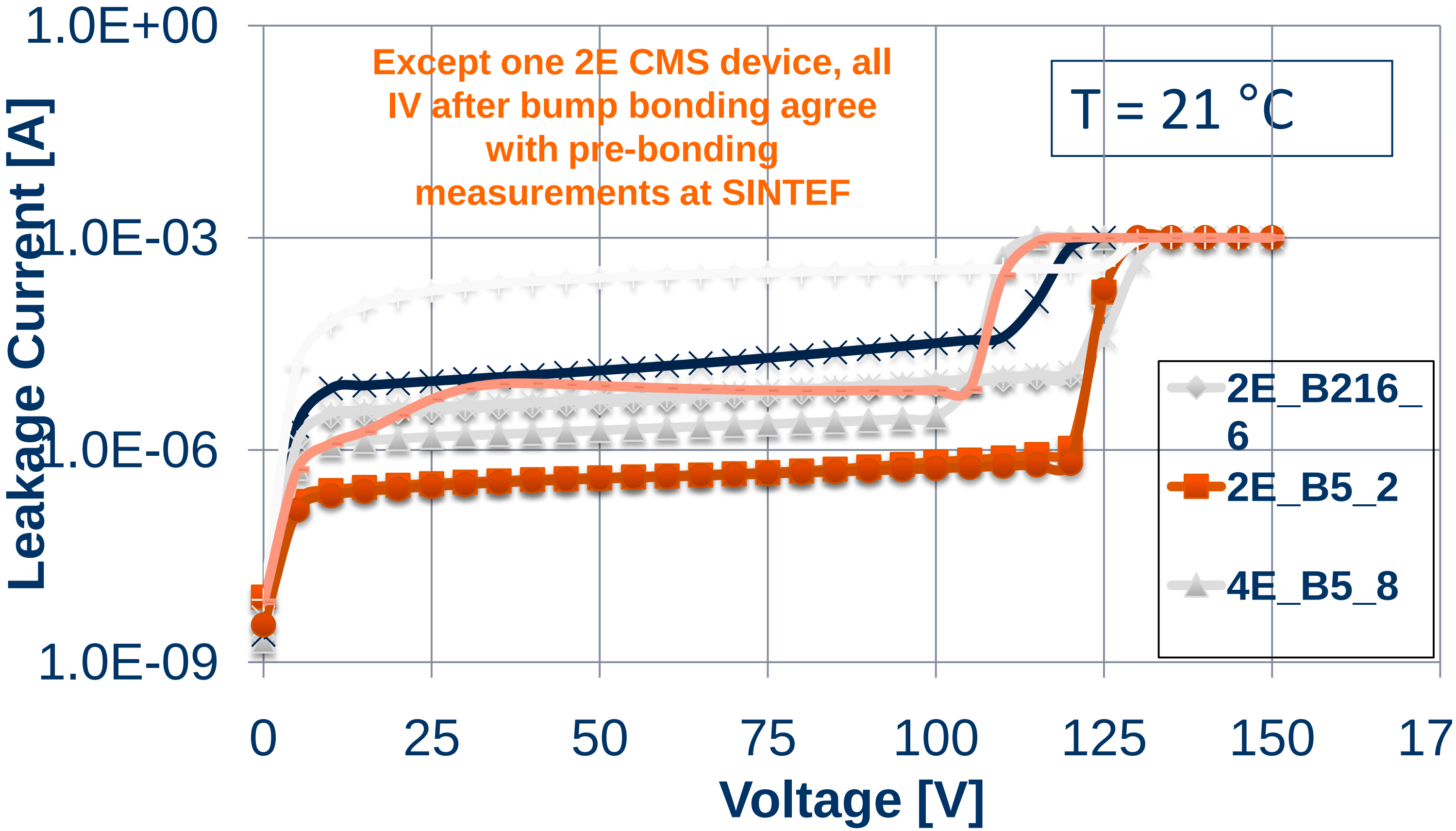


Test chip 43

Test devices diced at SINTEF

Leakage and breakdown degraded after dicing

Tests - IV Measurement (CMS - Post UBM)



Except one 2E CMS device, all IV after bump bonding agree with pre-bonding measurements at SINTEF

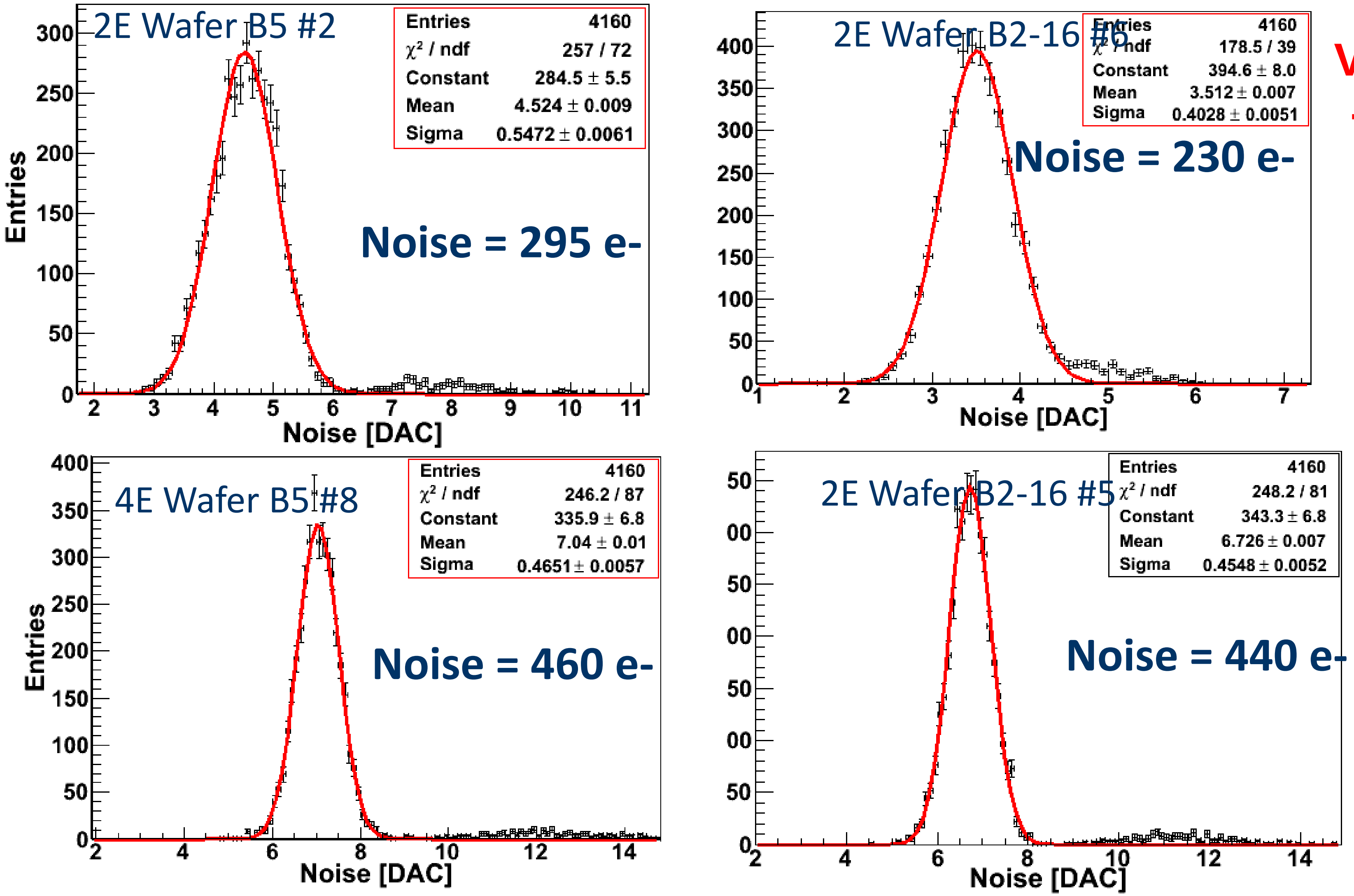
E.Alagoz[1], O.Koybasi[1], K.Arndt[1], D.Bortoletto[1], I.Shipsey[1], G.Bolla[1], R.Riviera[2], M.Turqueti[2], L.Uplegger[2] and S.W.L.Kwan[2]

[1]Purdue University

[3]Fermilab

Detector	Voltage [V]	Purdue IV [µA]	SINTEF IV [µA]	Breakdown
2E-WB5-2	40	0.7	1	120
2E-WB2-16-6	40	5	5	120
4E-WB5-8	40	2	5	100
4E-WB2-16-5	40	10	15	100

Tests - Noise (CMS - Post UBM)



V = -40 V

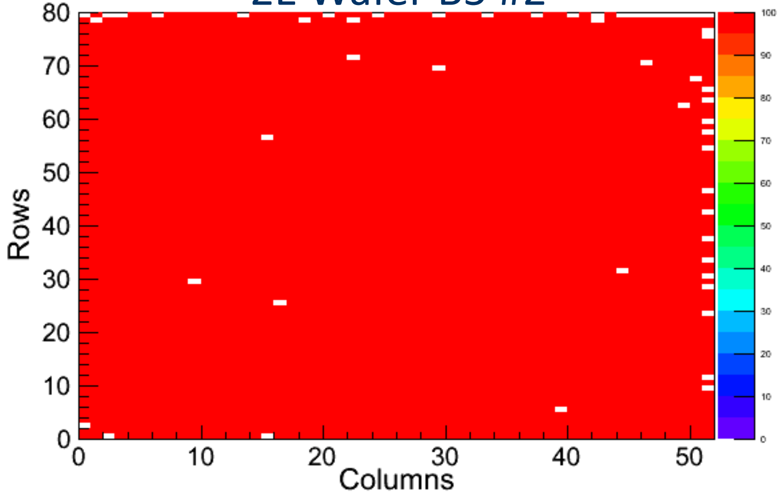
T=21 °C

1 DAC = 65.5 e-

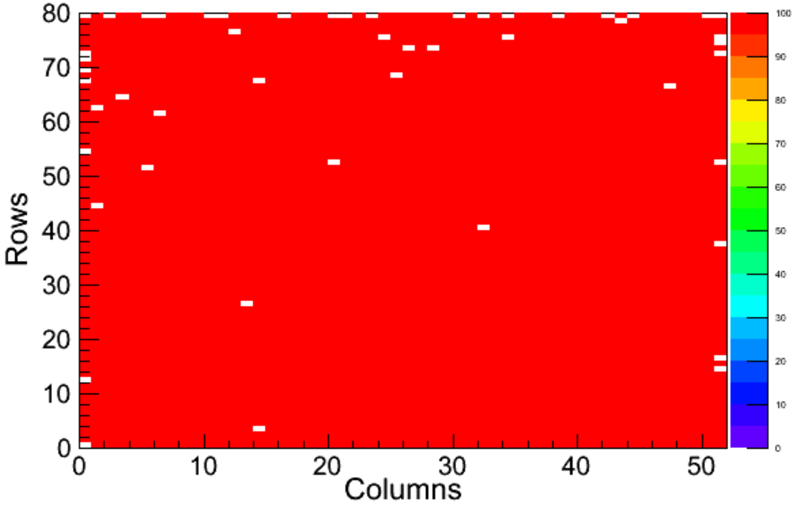
E.Alagoz[1], O.Koybasi[1], K.Arndt[1], D.Bortoletto[1], I.Shipsey[1], G.Bolla[1], R.Riviera[2], M.Turqueti[2], L.Uplegger[2] and S.W.L.Kwan[2]
[1]Purdue University, [3]Fermilab

Test – bump bonding tests

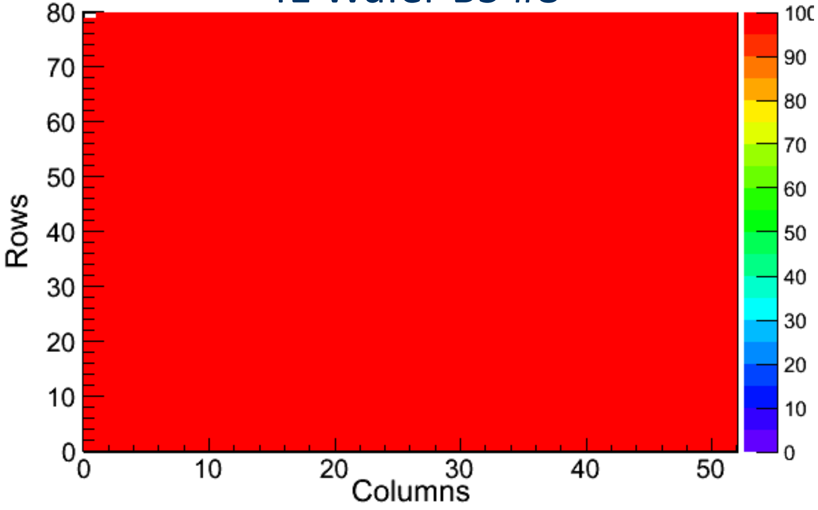
2E Wafer B5 #2



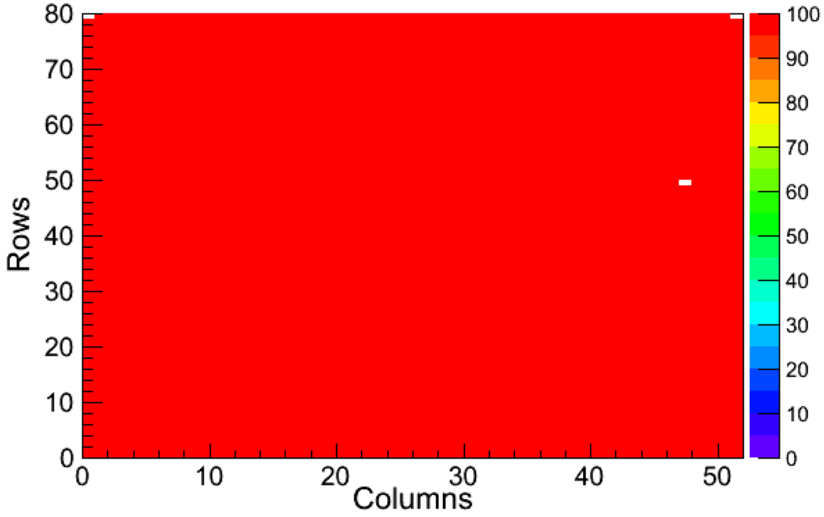
2E Wafer B2-16 #6



4E Wafer B5 #8



4E Wafer B2-16 #5



E.Alagoz[1], O.Koybasi[1], K.Arndt[1], D.Bortoletto[1], I.Shipsey[1], G.Bolla[1], R.Riviera[2], M.Turqueti[2], L.Uplegger[2] and S.W.L.Kwan[2]

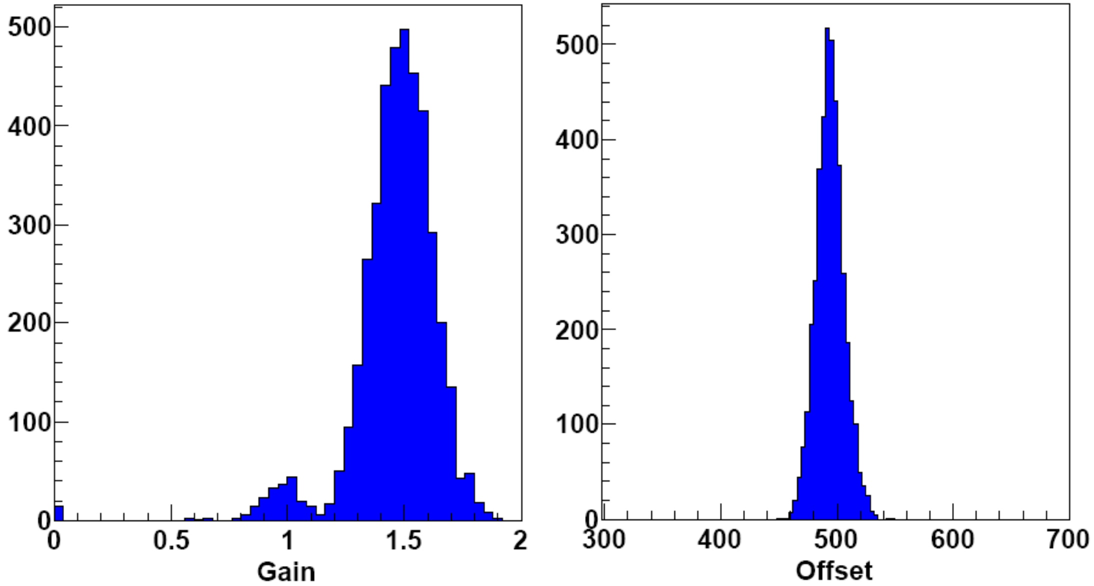
[1]Purdue University, [3]Fermilab

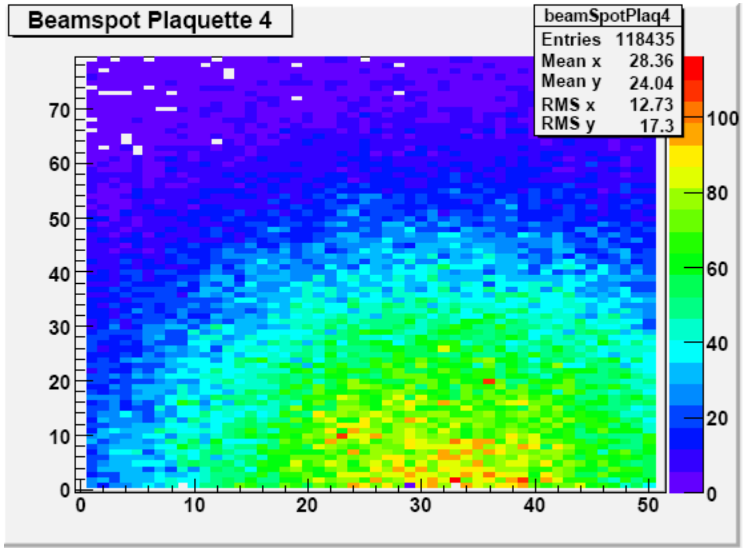
FNAL with 120 GeV protons (CMS 2E)

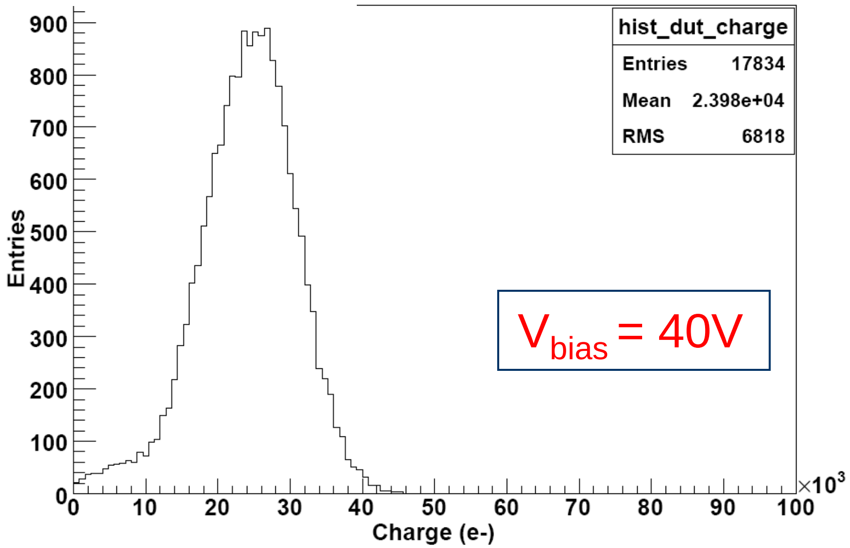
- ADC to electron conversion:
  Vcal^{*} [DAC] = ADC x gain - offset
  Charge (e-) = Vcal x 65.5 – 410

  * 1 Vcal [DAC] = 65.5 electrons

- T ≈ 11 °C on carbon fiber (estimated to be 6 °C higher on the sensor)







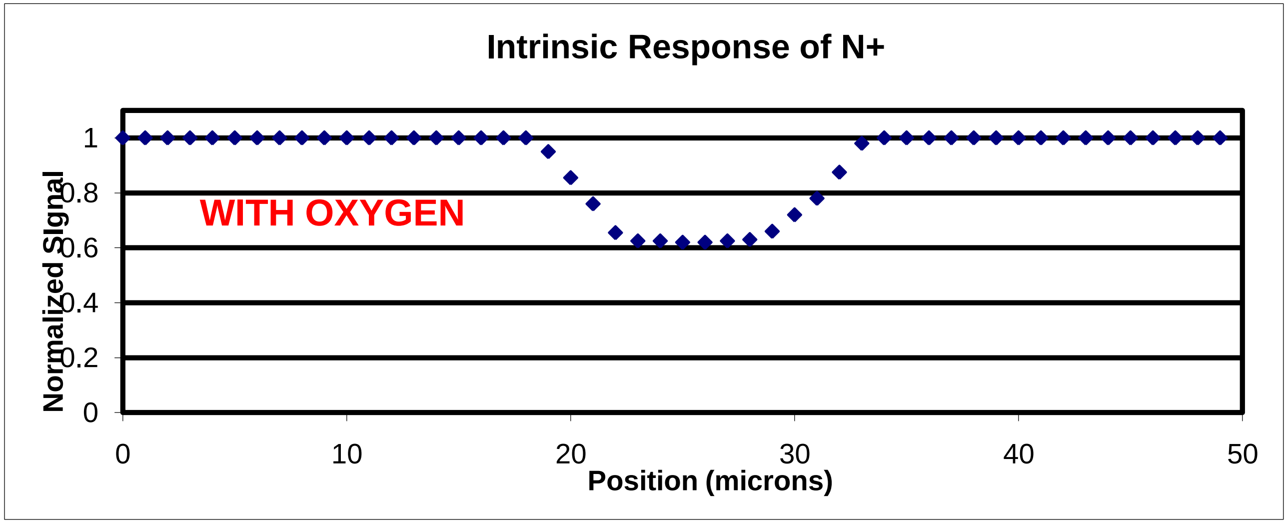
V_{bias} = 40V

X-RAY STUDIES OF ELECTRODE RESPONSE

Data showing the response of electrodes using to a 2 um wide X-ray beam

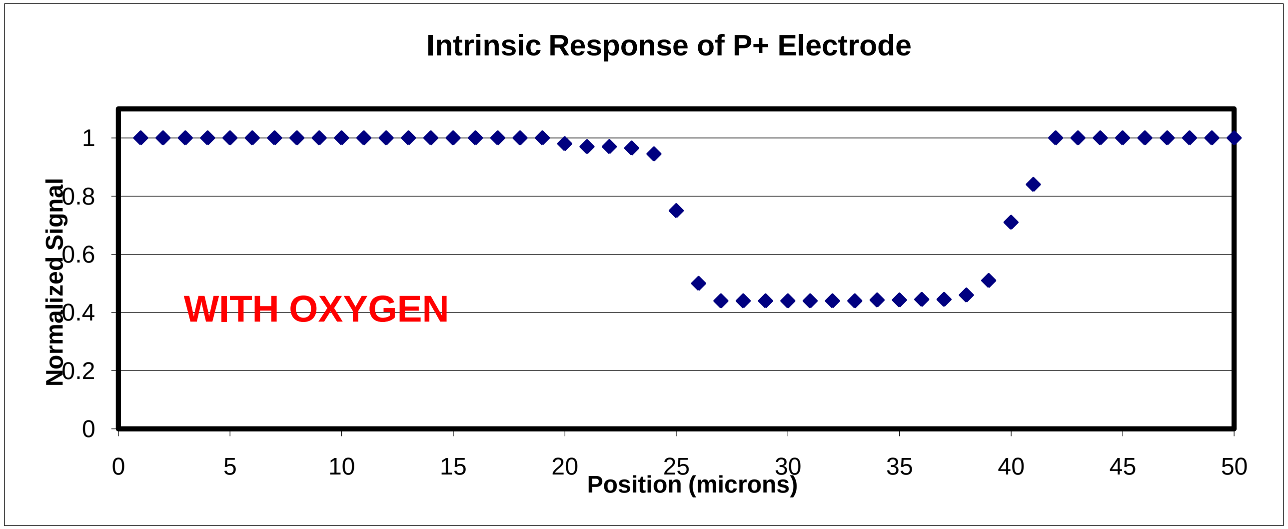
N+ electrode efficiency about 60%

POCL3



P+ electrode efficiency about 42%

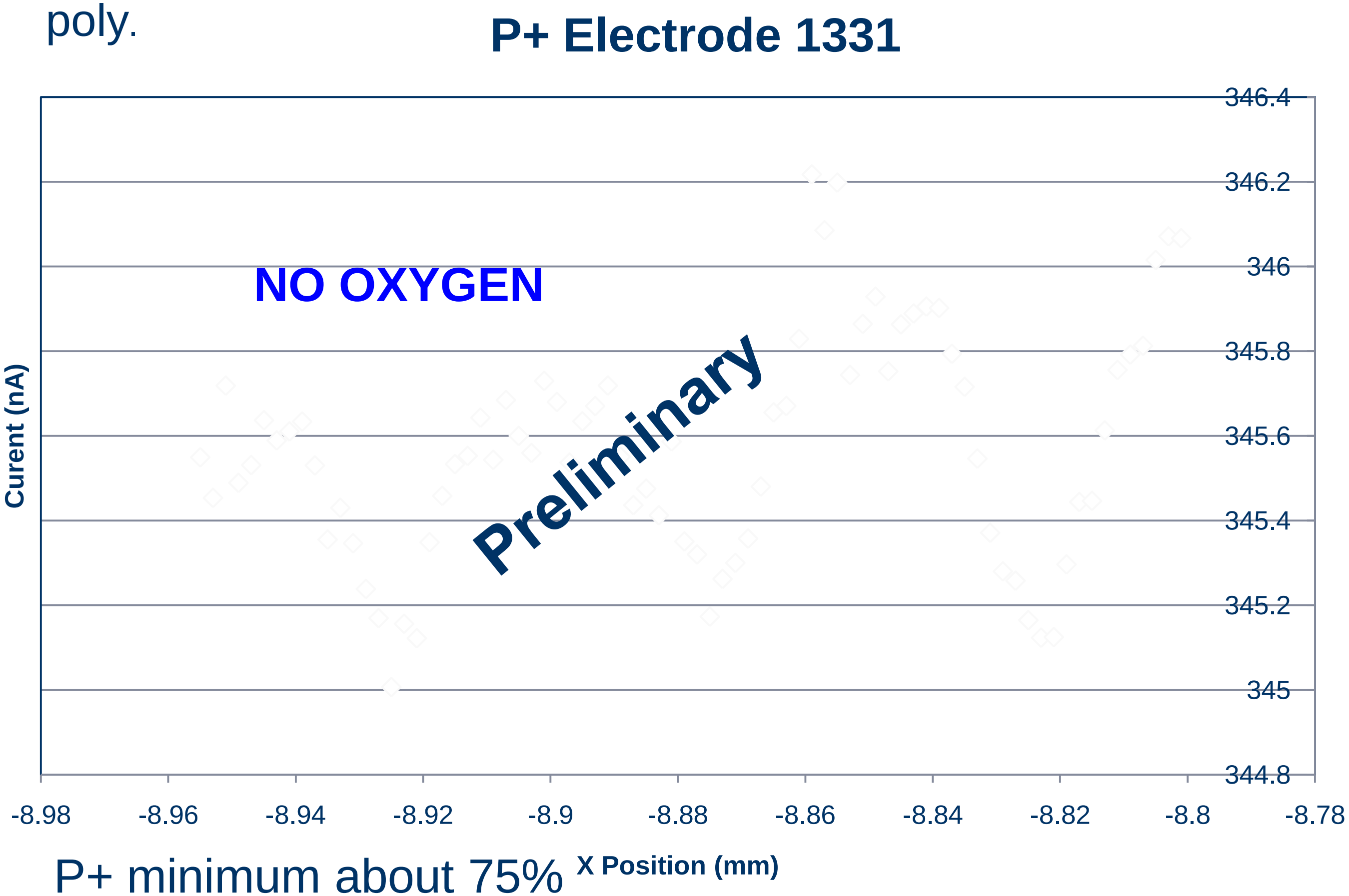
BBr3 + O2

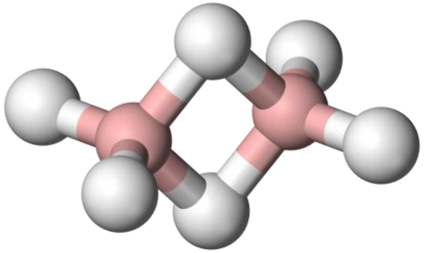


*** C. Kenney, J. Hasi (SLAC)**

P+ Electrode Signal (Diborane)

Data showing the electrode response of a Sintef device filled with diborane-doped poly.





Replace BBr5/O2 with B_2H_6

P+ minimum about 75%

Uncertainties are at least +/-10%

Need to deconvolve the beam shape

*** C. Kenney, J. Hasi (SLAC)**

Summary

- **On wafer level**
  - **IV measurements at SINTEF show increase of leakage current with increasing number of electrodes per pixel**
  - **CMS results consistent with SINTEF measurements (2Es have better IVs)**
  - **4E has the lowest yield**
  - **Good devices are located mostly in the centre of wafers**
  - **Overall yield about 35%**

- **Degradation after bump bonding**
  - **Some studies show copper contamination might be the culprit**
  - **Other tests show it is inconclusive**
  - **Dicing also seems to degrade the performance of detectors**
  - **Surface related issues?**

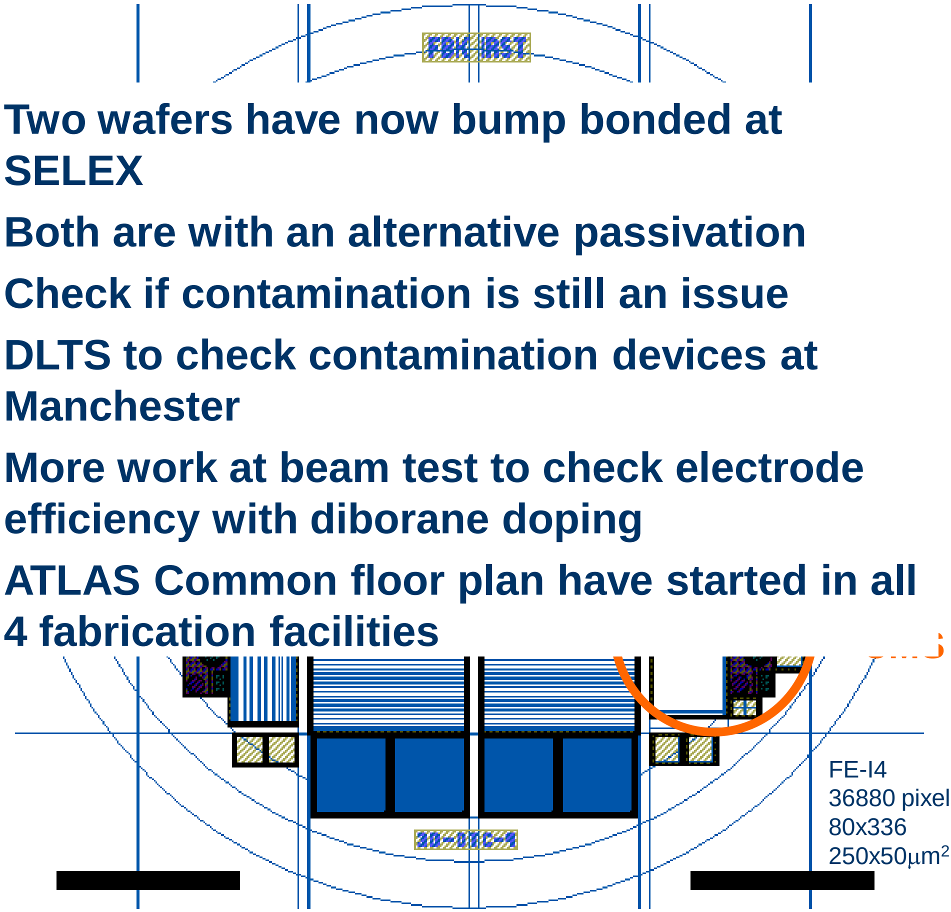
- Testbeam at FNAL with 120 GeV protons (CMS):
  - 2E devices have good performance
  - Noise level too high for 4E devices

The ATLAS 3D R&D Collaboration

Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors with Extreme Radiation Hardness

Approved in July 2007

Design by GF Dalla Betta, C. Kenney, A. Kok, G Pellegrini

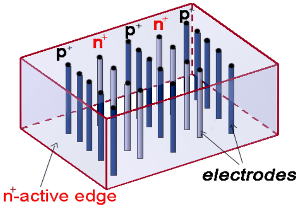


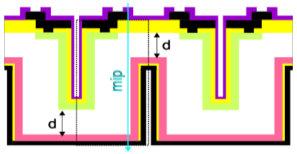
- **Two wafers have now bump bonded at SELEX**
- **Both are with an alternative passivation**
- **Check if contamination is still an issue**
- **DLTS to check contamination devices at Manchester**
- **More work at beam test to check electrode efficiency with diborane doping**
- **ATLAS Common floor plan have started in all 4 fabrication facilities**

FE-I4
36880 pixels
80x336
250x50μm^2

VTT Finland joined

Both CNM and FBK are now moving to through wafer electrodes





3D-DDTC

- 8 x FE-I4
- 9 x FE-I3
- Other test structures
- FZ p-type silicon
- 230μm thick

- 120 wafers x 8 = 960 FE-I4 of which:
- 480 full 3D with active Edges
- 320 double sides with slim fences and : 1080 x FE-I3