The Via Revolution

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Vertex 2010
Loch Lomond, Scotland
June 7-11
Introduction

• A revolution has started in the electronics industry. The revolution is due to the acceptance of through silicon vias (TSVs) in wafers as a new technology to replace transistor scaling as a means of improving circuit performance. With this new feature every integrated circuit can be considered to be a two sided device where connections can be made to the top and bottom or just the bottom of a chip. This leads to 3D integrated circuits with multiple levels of transistors and increased routing levels.

• The adoption of TSV techniques also allows for more flexible packaging such as WLP (Wafer Level Packaging) and SiIP (Silicon Interposers).

• This talk will give an overview of TSV technologies along with how and where TSVs are used.
Some Basic TSV Information

- TSV ranges in size from 1-100 μm in diameter and are filled or plated with a conductive material.
- TSVs are primarily used as an electrical connection or a heat conductor.
- A TSV is a critical part of the 3D integration process.
- TSVs are used in:
  - 3D wafer level packages
  - 3D silicon interposers
  - 3D integrated circuits
  - These applications will be discussed later
- “3D packaged” parts that do not use TSVs are NOT considered 3D integration
TSV Hole Fabrication Techniques

- **Etching**
  - Deep Reactive Ion Etch (DRIE) is used to etch holes in silicon.
    - The most widely used method for forming holes in silicon.
    - The process tends to form scalloped holes but can be tuned to give smooth walls.
    - Small diameter holes (1 um) and very high aspect ratio (100:1) holes are possible.
  - Plasma oxide etch is used to form small diameter holes in SOI processes. This process used by MIT LL.
    - Since the hole is in an insulating material, it does not require passivation before filling with conducting material.
  - Wet etching
    - KOH silicon etch give 54.7° wall angle

- **Laser Drilling**
  - Used to form larger holes (> 10 um)
  - Can be used to drill thru bond pads and underlining silicon with 7:1 AR
  - Toshiba and Samsung have used laser holes for CMOS imagers and stacked memory devices starting in 2006.
DRIE for Through Silicon Vias

- Holes are formed by rapidly alternating etches with SF$_6$ and passivation with C$_4$F$_8$
- Any size hole is possible (0.1 - 800 um)
- Etch rate is sensitive to hole depth and AR (aspect ratio).
DRIE Via Shapes and Passivation

- **Via shapes**
  - **Annular vias** - provide larger conducting volume and reduced thermal stress near vias
  - **Trenches** - used to provide high current capacity to device backside, available in IBM 0.35 um BICMOS
  - **Cylindrical** - has steep side walls (89°)
  - **Tapered** - Has angled side walls to allow easier plating or filling of via
  - **Combinations** of the above

- **Vias in CMOS must have passivated walls (often BCB or PECVD)** before filling to avoid shorts.

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Annular and trench vias from IBM

Cross section of cylindrical, tapered, and combination vias using DRIE
Via Fill Materials and Fill Factor

- **Common via fill materials**
  - **Electroplated Copper**
    - Preferred by many but has serious TCE mismatch with silicon leading to oxide cracking
    - Can fill larger vias
  - **CVD Tungsten**
    - Excellent TCE match to silicon but only used for small diameter vias.
    - Has thermal conductivity similar to Si
  - **Polysilicon** - used less often

- **Fill factor**
  - Larger holes generally have plated walls (easier integration)
  - Smaller holes generally filled (more complex process)

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity (W/m/K)</th>
<th>Thermal Coefficient (ppm/K)</th>
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<tbody>
<tr>
<td>Silicon</td>
<td>149</td>
<td>2.6</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>1.4</td>
<td>0.5</td>
</tr>
<tr>
<td>Copper</td>
<td>410</td>
<td>16.5</td>
</tr>
<tr>
<td>Tungsten</td>
<td>170</td>
<td>4.5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>235</td>
<td>23.1</td>
</tr>
</tbody>
</table>

Oxide fracture due to “copper pumping” - R. Patti, Tezzaron

Plated side wall via and filled via

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An Interesting Look Back at Some Silicon Wafer Via History

- In 1975, a GaAs IC used a via for backside grounding.
- More than 10 years ago, backside illuminated CCDs were fabricated by thinning the CCD and opening a long trench behind the normal bond pads to allow wire bonding from the back side of the die.
- In 2005 the technology was applied in HEP to a MAPS device wherein separate openings were made behind each bond pad to allow for wire bonding from the backside and thus allow backside illumination (BSI).
- More recently, all Medipix3 I/O signals have TSV landing pads in place for back side wire bonding to allow backside illumination.
3D Integration Platforms with TSVs

- **3D wafer level packaging**
  - Backside contact allows stacking of chips
  - Low cost
  - Small package

- **3D Silicon Interposers (2.5D)**
  - Built on blank silicon wafers
  - Provides pitch bridge between IC and substrate
  - Can integrate passives

- **3D Integrated circuits**
  - Opens door to multilevel high density vertical integration
  - Shortest interconnect paths
  - Thermal management issues

![3D Wafer level package](image1)

![3D Silicon interposer](image2)

![MIT LL 3D integrated APD Pixel Circuit](image3)

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Vias Used in 3D Integration

- Three different types of vias are used in 3D integration
  - Blind TSV - (via first or middle)
  - Full TSV - (via last)
  - Backside TSV - (via last)

- TSVs can be implemented at three different stages in the IC fabrication process.
  - Via first - before FEOL (Front end of line/transistor formation) processing
    - Small vias
  - Via middle - After FEOL and before BEOL (Back End Of Line/metalization) processing
    - Small vias
  - Via last - After BEOL processing
    - Generally large vias
    - Via last technique often requires space on all metal layers.
    - Very bad for high density designs

Example of three different types of vias used in 3D integration
Common TSV Processing Options

Via First

1) Before FEOL:

FEOL | Etch | Fill | FEOL+BEOL | Thinning | Bonding

2) After FEOL:

FEOL + BEOL | Etch | Fill | Thinning | Bonding

Via Middle

3) Before bonding:

FEOL + BEOL | Bonding | Thinning | Etch | Fill

Via last

4) After bonding:

FEOL + BEOL | Bonding | Thinning | Etch | Fill
3D Wafer Level Packaging

- WLP is used for CMOS image sensor (CIS)
  - Via formed after BEOL processing
  - Via goes from backside to metal 1
  - Permits smaller packages
  - Provides increased performance
  - Low cost package
- HEP devices can also benefit from WLP.
3D Interposers

- Silicon interposers have become known as 2.5D integration because there are TSVs in the silicon interposer.
  - Use full through wafer via
  - Allows fine pitch interconnections between die.
  - Good CTE match between chips and substrate
  - May have multiple levels of interconnection on interposer
- Beginning to become available from different sources
• Allvia\textsuperscript{12}
  - Allvia focuses on 2 types of via technologies
    - Via first, blind filled via, front side TVS
    - Via Last, plated via, back side via
  - Also does full TSVs for SiIP
  - Via dia 30-150 um
  - AR = 5 max
  - Integrated caps up to 1.5 uf/cm\textsuperscript{2} for power filtering.
  - Top and bottom routing layers (2-5 mil lines and spaces)
• RTI\textsuperscript{6}
  - Multilevel metal layers
  - TSVs from backside
  - Passive device layer
• IPDIA\textsuperscript{13}
  - SiIP MPW Jan & June 2010
  - Integrated passive devices

<table>
<thead>
<tr>
<th>Thickness</th>
<th>300 ( \mu )</th>
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<tbody>
<tr>
<td>Via diameter</td>
<td>75 ( \mu )</td>
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<tr>
<td>Via filling</td>
<td>Copper</td>
</tr>
<tr>
<td>Via resistivity</td>
<td>&lt; 10 mOhms</td>
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<tr>
<td>IPD generation</td>
<td>PICS2</td>
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**IPDIA Si Interposer MPW run**
The TSV technology has been proposed for use in CMS to locally identify high pt tracks and thus minimize data transfer.

This can be done by having two layers of sensors separated by an interposer of modest thickness (~1 mm).

Signals would pass from the top sensor through the interposer to a ROIC which processes signals from the top and bottom sensors to look for steep tracks.

A 3D track trigger demonstrator chip called VICTR is now at the foundry.
3D Integrated Circuits

- 3D integrated circuits have 2 or more layers of thinned circuits that are bonded together and interconnected to form a multilayer monolithic device.
- Allows integration of wafers from different semiconductor processes
- Vias are needed to provide interconnection between tiers or connections to the top or bottom of the assembled 3D stack.
- Vias allow performance improvements due to shorter traces between functional blocks and lower overall mass.
- Yole says that at least 15 companies now have TSV research programs or pilot production.

256 x 256 Infrared Pixel Array
Austria Microsystem TVS Process

- The TSV process is available on every 0.35 um CMOS MPW run in 2010 - full through wafer via
- Via Last process from top side (must leave space on all routing layers for via).
- Applications
  - Mating ROIC to photo diode sensor
  - Mating 2 tiers of CMOS or BiCMOS
  - Also can be used for WLP with backside contact and routing
- Two tiers bonded with low temperature oxide bond
- TSV specs
  - Diameter = 100 um
  - Depth = 250 um (wafer thickness)
  - Min via pitch = 400 um
  - Plated vias (not filled)
  - Max TSV current = 100 ma

Example showing via from ROIC to sensor

AMS via cross section
MIT LL 3D Vertical Integration Process

- MIT LL uses a via last process on their SOI wafers
- Space must be left on all metal layers for via insertion
- An oxide bond is used to mate wafers.

Step 1: Fabricate individual SOI tiers (FEOL + BEOL)

Note: Wafer 1 can be SOI or bulk

Step 2: invert, align, and bond wafer 2 to wafer 1 using an oxide bond

Step 3: remove handle silicon from wafer 2, etch vias, deposit and CMP tungsten. (The BOX acts as an etch stop when removing the handle silicon.)

Note: additional tiers can be stacked by using a face to back configuration on top of wafer 2
MIT LL Vias in 3 Tier IC

- **Features**
  - Small vias in 180 nm fully depleted SOI process
  - Stacked vias
  - Offered on three MPW runs for DARPA

Cross section of 3 tier IC showing 3D vias between tiers
Tezzaron 3D Process

- Uses via middle process in Chartered CMOS process
- 6um blind tungsten vias are inserted after FEOL and before BEOL processing

Assume identical wafers
Flip 2nd wafer on top of second wafer
Bond 2nd wafer to 1st wafer using Cu-Cu thermocompression bond

Thin 2nd wafer to about 12um to expose super via
Add metallization to back of 2nd wafer for bump or wire bond

Additional wafers can be stacked face to back on top of 2nd wafer

After FEOL fabricate 6 um super contact (via)
Complete BEOL processing
HEP Multiproject Run Using Tezzaron’s Via Middle Technology

- Consortium of 15 institutions from 5 countries was formed to explore 3D IC design and to use the Tezzaron via middle process in an MPW run for HEP designs
  - Process used the Chartered 0.13 um CMOS process
  - Two tiers with a single mask set
  - More than 20 designs included
  - Details presented in talk by Gianluca Traversi

- Fermilab designs:
  - H: VICTR - pixel readout chip mating to two sensors for track trigger in CMS
  - I: VIP2b - ILC pixel chip with time stamping and sparcification
  - J: VIPIC - fast frame readout chip for X-ray Photon Correlation Spectroscopy at a light source
  - TX and TY - test chips
Consortium future

• Consortium awaiting return of 2D and 3D wafers from first MPW run.
• New consortium members have been added and space for the next MPW run is fully booked.
• MOSIS/CPM/CMC have entered into an arrangement with Tezzaron to offer 3D IC runs using the Chartered 0.13 um process
  – Development and organization of tools is being lead by CPM with support from CMC
    • Adding 3D LVS
    • Fill subroutines
    • Libraries
    • Etc
  – MOSIS will act as direct interface to Tezzaron, and organize the MPW frame for submission
  – The new tool set is expected by the end of the June
• It is anticipated that the consortium will use the services of MOSIS/CMP/CMC for future runs.
• The consortium will continue to provide a venue to discuss design issues and compare test results.
TSVs in Unusual Places

- **3D Pixel Sensors**\(^\text{17}\)
  - Small diameter blind vias are formed using DRIE
  - Top vias are n+, bottom vias are p+
  - Sensors suitable for bump bonding or 3D integration with ROIC

- **TSVs for cooling**\(^\text{10}\)
  - Micro channel fabricated in SiIP by direct bonding of silicon to silicon.

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Micro channel vias for interposer cooling

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In the Future??

Cooling channels can be imbedded directly in a 3D IC for heat removal\textsuperscript{18}

Micro channels become horizontal TSVs when placed between layers of a 3D IC.

Study underway at Ecole Polytechnique Federale de Lausanne
Summary

• TSVs have been used in integrated circuits for some time. Recently, however, a via revolution has developed since it is now recognized that TSVs provide a viable means to extend the performance improvements associated with Moore’s Law by building 3D integrated circuits.

• As a side benefit, wafer level packaging and silicon interposers are using via technologies to offer packaging options here-to-fore not readily available. Vias and 3D integration are here to stay and should find applications in HEP whether it is via first, via middle, or via last.

• HEP should be ready to embrace the via revolution and the benefits it will bring.
References

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17) G. Pellegrini, et. al., First double-sided 3D detectors fabricated at CNM-IMB, NIM 2008.