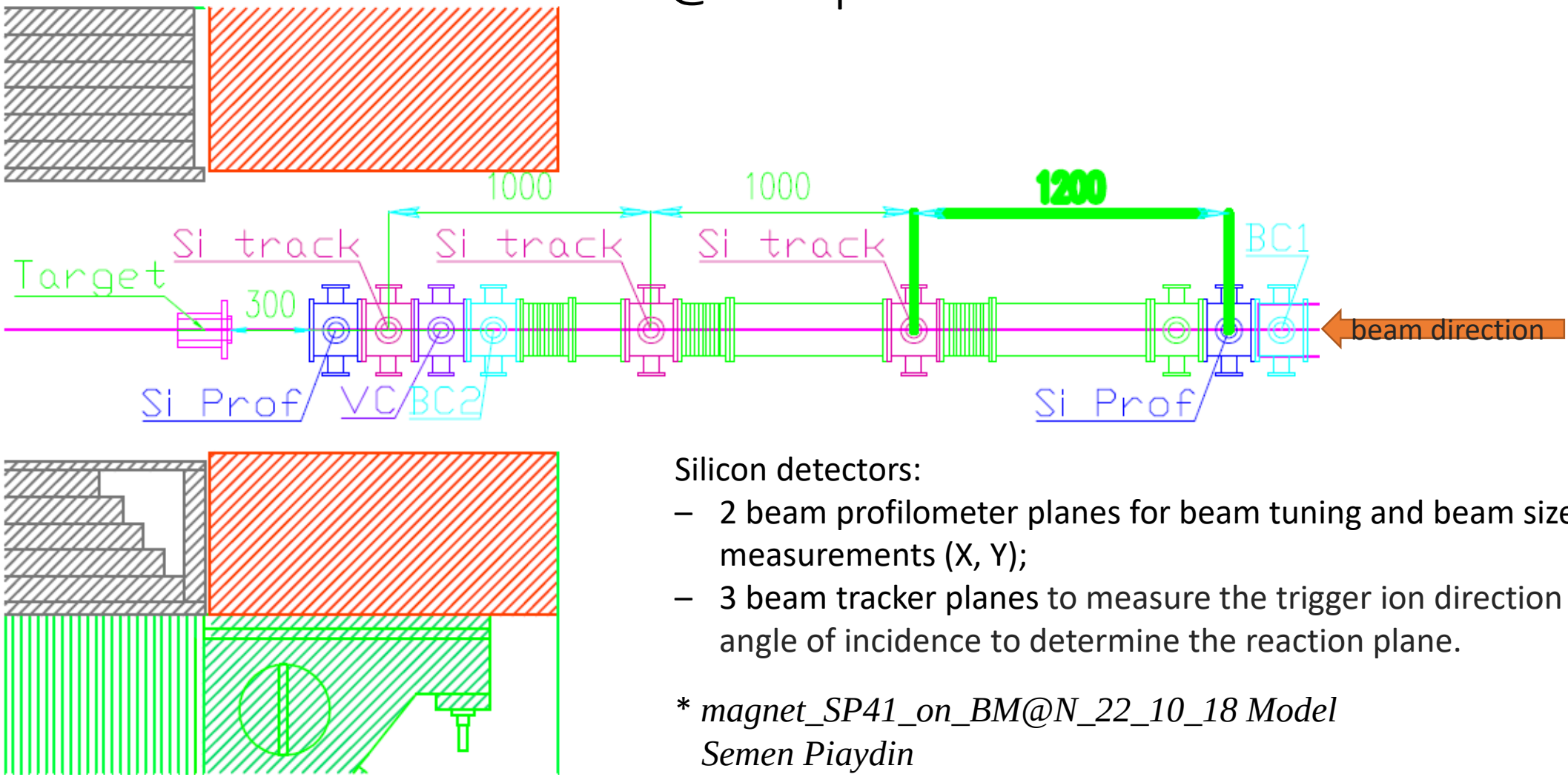
The development of Silicon beam tracker and beam profilometer at the BM@N experiment

***Yu. Ivanova*, S. Khabarov, Yu. Kopylov, E. Streletskaya, O. Tarasov, B. Topko, N. Zamyatin, E. Zubarev**

LXX International conference NUCLEUS-2020

13 October 2020

Silicon detectors upstream of the target at BM@N experiment



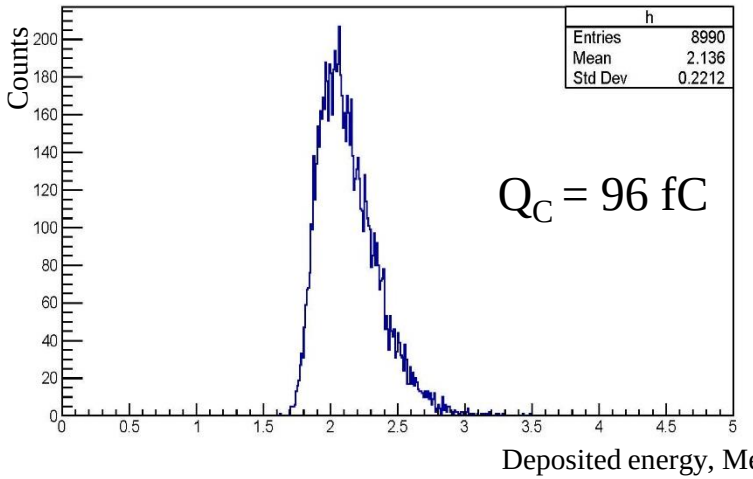
Silicon detectors:

- 2 beam profilometer planes for beam tuning and beam size measurements (X, Y);
- 3 beam tracker planes to measure the trigger ion direction and angle of incidence to determine the reaction plane.

* *magnet_SP41_on_BM@N_22_10_18 Model*
Semen Piaydin

Simulation of deposited energy in 175 µm silicon

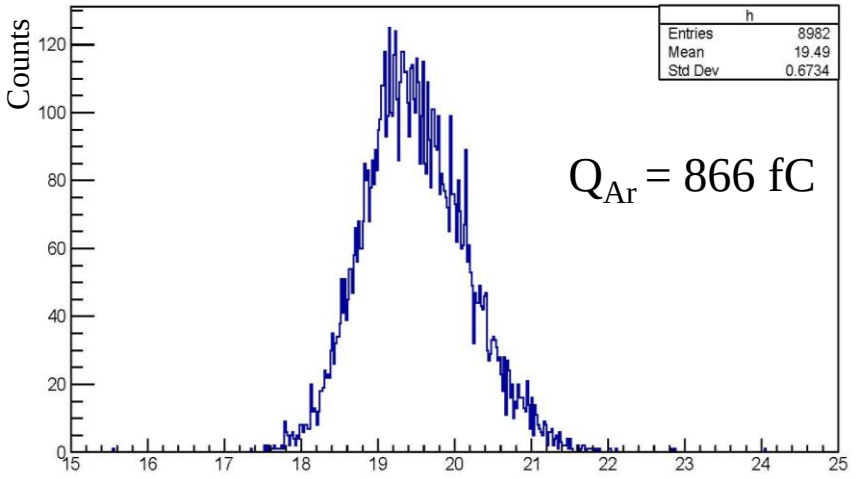
Carbon 4 AGeV ions deposited energy



Q_C = 96 fC

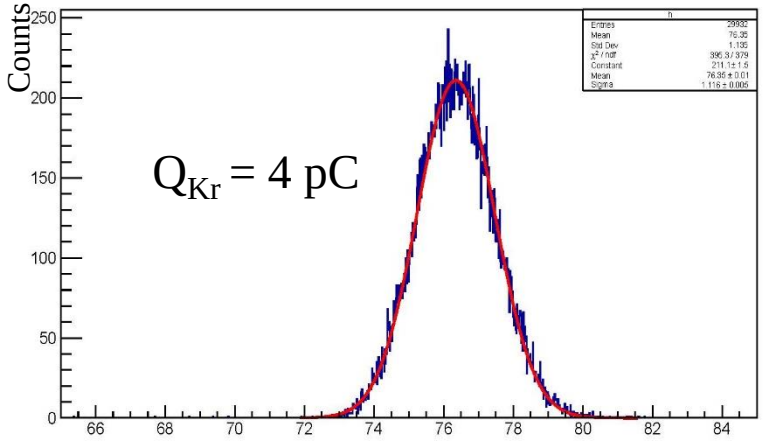
VA163 (IDEAS) as FEE ASICs for *light ions*

Argon 4 AGeV ions deposited energy



Q_{Ar} = 866 fC

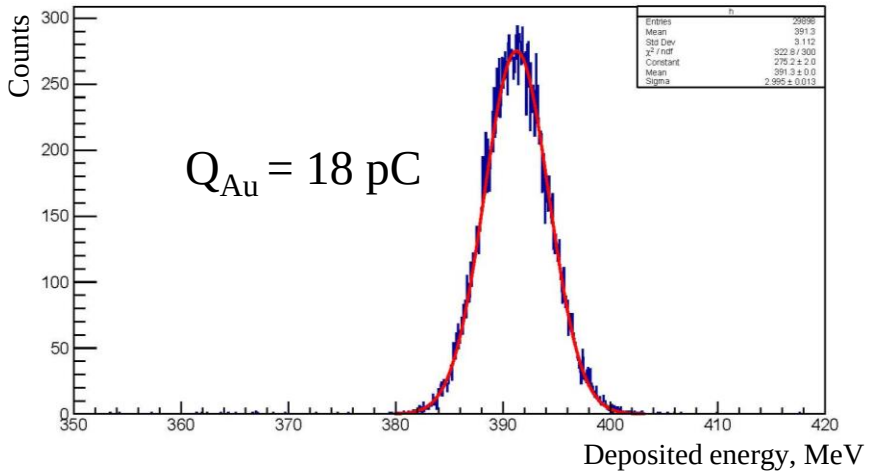
Krypton 4 AGeV ions deposited energy



Q_{Kr} = 4 pC

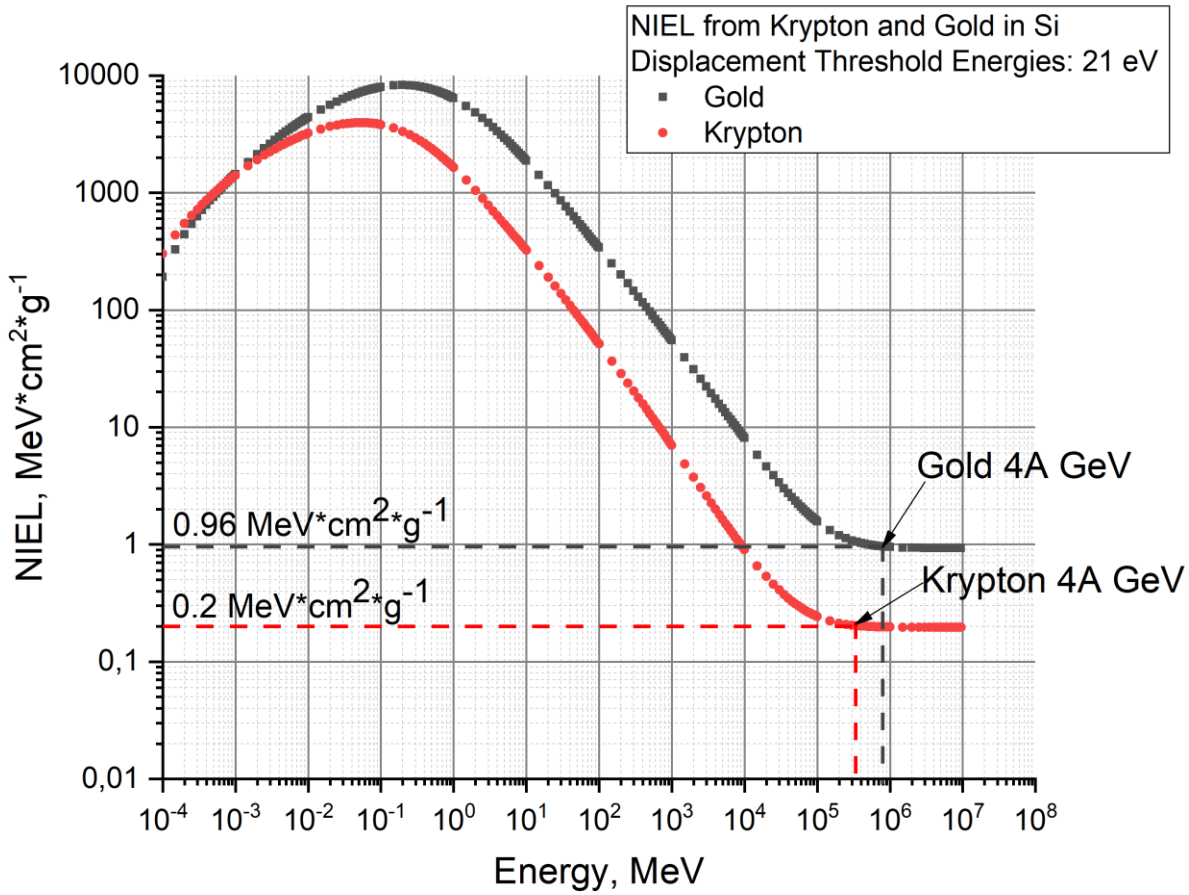
VA32HDR11, VATA64HDR16.2 for *heavy ions*

Gold 4 AGeV ions deposited energy



Q_{Au} = 18 pC

Expected radiation damage of beam tracker



SR-NIEL modeling results of NIEL in silicon detector for Kr^{36+} (red) and Au^{79+} (black) ions.

NIEL from 1 MeV neutron in Si (ASTM Standard E722-09):
NIELn=0.00204 MeV*cm^2* g^{-1}
Hardness factor of 4A GeV Gold: NIELgold/NIELn≈470;
Hardness factor of 4A GeV Krypton: NIELkrypton/NIELn≈98;

Radiation conditions in beam tracker positions:
Beam diameter: d=3 cm (~ 64 strips for each side in beam zone)
Flux of ^{197}Au: F=10^6 nucl./sec;
Time of irradiation: t=2 months;
$NIEL_{Au}(4\ GeV/nucl)$=$9.6107 \cdot 10^{-1}\ MeV \cdot cm^2 \cdot g^{-1}$;

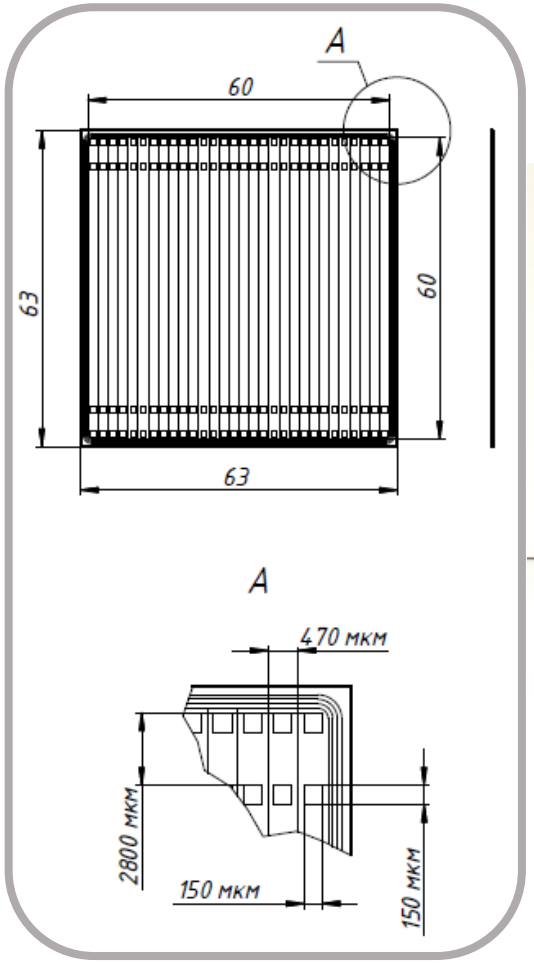
$$\Phi_{1MeV} = \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \Phi_{Au} = \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \frac{4 \cdot F \cdot t}{\pi \cdot d^2} \approx 3.45 \cdot 10^{14}\ cm^{-2}$$

Expected total dark current increase after 2 months at +20 Cº (without self annealing):

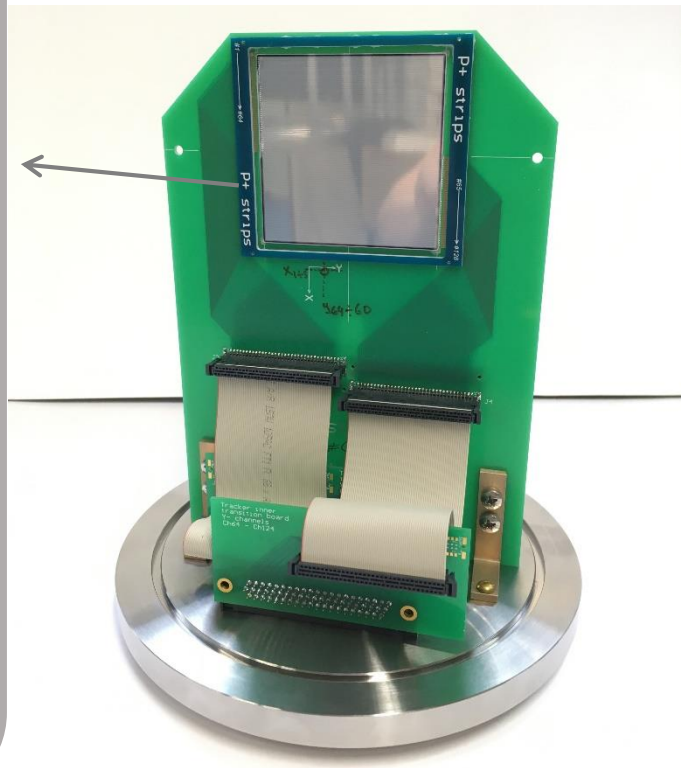
$$\Delta I = \alpha \cdot S_{beam} \cdot h_{detector} \cdot \Phi_{1MeV} = 5 \cdot 10^{-17} \cdot 7.07 \cdot 175 \cdot 10^{-4} \cdot 3.45 \cdot 10^{14} = 2.13\ mA$$

Expected dark current increase of 1 strip in beam zone: $\Delta I \approx 35\ \mu A$

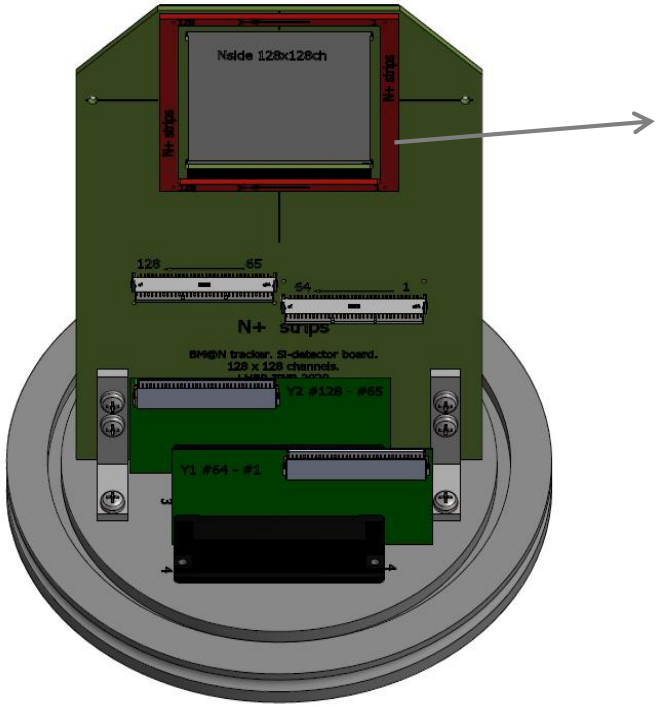
Beam tracker. Double-sided Silicon Detector (DSSD)

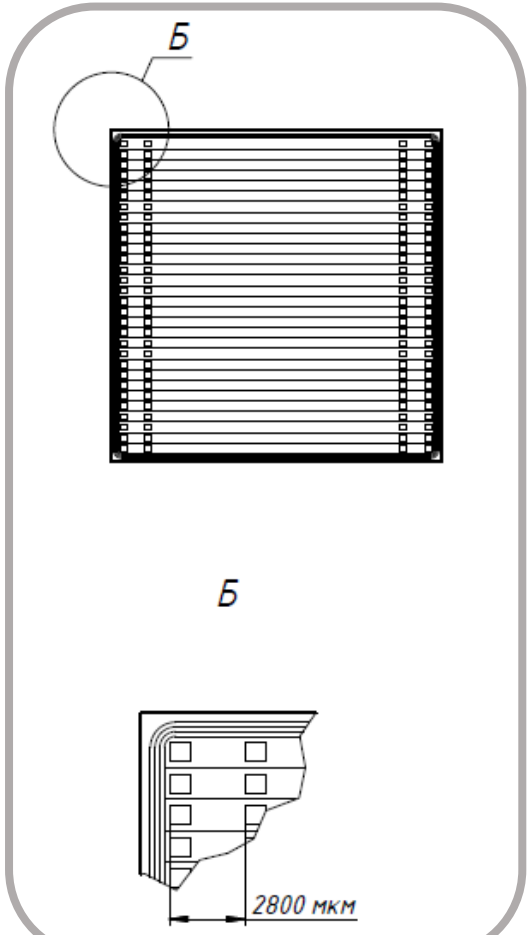


p+ side



n+ side



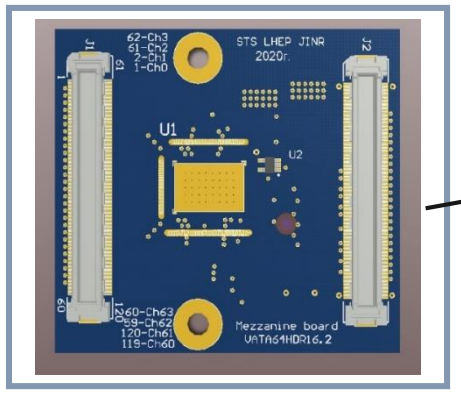


Size: 63x63x0,175 mm^3 (on 4” – FZ-Si wafers n-type, thickness 175 mkm);
Active area: 61x61 mm^2; Resistivity ~ 10 kOhm*cm;
Topology: double sided microstrip (DSSD) (DC coupling);
Pitch p+ / n+ strips: 470 µm; Stereo angle between p+/n+ strips: 90^0;
Number of strips: 128(p+)×128(n+).

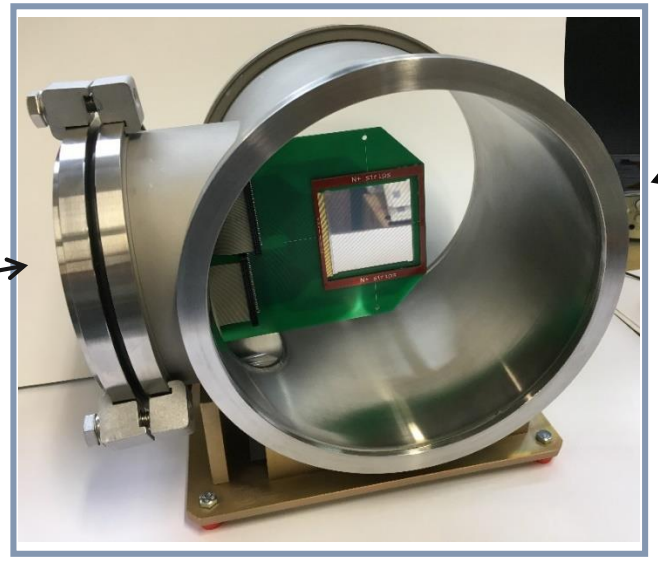
Beam tracker. FEE

Ions	Charge	IDEAS ASIC	ASIC channels	Dynamic range	Shaping time
light ($_{6}C$ – $_{18}Ar$)	96 - 866 fC	VA163 + TA32cg2	32	±750fC	500ns
Heavy ($_{36}Kr$ - $_{79}Au$)	4 - 18 pC	VATA64HDR 16.2	64	-20pC ÷ +55pC	50/100/150/ 300ns

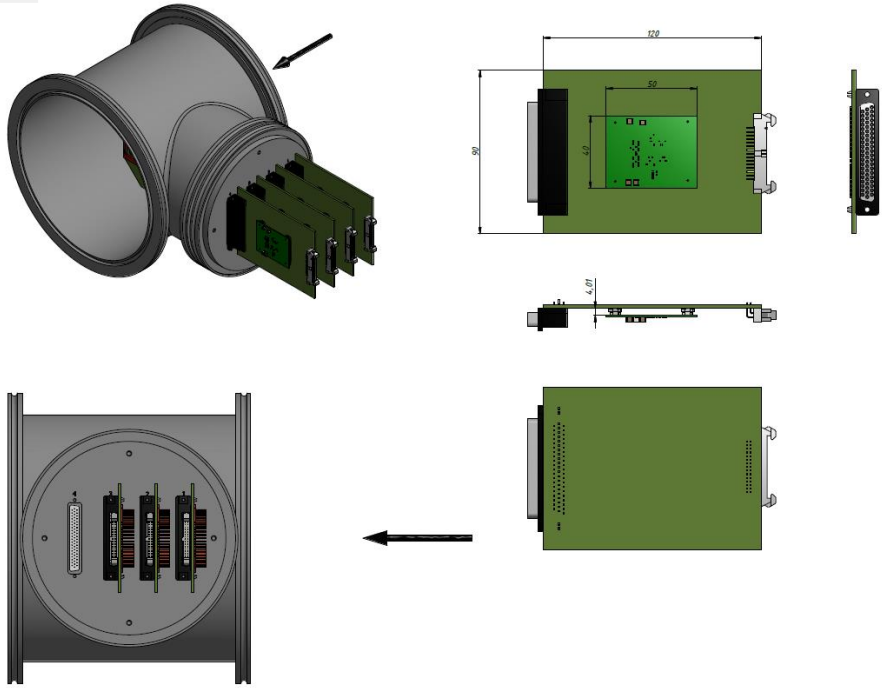
- silicon beam tracker is designed to determine the coordinates (X, Y) of incident “trigger ion”;
- self-trigger counter = ion beam flux/run.



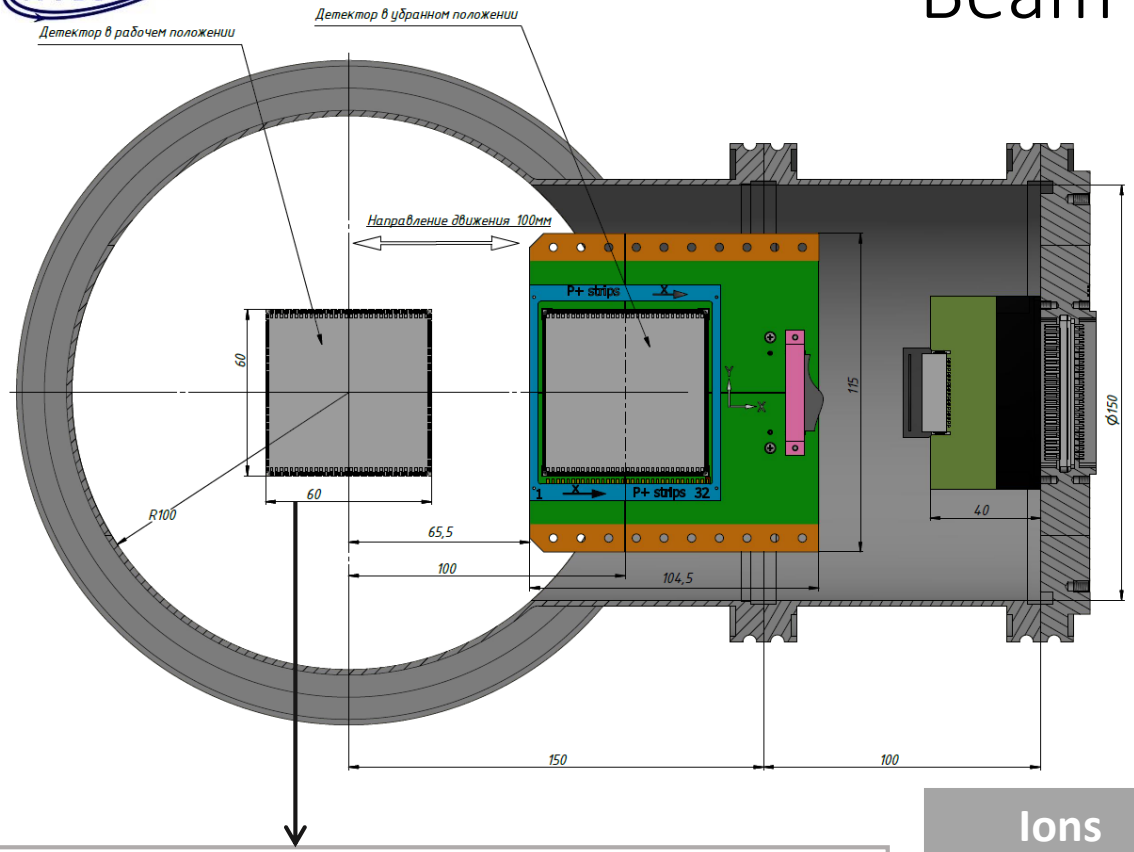
A PCB design of a mezzanine card with one VATA64HDR16.2



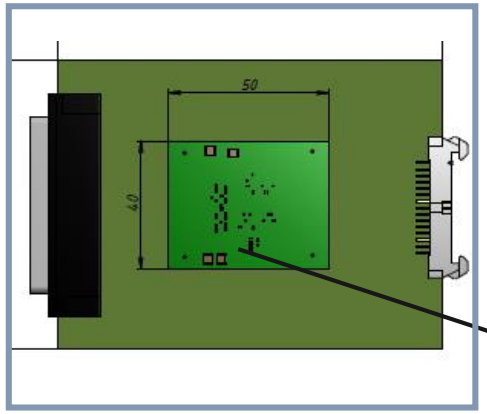
DSSD coordinate plane inside the beam pipe



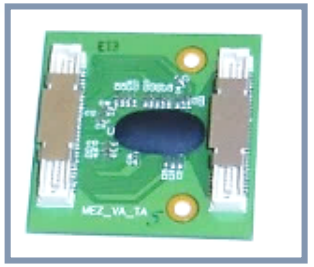
Beam profilometer



DSSD: Active area: 58x58 mm^2;
on 4” – FZ-Si wafers n-type, thickness 175µm;
Stereo angle between p+/n+ strips: 90^0;
Number of strips: 32(p+)×32(n+).



FEE boards on the outside of vacuum station flange

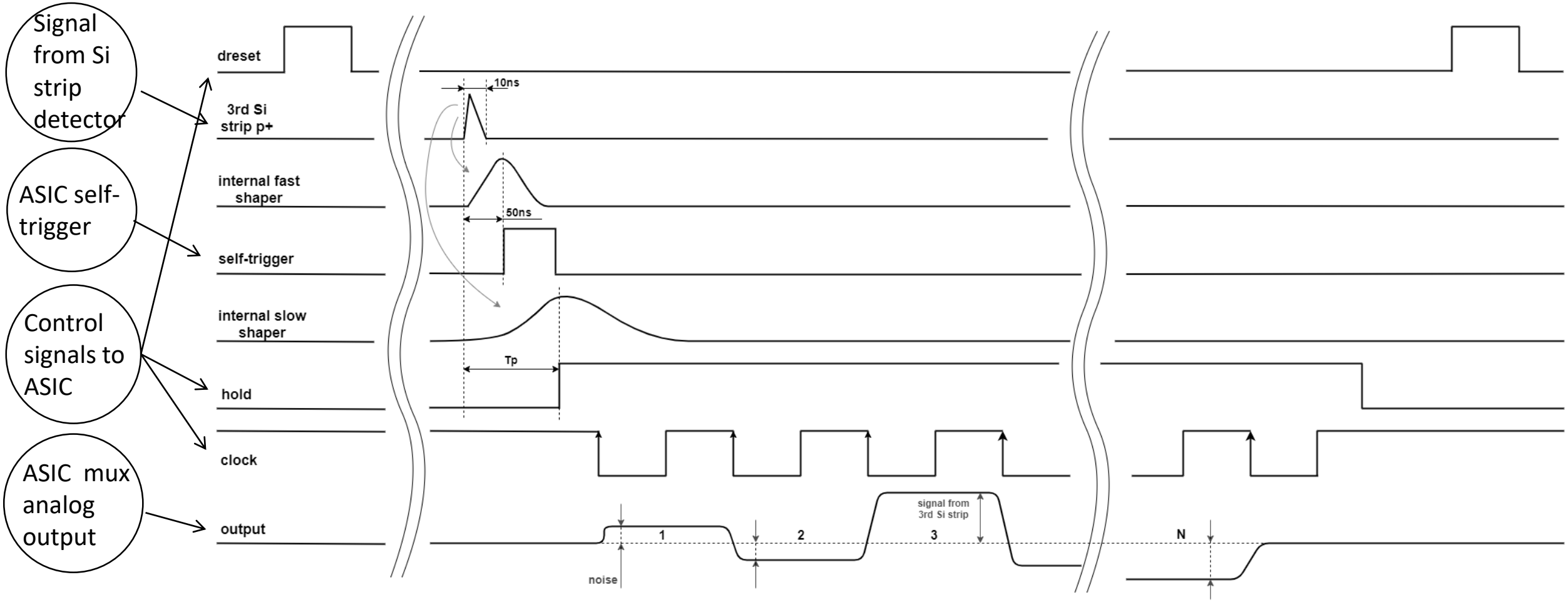


A mezzanine card with VA32HDR11+TA32cg2 or VA163+TA32cg2

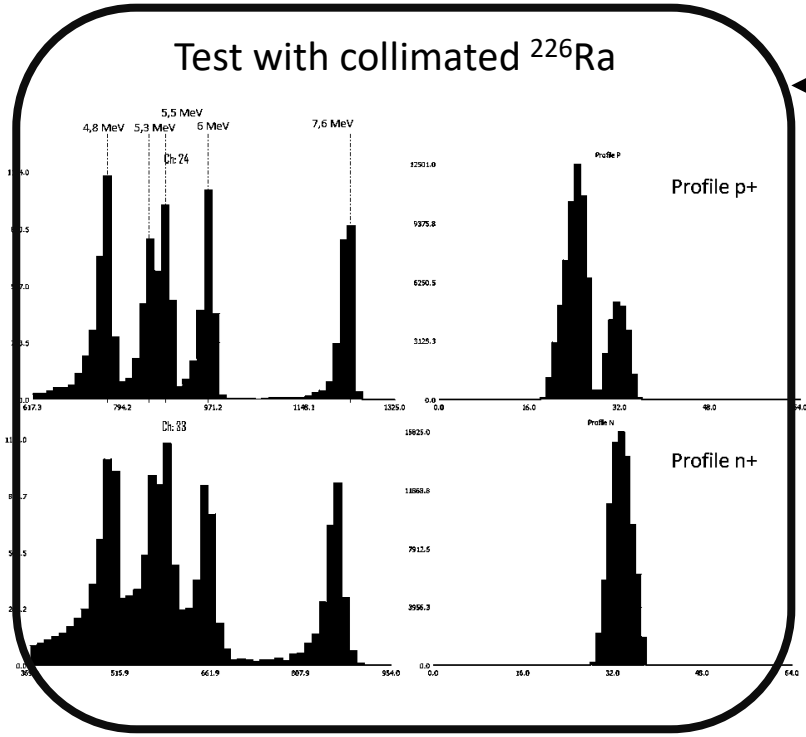
- silicon beam profilometer is designed to tune the beam;
- detector planes could be automatically removed from beam zone after tuning.

Ions	Charge	IDEAS ASIC	ASIC channels	Dynamic range	Shaping time
light ($_6$C – $_{18}$Ar)	96 - 866 fC	VA163 + TA32cg2	32	±750fC	500ns
Heavy ($_{36}$Kr - $_{79}$Au)	4 - 18 pC	VA32HDR11 + TA32cg2	32	-35pC ÷ +25pC	900ns

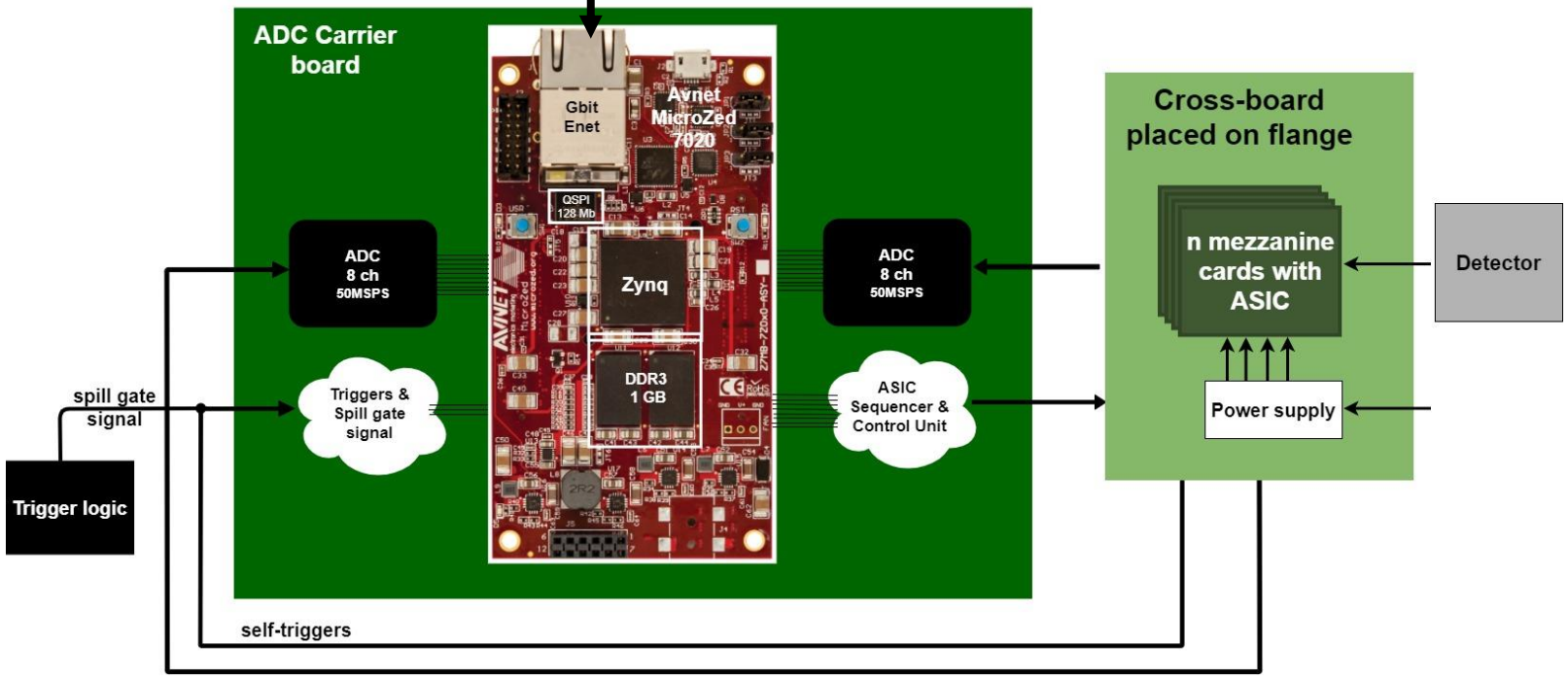
IDEAS ASIC readout diagram



Beam profilometer



Example of amplitude information and α-source profile from p+ and n+ strips of DSSD



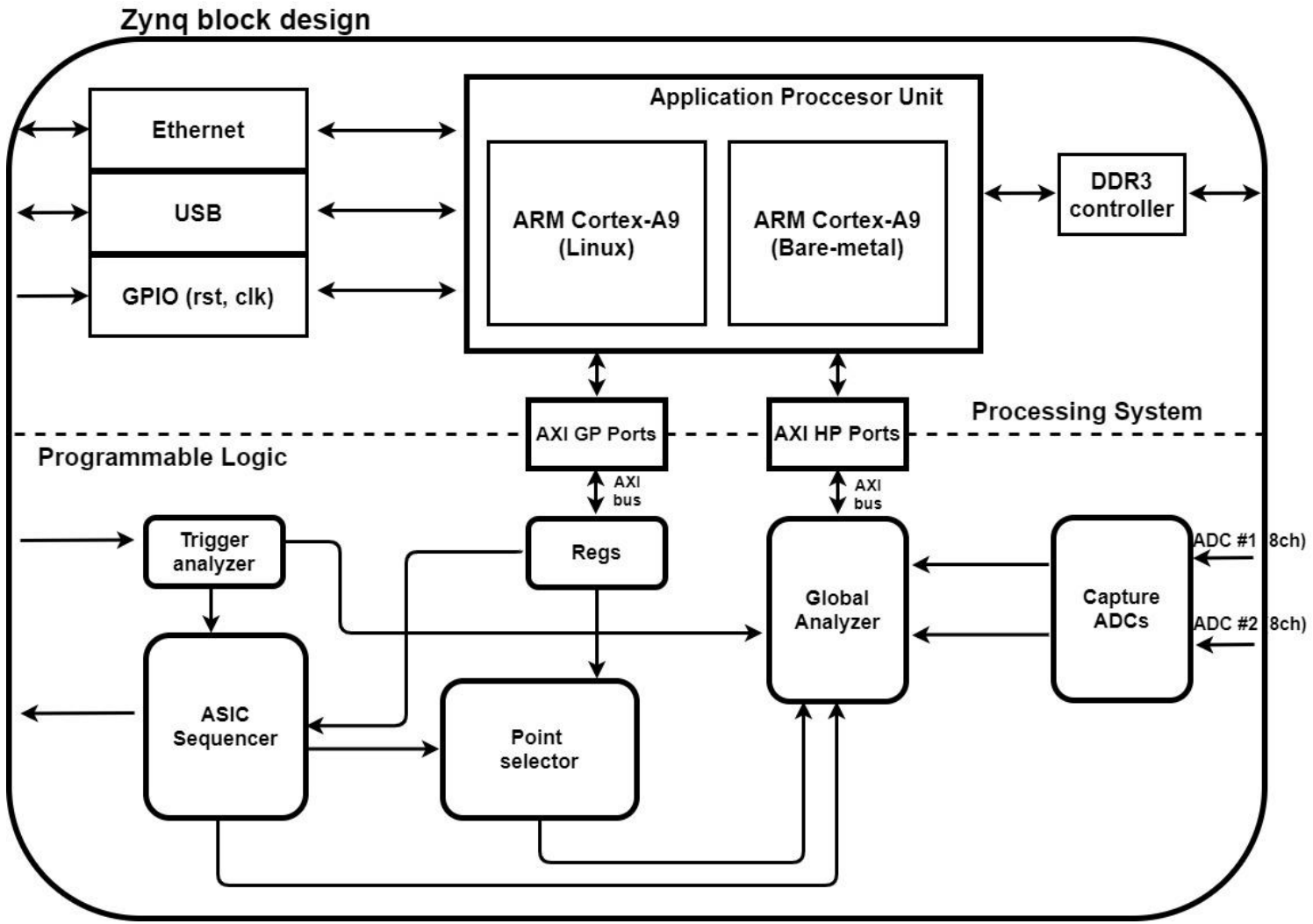
Autonomous measurement system for Silicon beam profilometer:

- based on Xilinx Zynq SoC;
- supports different mezzanine cards;
- 2 ADC (2x8channels) to digitize ASIC output data;
- display information.

Beam profilometer

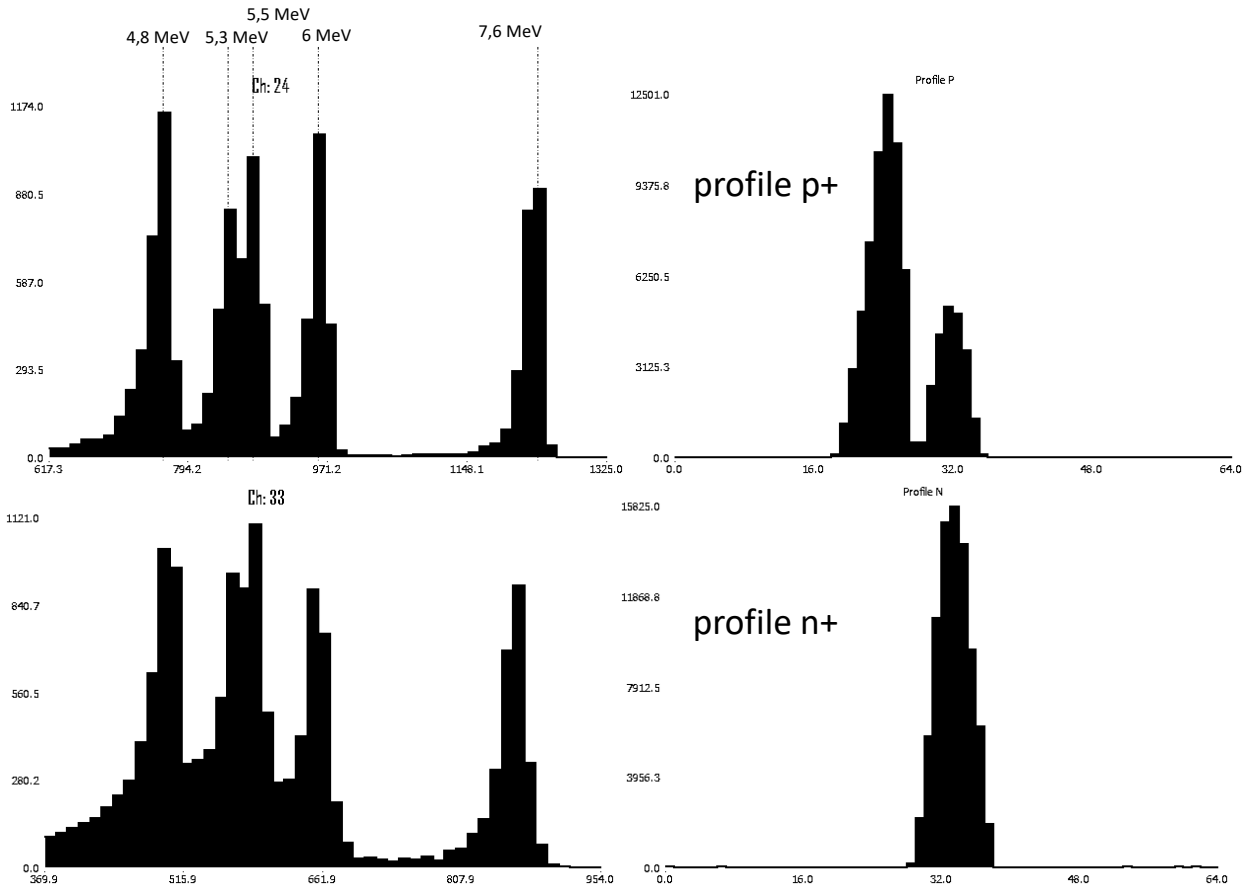
FPGA design of the ADC Carrier board:

- configure ASICs by external trigger;
- capture ADC data and analyze;
- pedestal subtraction and zero suppression;
- send via Ethernet.

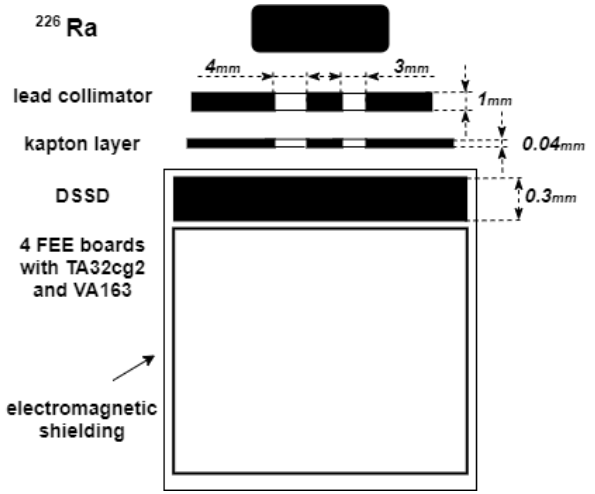


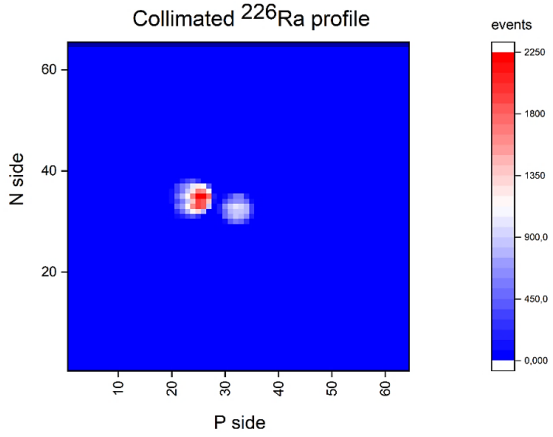
Beam profilometer prototype

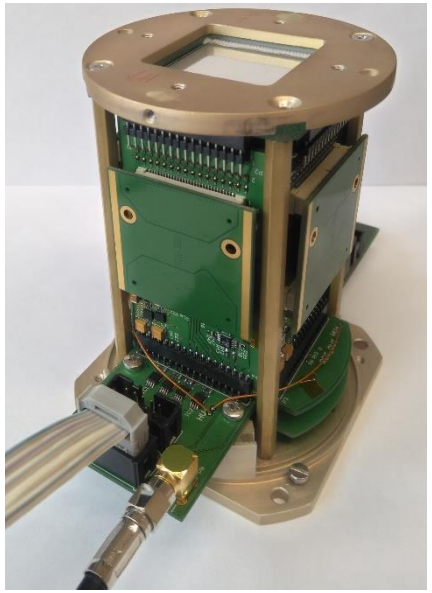
Test with collimated ^{226}Ra



Experimental setup (no vacuum)







beam profilometer prototype:

- DSSD with 300-µm, active area 32x32 mm^2, 64(p+)×64(n+) strips, 90^0 stereo angle between strips;
- FEE: VA163 and TA32cg2 ASICs.

Conclusion

For BM@N experiment (JINR, Dubna) development of coordinate planes based on Double-sided Silicon Detectors (DSSD) for next beam detectors are in progress:

- 3 beam tracker planes:
  - DSSD are based on planar technology thin (175 µm) 4” – FZ-Si wafers n-type conductivity;
  - FE boards on the outside of flange with two versions of ASICs - for light and heavy ions + DAQ-BM@N;
  - self-trigger counter for measuring of total ion beam flux/run.
- 2 beam profilometer planes:
  - 175 µm double-sided 32x32 strip detector;
  - FE boards on the outside of flange with two versions of ASICs - for light and heavy ions;
  - autonomous measurement system in self-trigger mode.