Plans / Ideas for the LHC BPM Upgrade

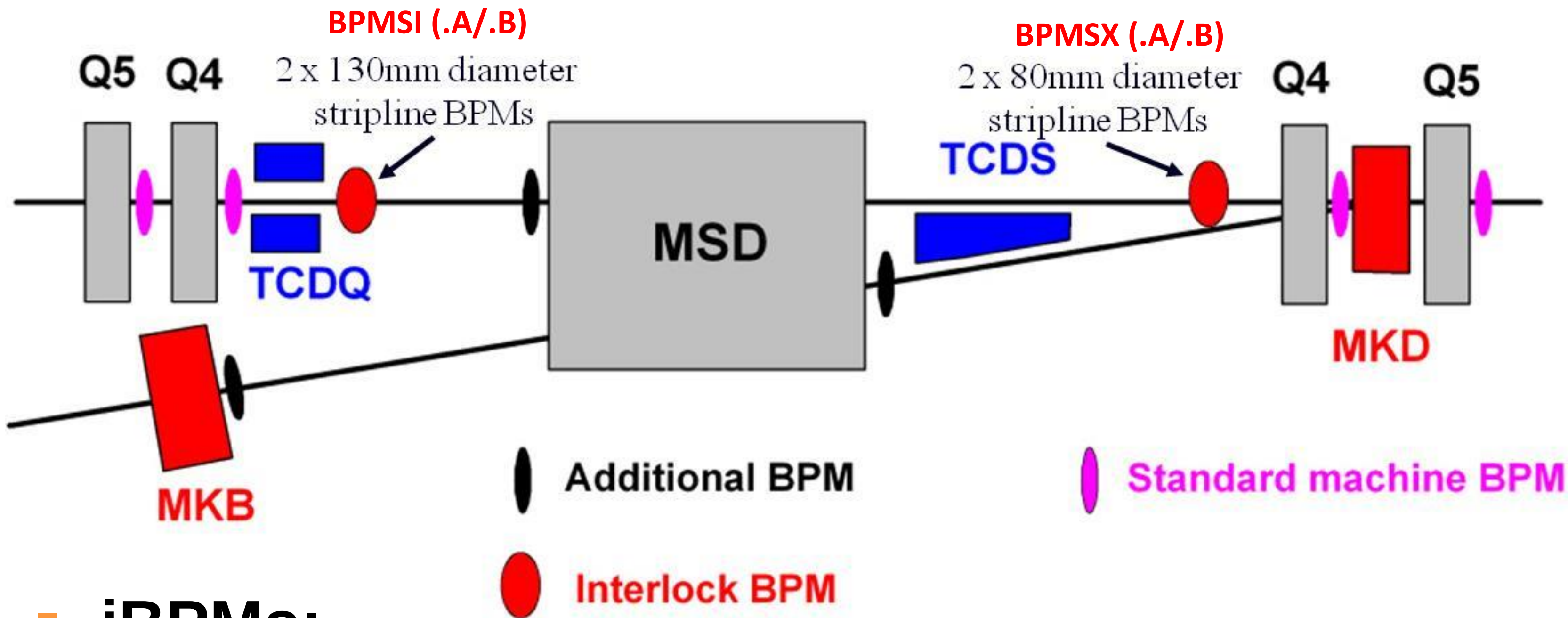
Manfred Wendt (BE-BI-BP)

3/9/2019

Overview of upcoming LHC BPM Activities

- **Interlock BPM consolidation**
  - **8 stripline BPMs left & right of point 6**
  - **New read-out electronics consolidation,**
    - ***initially triggered by operational problems with doublets***
  - **Prototype tested with beam during run 2**
    - ***on BPMS.4L5v***
    - ***Time-multiplexed BPM electrode signals***
    - ***VFC-based commercial 14-bit FMC ADC operating at 2.6 GB/s***
  - **Final prototype to be installed end of LS2**
    - ***Details to be worked out in close collaboration with MPP***
  - **Deployment of the entire system during an upcoming YETS…**

Overview (cont.)

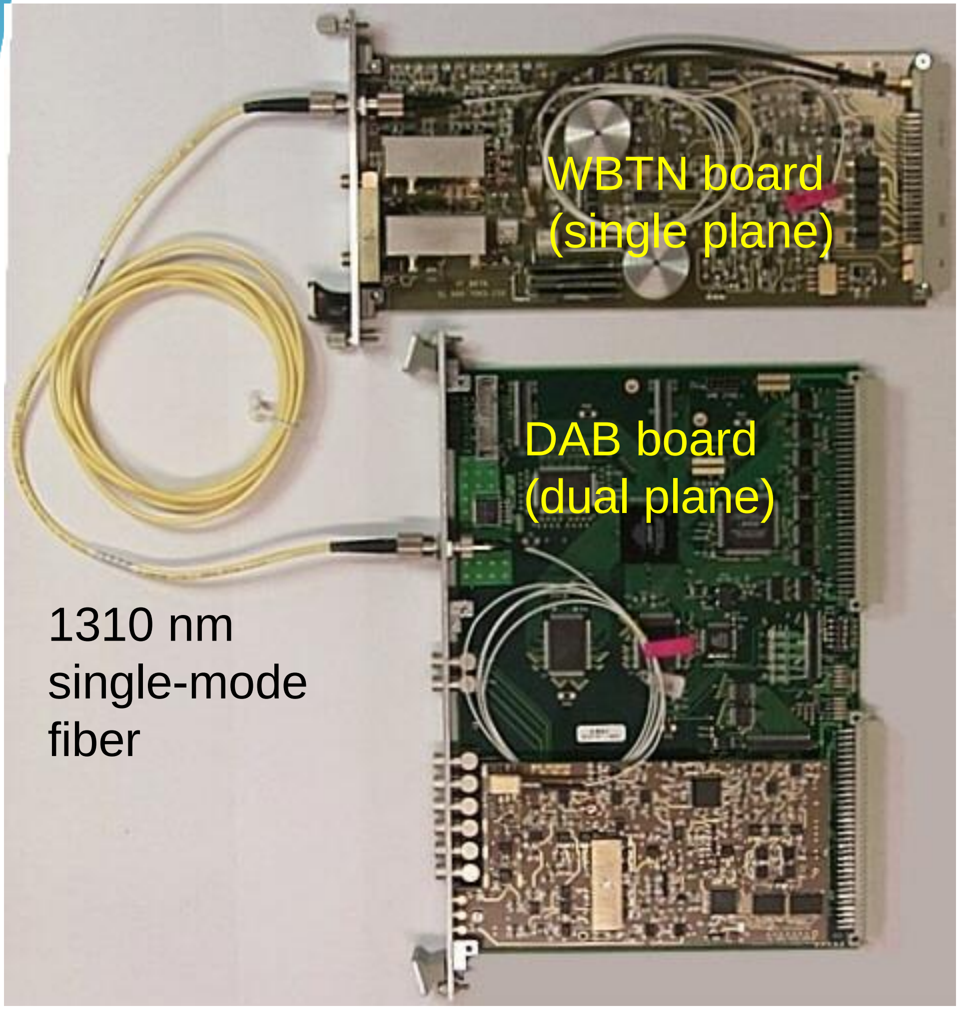


- **iBPMs:**
  "Guinea pig" for the following LHC BPM consolidation and upgrade projects
  - **Time-multiplexing of BPM electrodes**
  - **Single-channel read-out & digitalization in the 1st Nyquist pass-band.**

Overview (cont.)

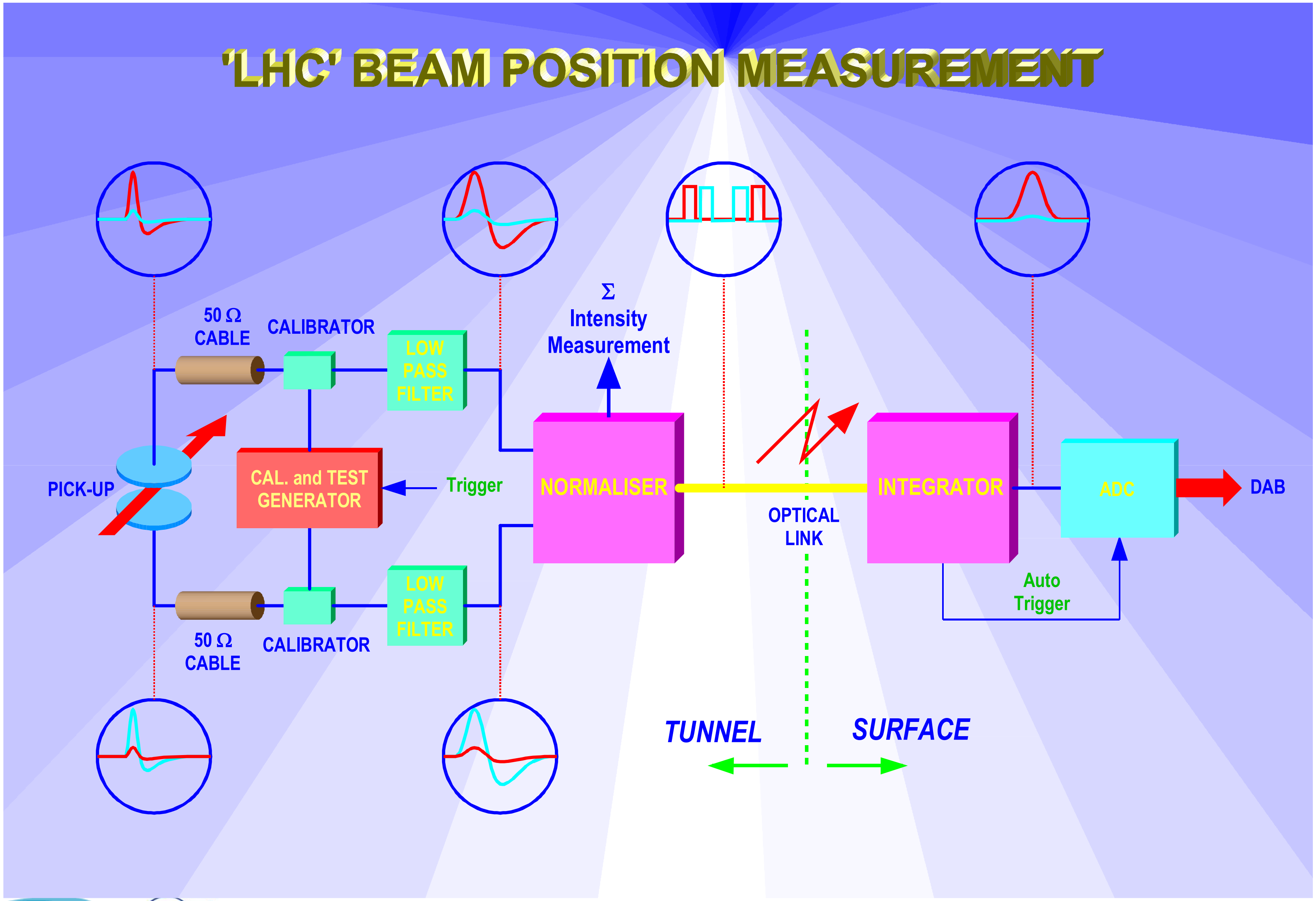
- **HL-BPMs (IR BPMs)**
  - **28 new stripline BPMs**
    - ***"cold" BPMs inside the cryostat***
    - ***Observations of both beams in the same beam pipe***
  - **Requires a new read-out system**
    - ***Final prototyping with beam before LS3!***
    - ***Deployment of the entire system by end of LS3!***
- **Ring BPM consolidation**
  - **New read-out electronics for ~1000 LHC BPMs**
    - ***Based on the given infrastructure***
    - ***Radiation tolerant tunnel electronics***
    - ***Prototyping during run 3***
    - ***Deployment LS3/LS4?***

LHC BPMs: Status Quo

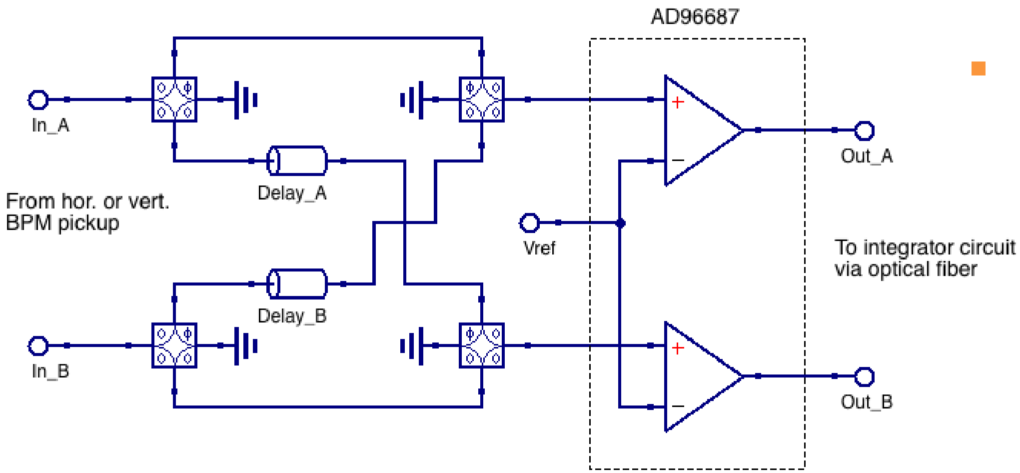


- **WBTN BPM System**
  - **Time encoded bunch-by-bunch signal processing**
  - **2 optical fibers per BPM**
- **DOROS BPMs**
  - **Narrowband electronics**
  - **Collimator & IR BPMs**

WBTN BPM Functional Principle



WBTN (cont.)



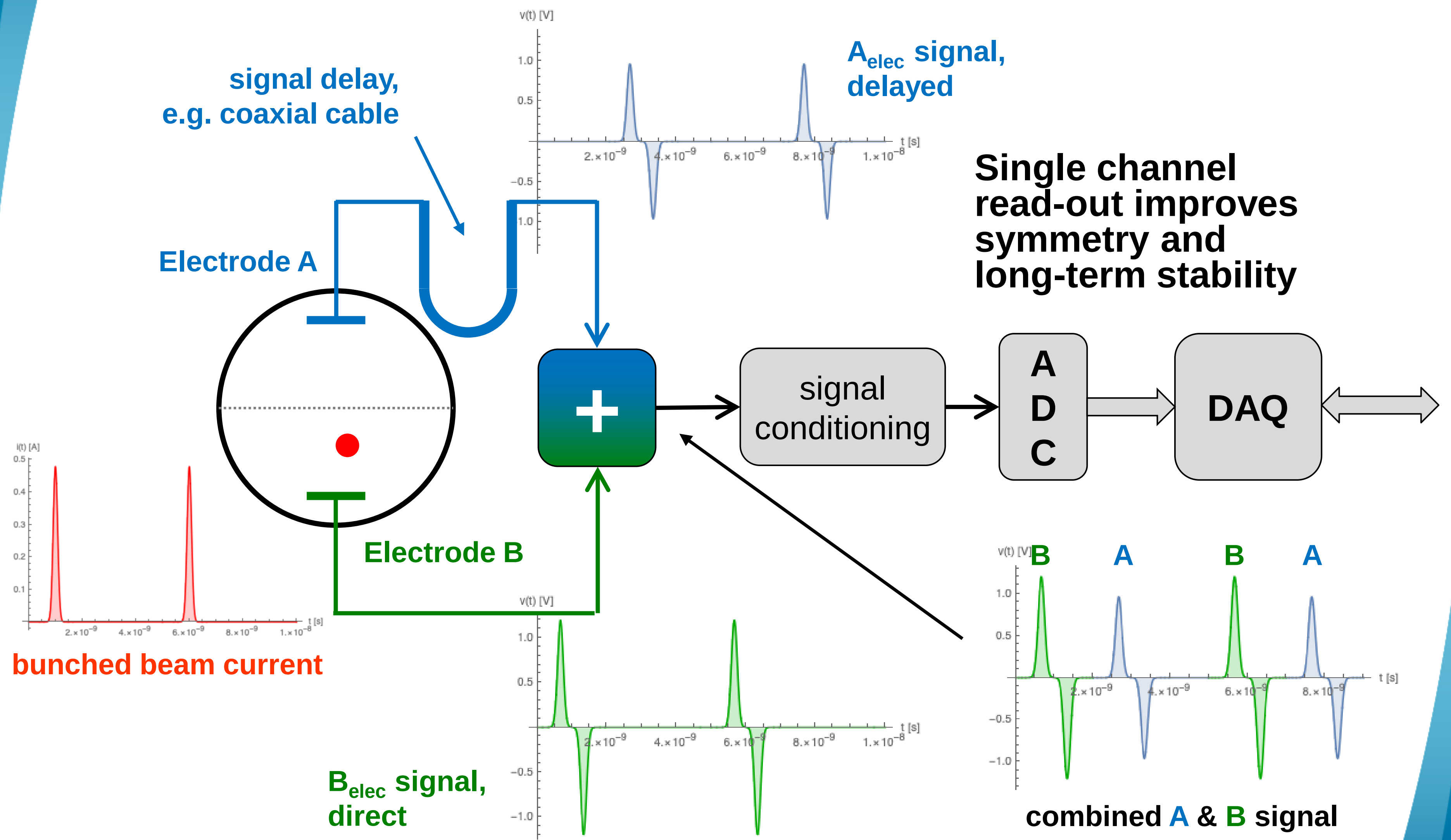
- **70 MHz LPF & AD96687 analog comparator define the core performance**
  - **<=46 dB dynamic range**
  - **Vref set to**
    - ***2mV: HI sensitivity***
    - ***67mV: LO sensitivity***

- **Still fulfills most requirements, BUT:**
  - **Residual temperature sensitivity**
    - ***Despite temperature controlled racks for the VME-based analog integrators***
  - **Aging effects, e.g. "electronic" offset drifts**
    - ***Analog electronics components***
  - **Sensitive to signal reflections between BPM pickup and read-out electronics**
  - **Dynamic range limitations**
    - ***Defined by the dual analog comparator circuit***
  - **Long-term maintainability, spares, calibration, etc.**
    - ***Complex analog signal conditioning circuit***
    - ***Will be 20 years in operation after LS3***

LHC BPM Consolidation

- **Requirements**
  - **Should meet ALL requirements of the present LHC BPM read-out system**
  - **PLUS some improvements, e.g.**
    - ***Resolution, reproducibility over long time periods, additional flexibility through gateware-based signal processing***
  - **Two main “customers”:**
    - ***LHC OP: pilot, but mostly full machine with nominals, beam orbit mode, OFB, stability, reproducibility***
    - ***ABP: (fat) pilot, TbT mode, SB resolution***
- **Boundaries**
  - **Keep the existing infrastructure**
    - ***BPM pickups, optical fibers***
  - **Requires radiation tolerant components!**

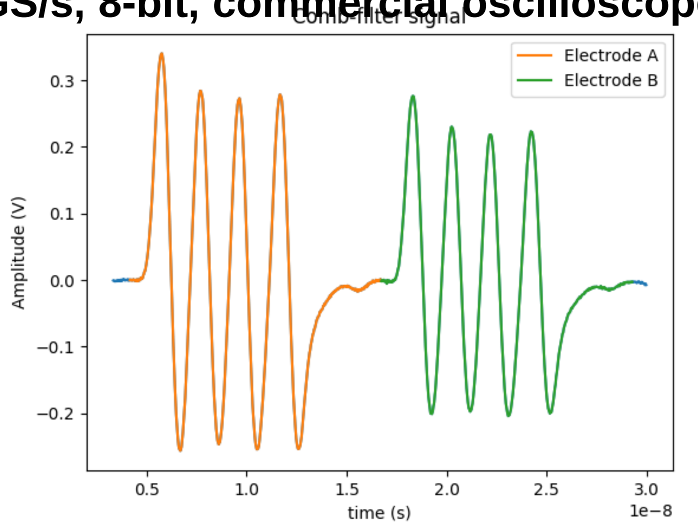
Concept: Time-multiplexed BPM signal processing

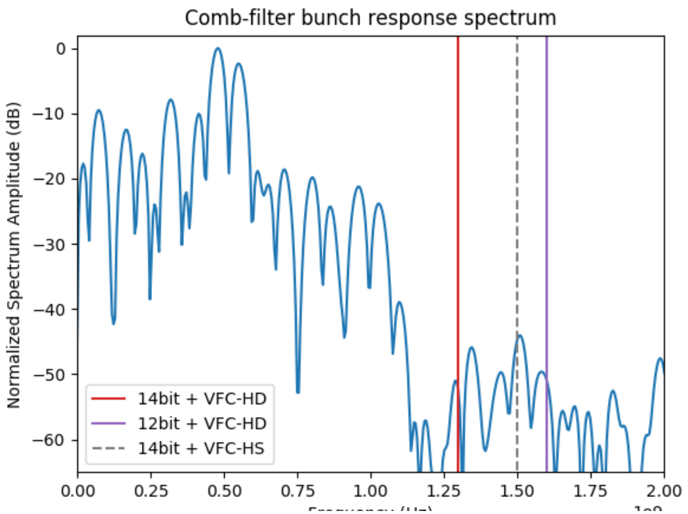


Single channel read-out improves symmetry and long-term stability

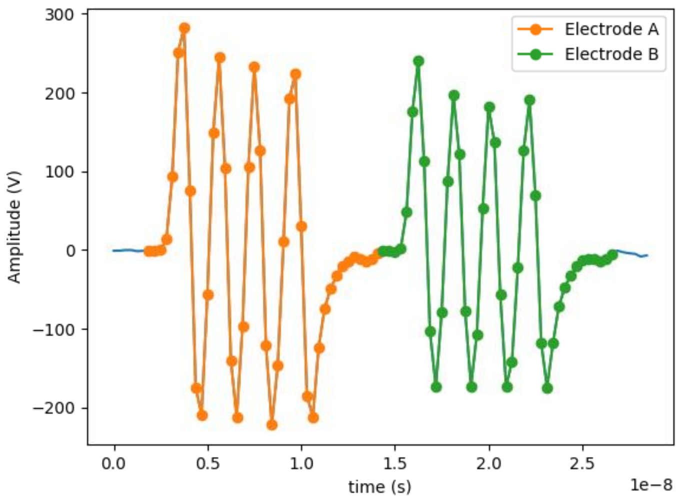
Interlock BPM R&D: Beam Measurements

60 GS/s, 8-bit, commercial oscilloscope

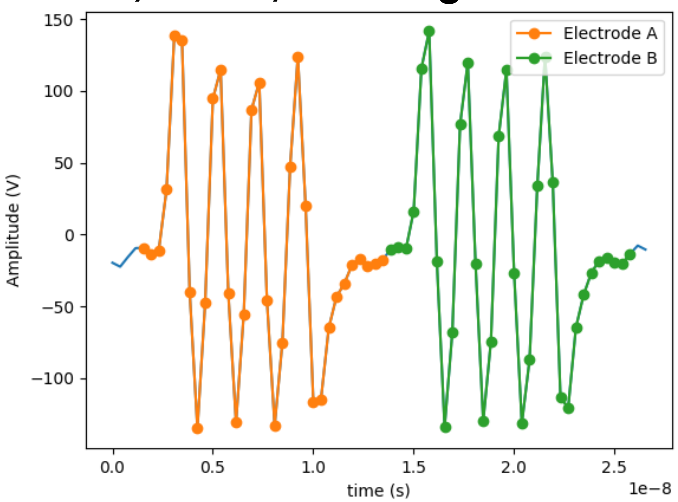




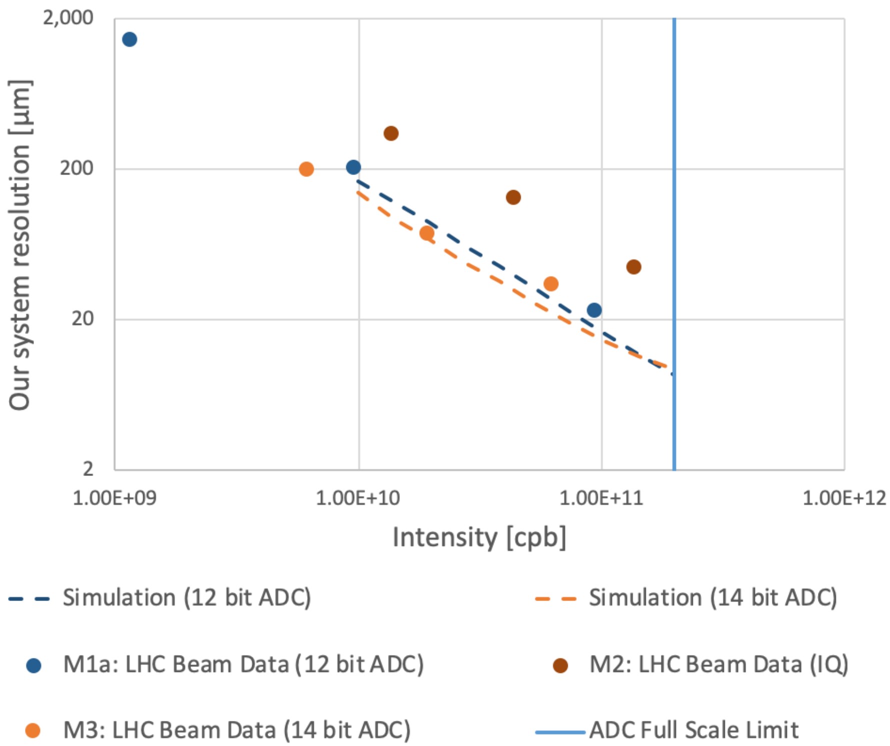
3.2 GS/s, 12-bit, FMC digitizer

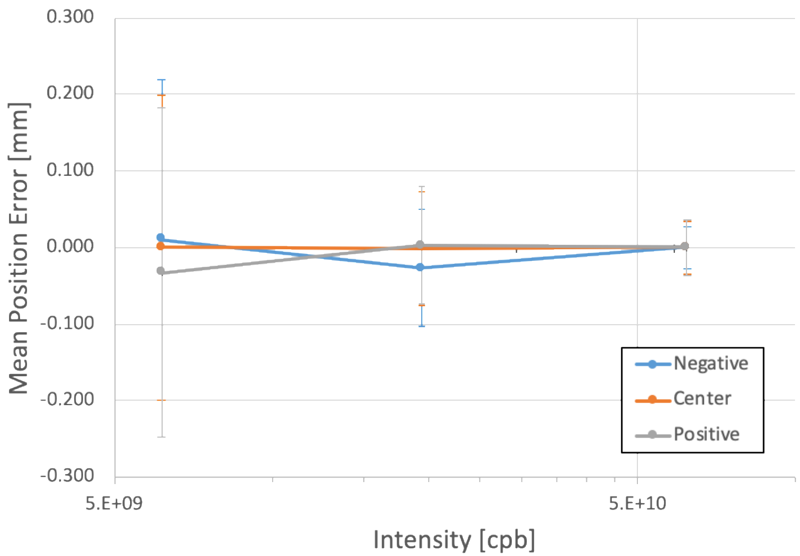


2.6 GS/s, 14-bit, FMC digitizer



Interlock BPM R&D: Estimated Performance





- Meets the LHC interlock BPM resolution requirement
  - <500 µm RMS bunch-by-bunch for a range of 5e9…2e11 ppb w/o gain switching!
  - including a beam displacement range of ±7.5 mm
- Keeps the reported mean value beam position over the entire bunch intensity range
- Operates also with 5+20 ns doublet bunches
  - at a reduced performance

Ideas / Plans for the LHC BPM Consolidation

- **Based on radiation tolerant ADCs**
  - **Space-grade / commercial 12-bit, multi-GB/s**

TELEDYNE e2V Everywhereyoulook™

- 1 Vpp 100Ω differential DC
- 100Ω Differential input AC coupled clock

for user's interleaving calibration

Sampling

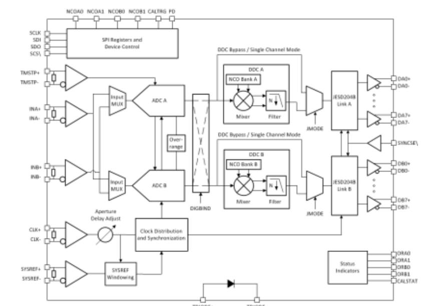
ADC12DJ3200QML-SP

12-Bit, Dual 3.2-GSPS or Single 6.4-Gsps ADC with JESD204B Interface

Features

• Configurations (SPI controlled):	Dual 12-bit 3.2 GSPS
	Single 12-bit 6.4 GSPS
• Low Power:	3.6 W total (1ch Mode, BG Cal)
• Buffered Inputs:	6-GHz Input Bandwidth (-3 dB)
• Input Fullscale:	0.8 Vpp (Adjustable, 0.5 Vpp to 0.95 Vpp)
• Noise Floor (3.2 Gsps):	-150 dBFS/Hz
• Noise Floor (6.4 Gsps):	-153 dBFS/Hz
• IMD3 at fin = 2.5GHz:	-73 dBc (@ -7 dBFS)
• Code Error Rate:	10^{-18}
• Optional Decimation	2x (real), 4/8/16x (complex)
• Digital Interface:	JESD204B
	Subclass 1 support
	8 Lanes at 12.8 Gbps (max Fs)
	16 Lanes at 6.4 Gbps (max Fs)
• Power supplies:	1.1V, 1.9V
• Package:	Space Grade Ceramic LGA (15x15mm)

1-ch Mode Performance (6.4 GSPS)	1 GHz	2.5 GHz
SNR (dBFS, typ, int. spurs excluded, -1dBFS)	56	55
NSD (dBFS/Hz, typ)	-153	-152
HD2,3 (dBc, typ)	-68	-68
Non HD2,3 (dBc, typ)	-73	-72
Interleaving Spur (dBFS, typ)	-63	-58



TI Confidential – NDA Restrictions

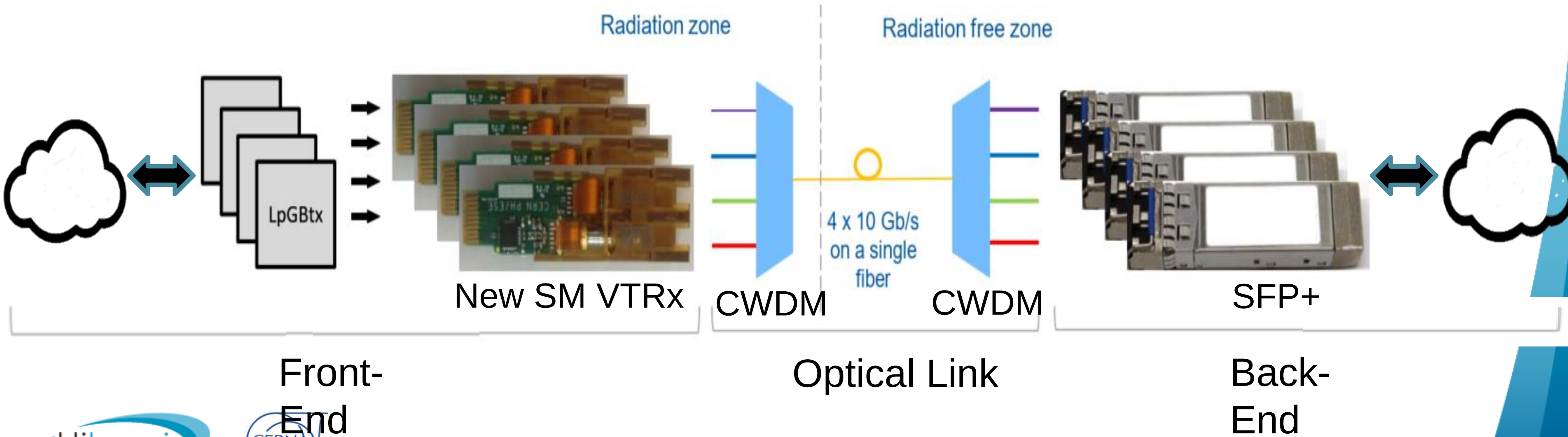
Texas Instruments

- **Need to qualify radiation compatibility our self!**

HiLumi HL-LHC PROJECT CERN

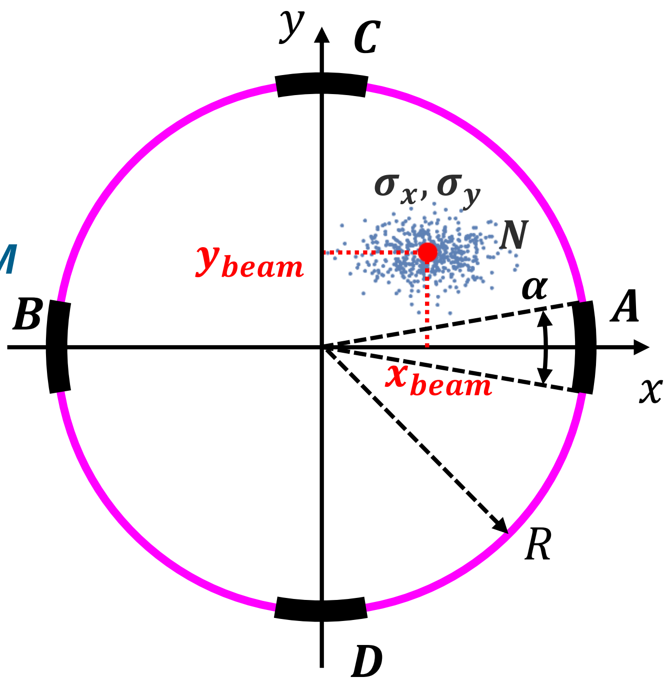
Ideas / Plans for the LHC BPM Consolidation

- **Requires radiation tolerant digital optical link technologies**
  - **Current plan:**
    Ship raw ADC data of each BPM to the surface for post-processing
  - **Choices to be made:**
    - ***ADC data format: serial or parallel?***
      - Parallel requires LpGBTx (7 elinks @ 1280 MB/s, 14 elinks @ 640 MB/s, 28 elinks @ 320 MB/s)
    - ***Max data payload, w/o or with wavelength multiplexing (CWDM)***
      - 2x or 4x CWDM, additional insertion losses, increasing costs! VTRx: 10.24 GB/s
    - ***Max serial lane rate***



Time-Multiplexing: 2 or 4 BPM Electrodes?

- **More choices to be made:**
  - **Measurement of higher moments: Quadrupolar Moment**
  - **Access to the beam emittance?!**
    - ***Requires perfect symmetry!***
    - ***Requires an elliptical beam profile at the BPM***
    - ***Requires perfect beam position "nulling"***
  - **Make use of statistics**
    - ***High sampling rate & # of samples***
    - ***Large number of BPMs***

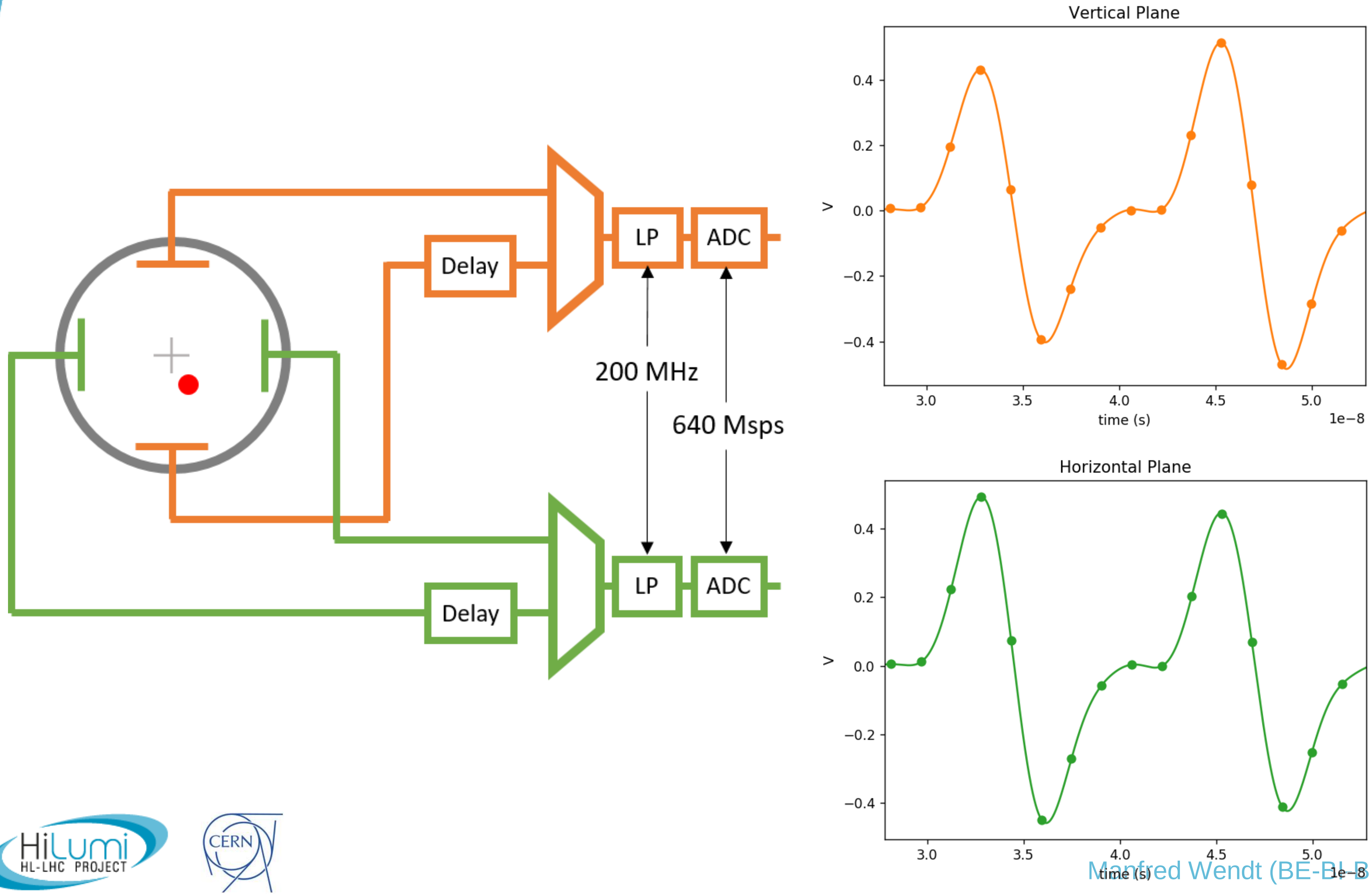


monopole moment ∝ intensity (common mode)

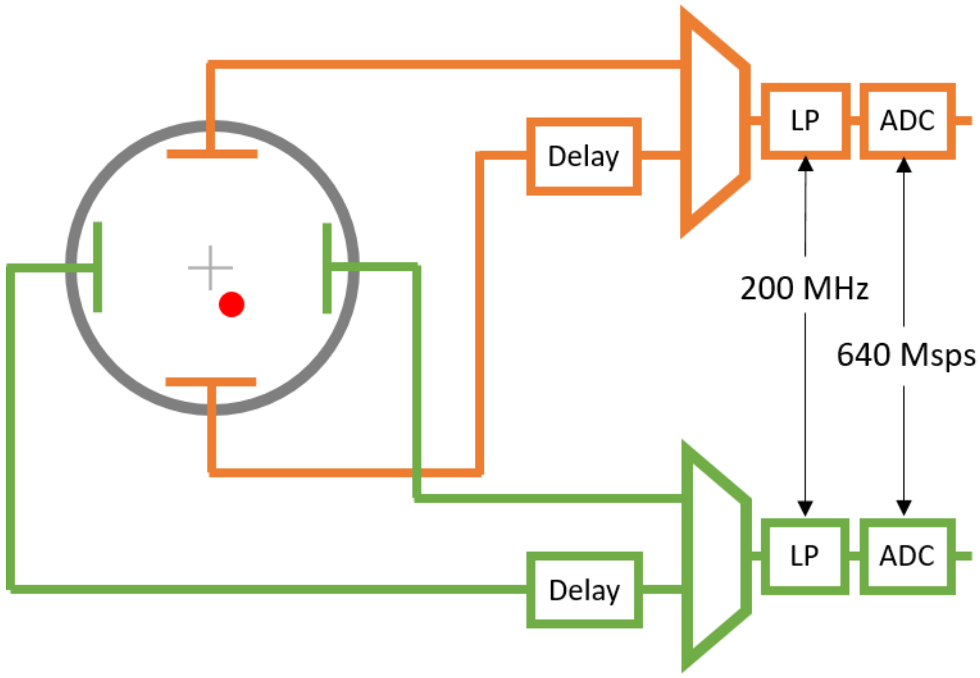
$$I_A = -\frac{I_{beam}}{\pi}\left[\frac{\alpha}{2} + \frac{2}{R}\sin\left(\frac{\alpha}{2}\right)x_{beam} + \frac{1}{R^2}\sin(\alpha)\left(\sigma_x^2 - \sigma_y^2 + x_{beam}^2 - y_{beam}^2\right) + \cdots\right]$$

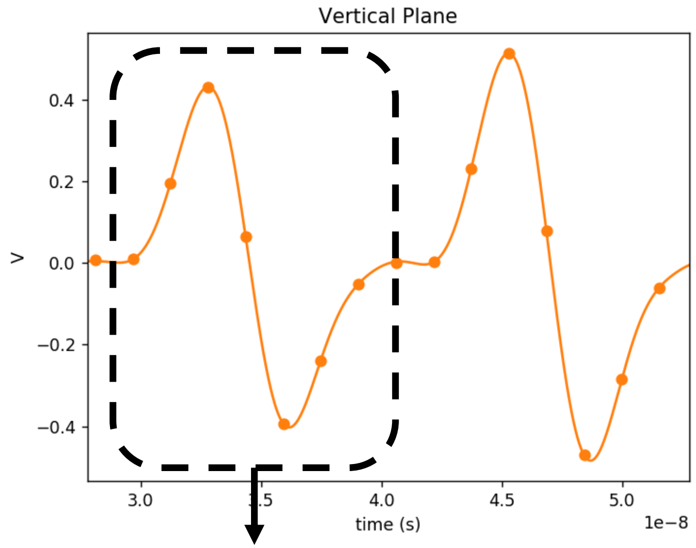
dipole moment ∝ position/R **quadrupolar moment ∝ (Δsize+Δpos)/R^2**

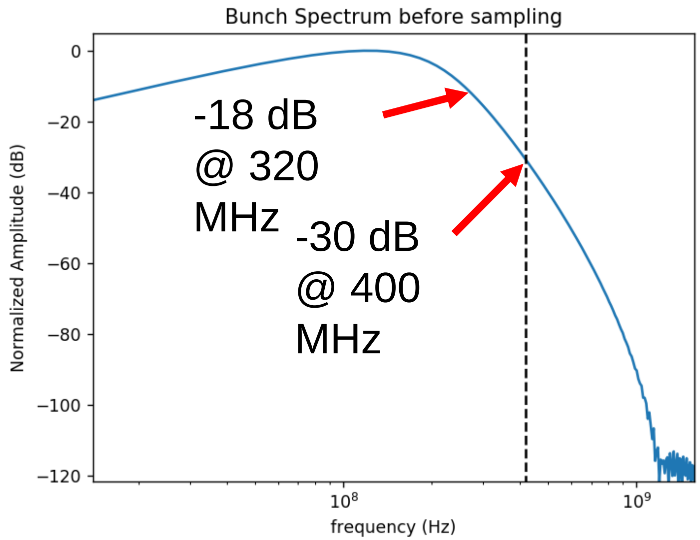
Electrode Time Multiplexing – 2 Electrodes



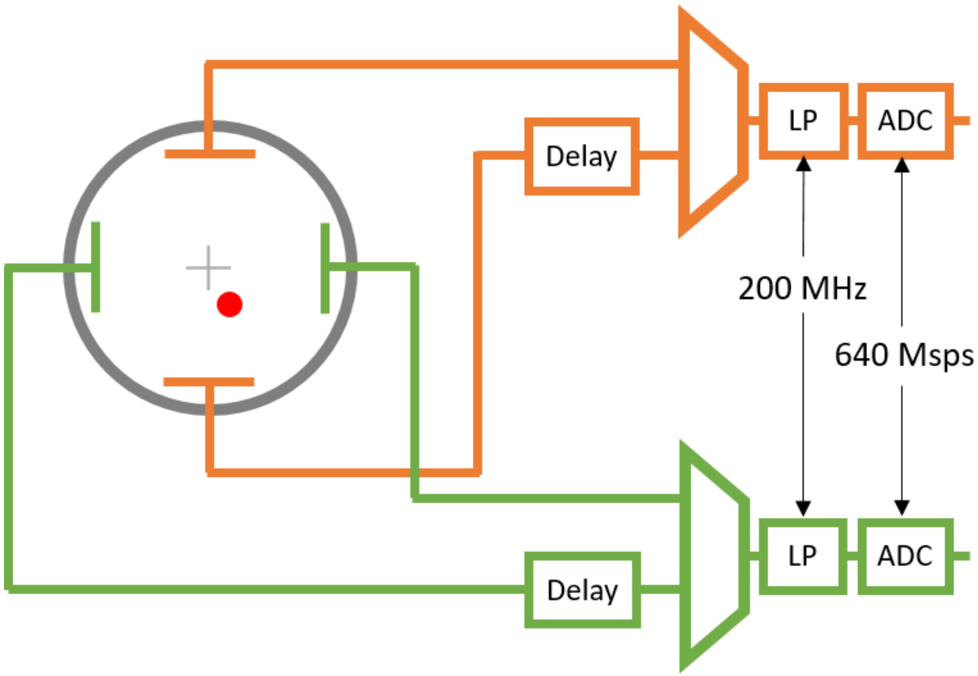
Electrode Time Multiplexing – 2 Electrodes

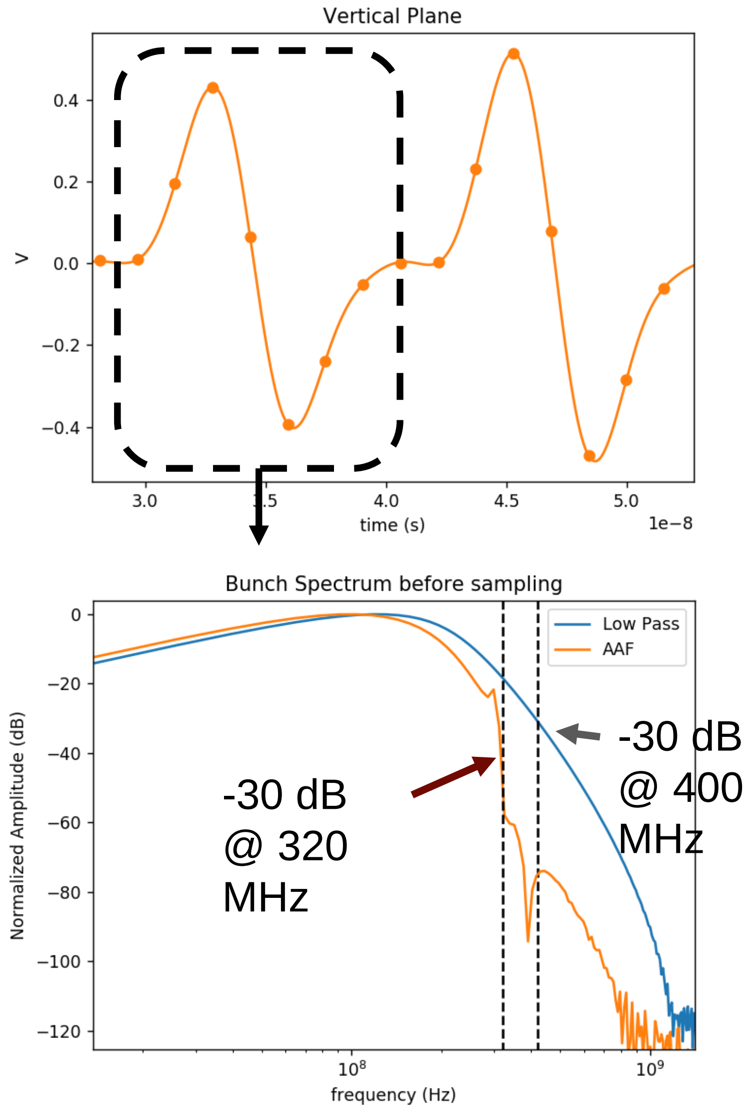






Electrode Time Multiplexing – 2 Electrodes





HL-LHC IR BPM Read-out System

- **Requires the compensation of error terms from the counterrotating beam!**
  - **B1-B2 bunch spacing can be as close as ~4 ns**
  - **Stripline BPM directivity likely to be <26 dB**
    - ***Requires “on the flight” error correction***
  - **Prefer commercial, non rad-tolerant solution!**
    - ***More choices, lower costs on “standard” components***
    - ***Benefit from RFSoC processor technologies***
    - ***Requires racks in non radiation areas***
      - Up to 140 meter long signal cables

- **RFSoC monolith (single die):**
  - **8x RF ADC**
    - ***12/14-bit, 4 GB/s***
  - **8x RF DAC**
    - ***14-bit, 6.5 GB/s***
  - **2x ARM Real-time processor**
  - **FPGA**
    - ***930k cells, 850k FFs***
  - **RAM, PLLs, etc.**

Key Components of the Zynq UltraScale+ RFSoC

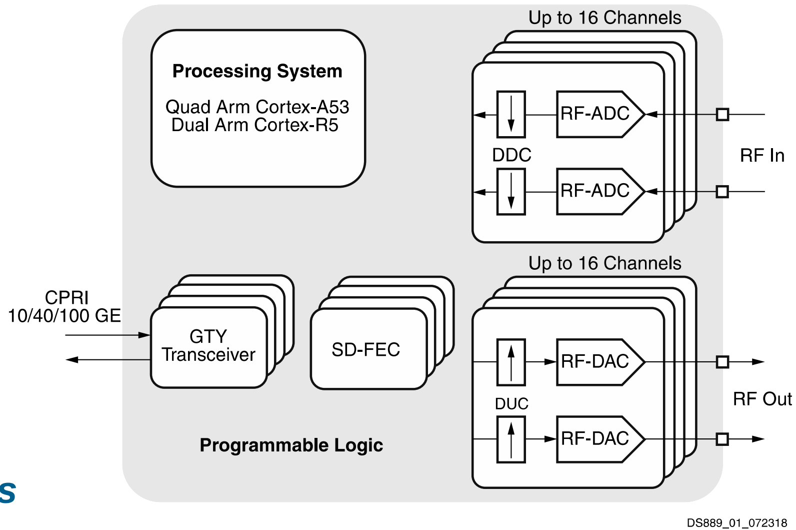


Figure 1: **Zynq UltraScale+ RFSoC**

Discussion

- **Interlock BPMs**
  - **Safety system: no gain switching**
    - ***Resolution limited by ADC dynamic range***
- **LHC IR & ring BPMs**
  - **AGC via DAC, e.g. triggered during abort gap**
    - ***How to handle gain setting during beam commissioning***
- **Calibration signals**
  - **Still need a concept for the ring BPMs**
    - ***RFSoC DAC based for the IR BPMs***
- **IR BPM signal cables**
  - **Should we save on the signal cable installation?!**
    - ***Time-multiplexing B1-B2 stripline ports near the pickup***

Summary

- **LHC BPM CONS and upgrade projects**
  - **Will be based on time-multiplexed single channel read-out techniques**
    - ***Offer better long term-stability, no symmetry breaking***
  - **Will make use of state-of-the-art RF and digital signal processing techniques**
    - ***High sampling rates give more statistics***
      - -> better resolution (~20…50x more samples than presently)
  - **Minimize analog and RF components**
    - ***Prone to aging, temperature and other drift effects***
  - **Will reuse the given infrastructure**
    - ***BPM pickups, optical fibers, etc. if applicable***