ALEJANDRO RODRIGUEZ ALVAREZ

SUMMER STUDENT

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Proposal of an auxiliary channel to monitoring and control the HMPID Readout Control Board

through the JTAG interface.

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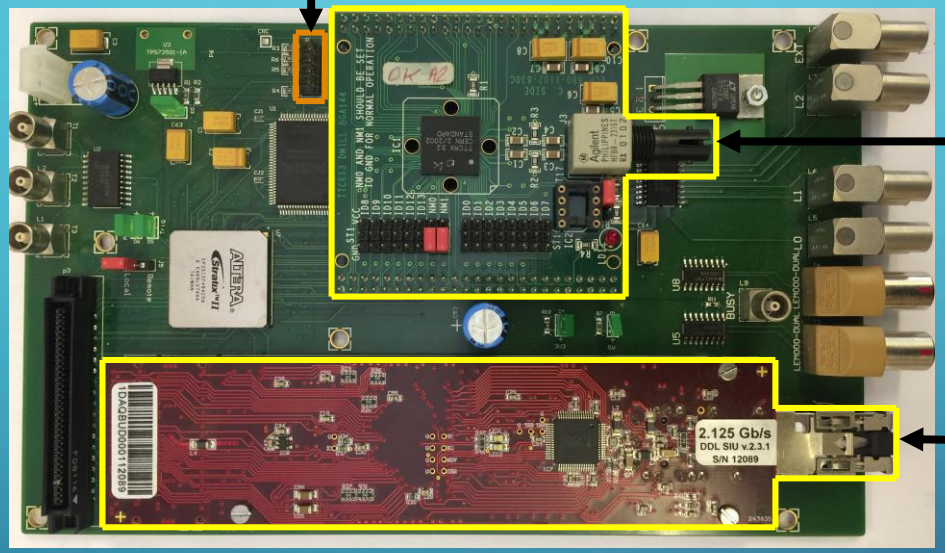
Objective:

- Develop and build an auxiliary channel for monitoring and control of the states of the Readout Card

- Perform this task without modifying the infrastructure that is already inserted.

Readout and Control Board (RCB)

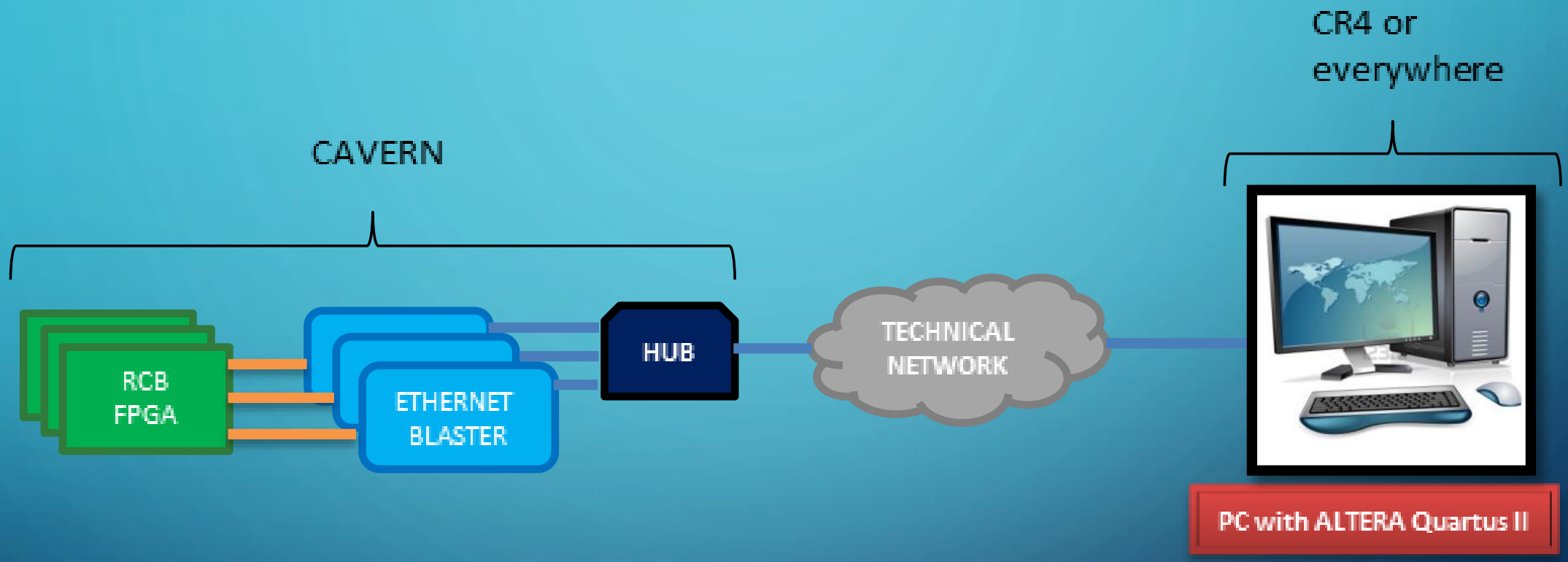
JTAG connector



TTCRx connected to the LTU (Unidirectional)

DDL SIU connected to the FLP (Bidirectional)

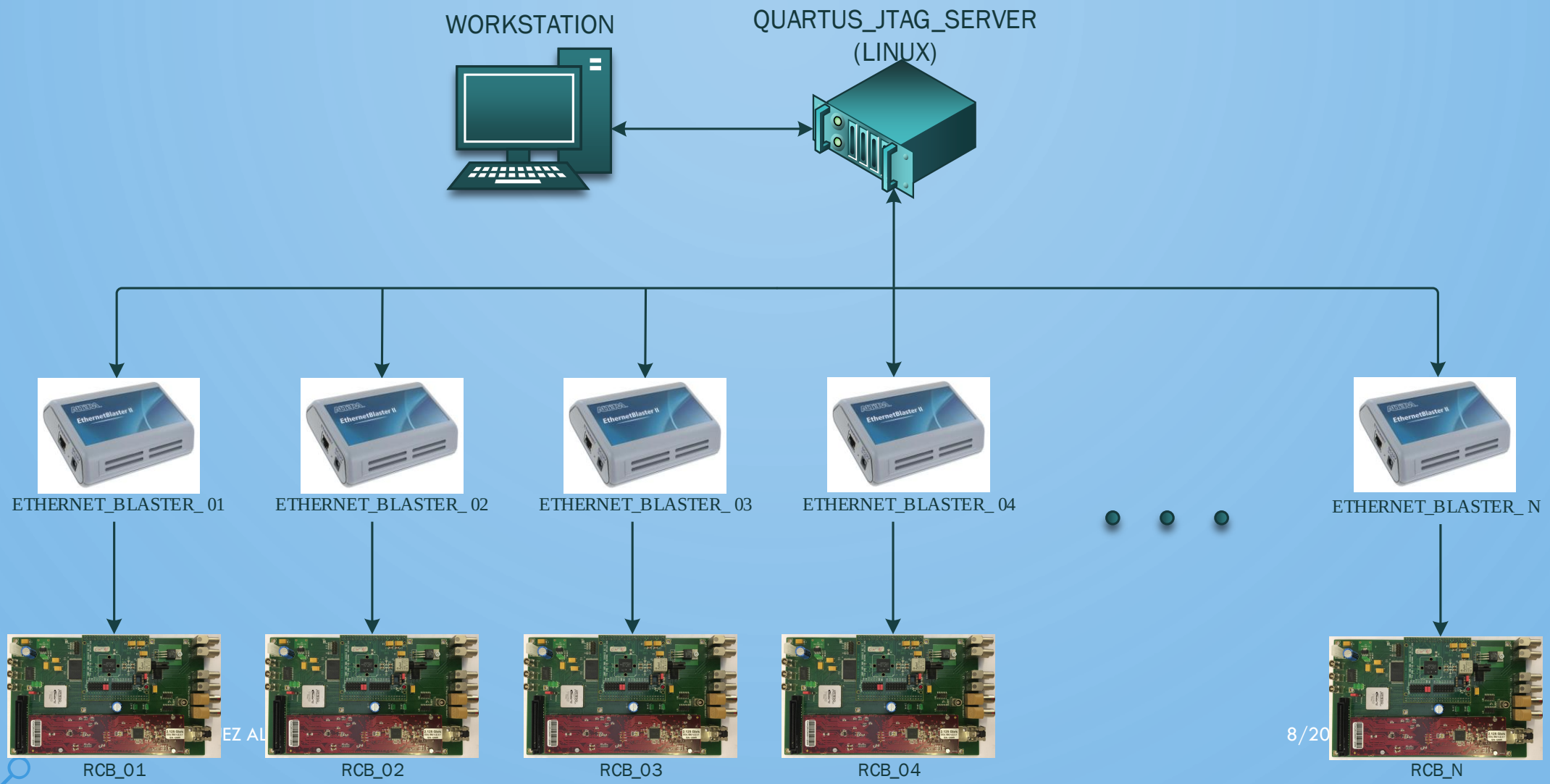
Current diagram setup for the remote programming system



Mapping between the EthernetBlaster IP addresses on the technical network, the flat cable flags and the DDL numbers

POSTION IN THE DETECTOR	DDL NUMBER	ETHERNETBLASTER IP ADDRESS	FLAT CABLE FLAG
RICH 0, LEFT	1536	10.160.128.67	1HMPBAIOC00019804
RICH 0, RIGHT	1537	10.160.128.64	1HMPBAIOC00019803
RICH 1, LEFT	1538	10.160.128.63	1HMPBAIOC00019806
RICH 1, RIGHT	1539	10.160.128.62	1HMPBAIOC00019805
RICH 2, LEFT	1540	10.160.128.57	1HMPBAIOC00019808
RICH 2, RIGHT	1541	10.160.128.65	1HMPBAIOC00019807
RICH 3, LEFT	1542	10.160.128.66	1HMPBAIOC00019809
RICH 3, RIGHT	1543	10.160.128.61	1HMPBAIOC00019810
RICH 4, LEFT	1544	10.160.128.55	1HMPBAIOC00019812
RICH 4, RIGHT	1545	10.160.128.56	1HMPBAIOC00019811
RICH 5, LEFT	1546	10.160.128.68	1HMPBAIOC00019814
RICH 5, RIGHT	1547	10.160.128.58	1HMPBAIOC00019813
RICH 6, LEFT	1548	10.160.128.59	1HMPBAIOC00019816
RICH 6, RIGHT	1549	10.160.128.60	1HMPBAIOC00019815

Proposal of the communication channel



WorkStation Requirements

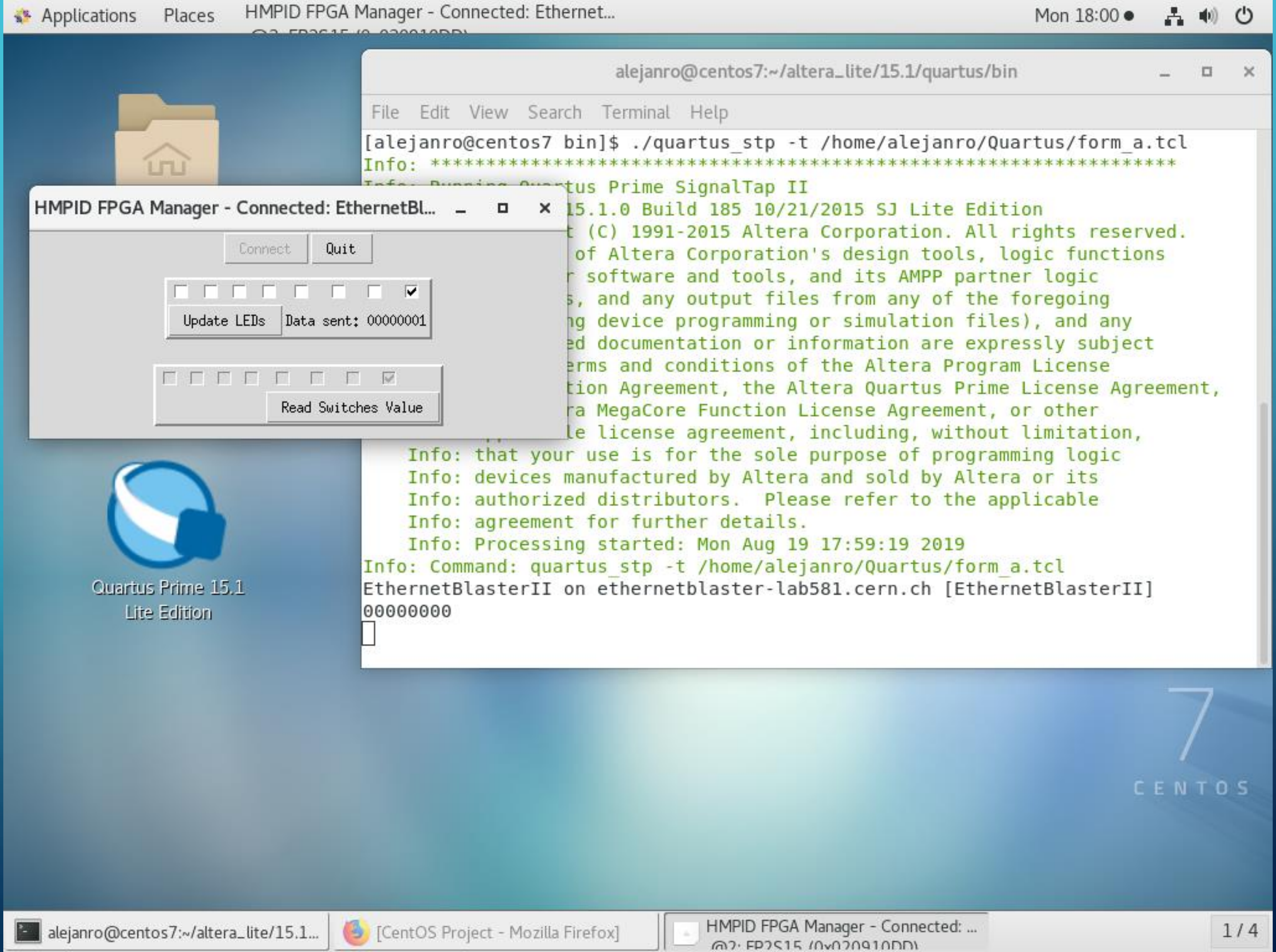
- ssh cliente

Sintaxis example:

ssh -Y user@jtag-server-address “quartus_stp –t script_name.tcl”

Quartus_JTAG_Server Requirements

- Running Altera Quartus II Software (quartus_stp executable)
- Access to all Ethernet Blaster Programmers must be configured
- Linux Operative System (CentOS 7)


Applications
Places
HMPID FPGA Manager - Connected: Ethernet...
Mon 18:00
alejanro@centos7:~/altera_lite/15.1/quartus/bin
File Edit View Search Terminal Help
[alejanro@centos7 bin]$ ./quartus_stp -t /home/alejanro/Quartus/form_a.tcl
Info: ***
tus Prime SignalTap II
15.1.0 Build 185 10/21/2015 SJ Lite Edition
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of Altera Corporation's design tools, logic functions
r software and tools, and its AMPP partner logic
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tion Agreement, the Altera Quartus Prime License Agreement,
ra MegaCore Function License Agreement, or other
le license agreement, including, without limitation,
Info: that your use is for the sole purpose of programming logic
Info: devices manufactured by Altera and sold by Altera or its
Info: authorized distributors. Please refer to the applicable
Info: agreement for further details.
Info: Processing started: Mon Aug 19 17:59:19 2019
Info: Command: quartus_stp -t /home/alejanro/Quartus/form_a.tcl
EthernetBlasterII on ethernetblaster-lab581.cern.ch [EthernetBlasterII]
00000000
HMPID FPGA Manager - Connected: EthernetBl...
Connect
Quit
Update LEDs
Data sent: 00000001
Read Switches Value
Quartus Prime 15.1 Lite Edition
CENTOS
alejanro@centos7:~/altera_lite/15.1...
[CentOS Project - Mozilla Firefox]
HMPID FPGA Manager - Connected: ...
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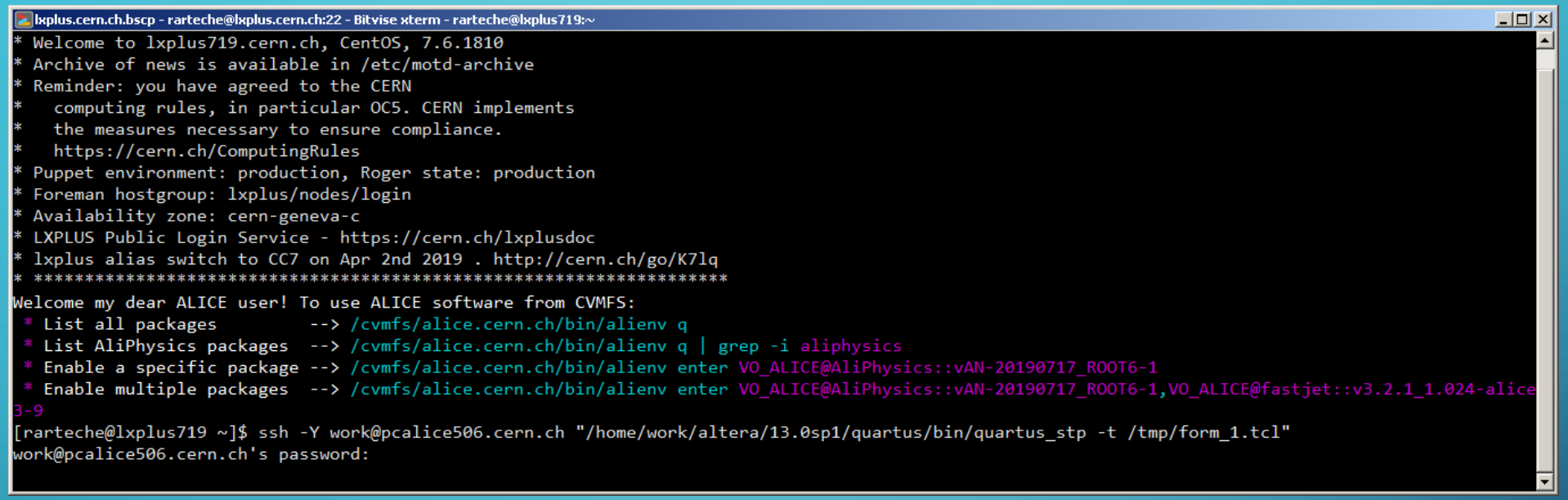
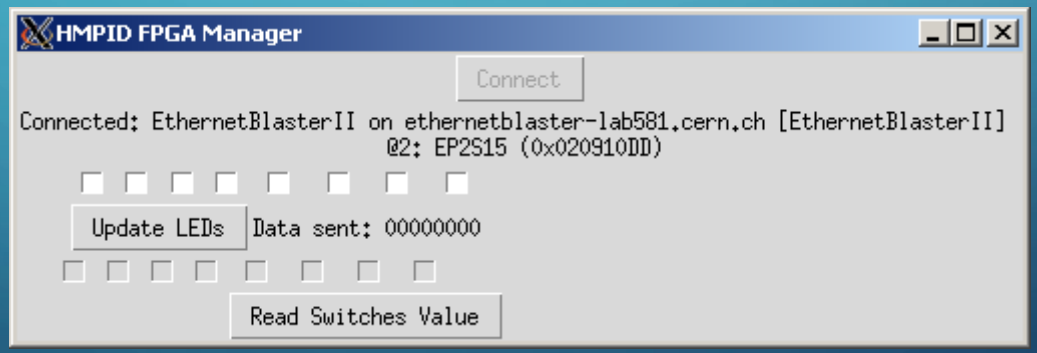
Current Implementation Test



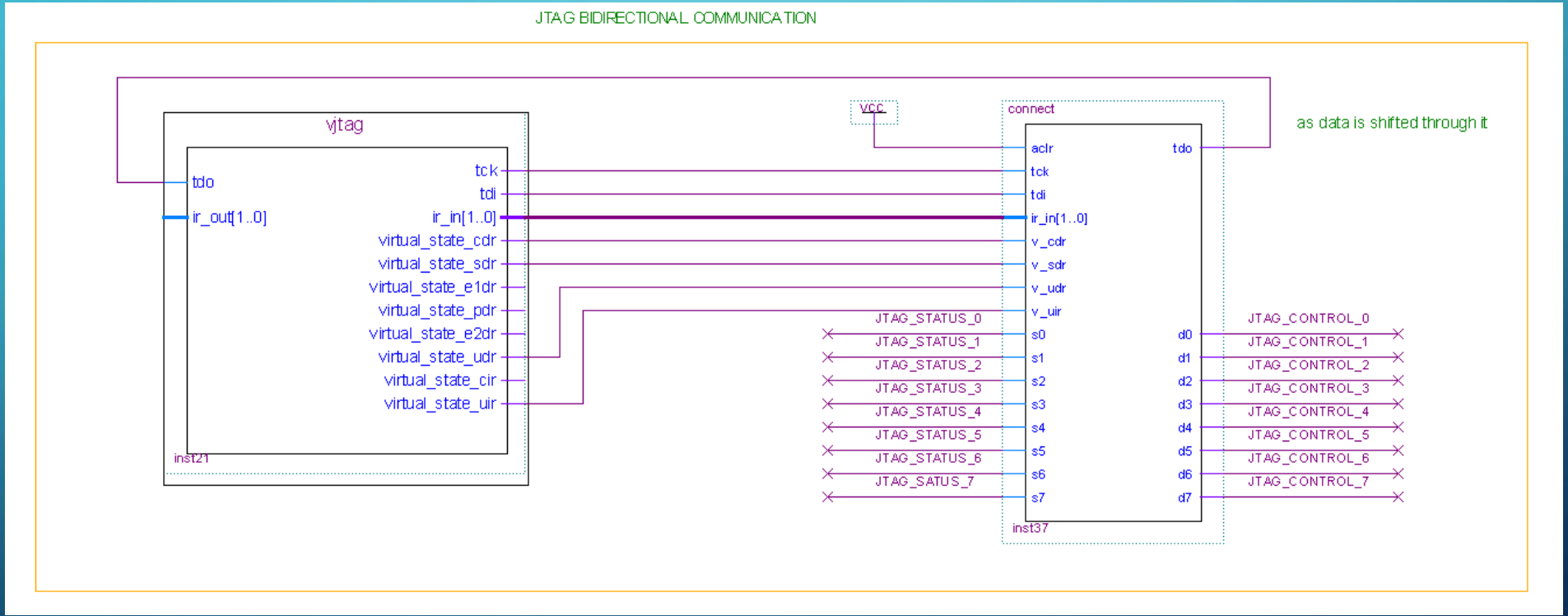


Design flow of the virtual JTAG IP core

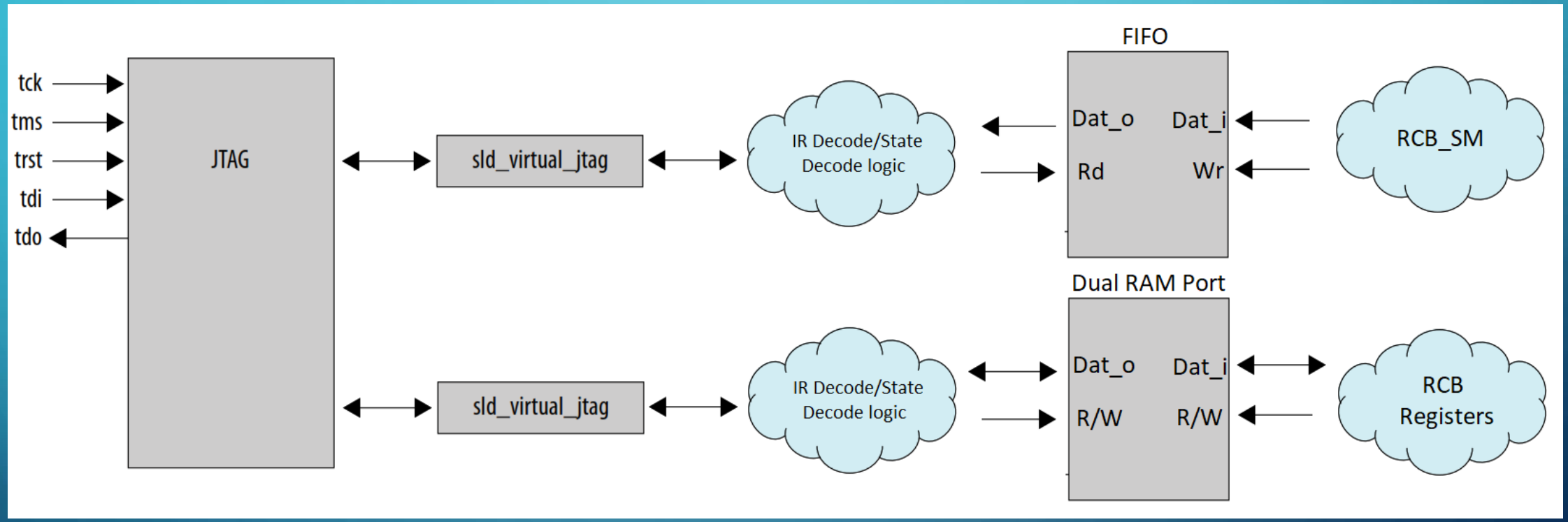
Designing with the Virtual JTAG IP core includes the following processes:

- Configuring the Virtual JTAG IP core with the desired Instruction Register length and instantiating the IP core.
- Building the glue logic for interfacing with the application.
- Communicating with the Virtual JTAG instance during runtime.

Current Implementation Test



Application example



Conclusion

- No need Hardware Modification.
- Allow to monitor and control what happen inside the RCB FPGA.
- The resource that use inside the FPGA are minimum.