WP 1.3 Modules

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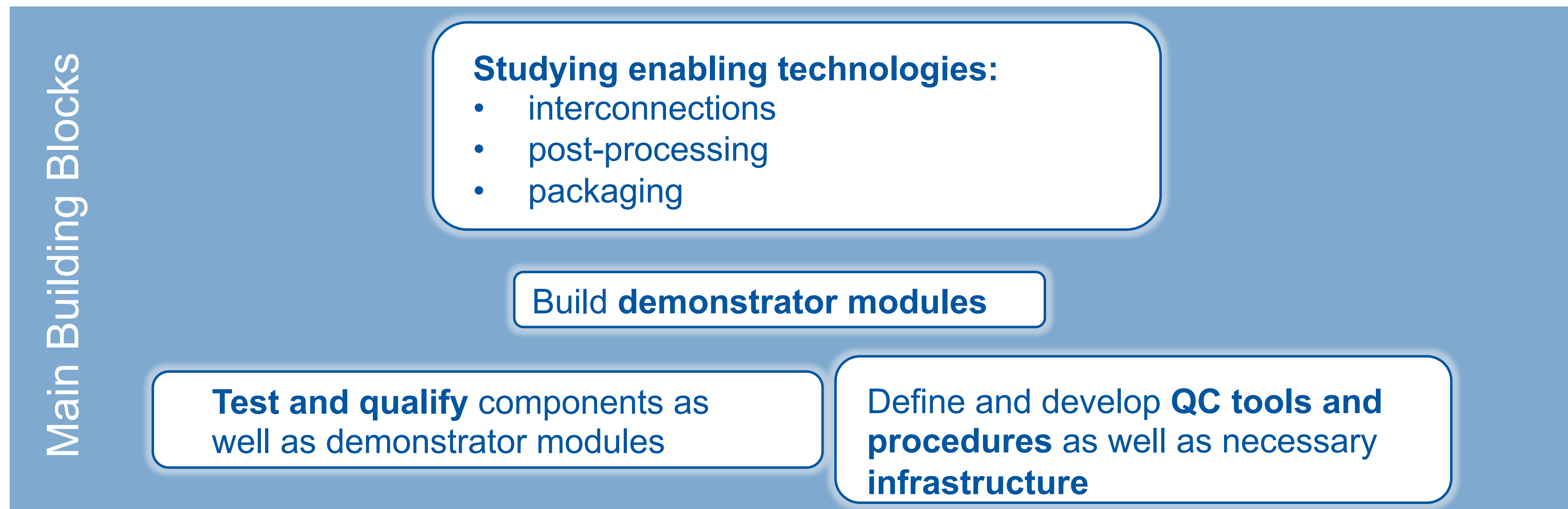
This activity focusses on the **study and development of new modules for hybrid and CMOS pixel detectors** and continues and builds on existing activities, e.g. pixel R&D in EP-DT.

Two main areas which are tightly linked are highly integrated module assembly techniques for large area **CMOS modules** and **compact hybrid modules**.

Proposed activities are in line with the originally proposed program (see presentation in the R&D workshop Oct. 2018), but have been streamlined to meet the proposed budget.



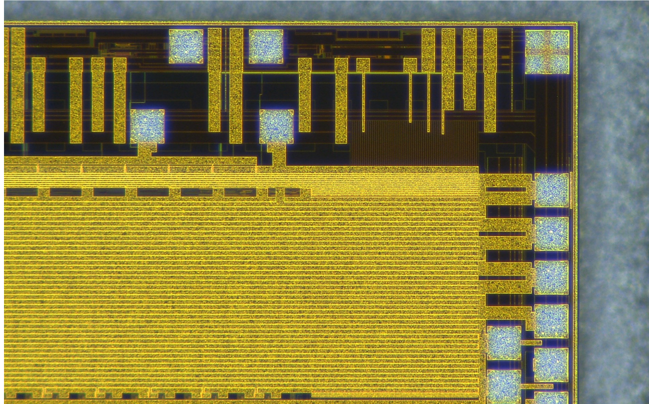
Post-processing

Thinning and dicing

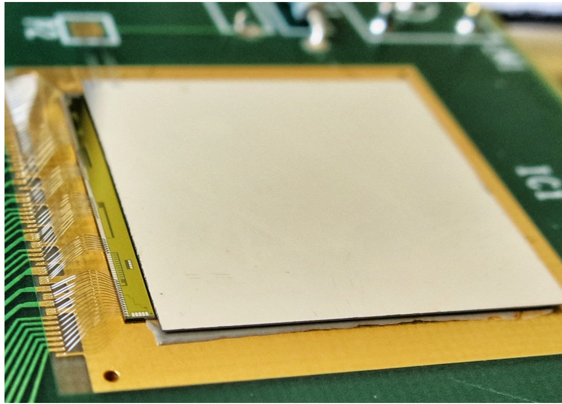
- Investigate alternative dicing techniques to achieve minimum dead area at the die edge and optimize die robustness on the edge
- Study stress effects and counter measures (process adaptation, compensation layers,..)
- Systematic thinning studies leading to ultra-thin sensors (<30 μm)
- Validation using existing wafers

Minimum gap tiling for hybrid+CMOS pixel modules – ultra-thin modules – large area modules with minimum material

Laser dicing of CMOS sensors (disco.com)



100μm+100μm Timepix assembly (IZM)



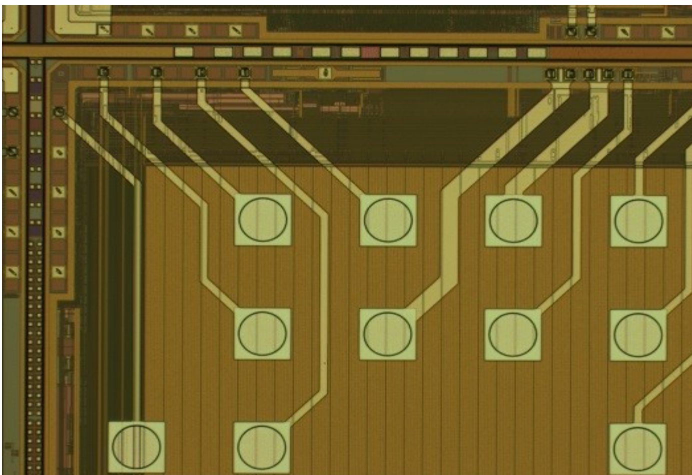
Post-processing & Interconnection

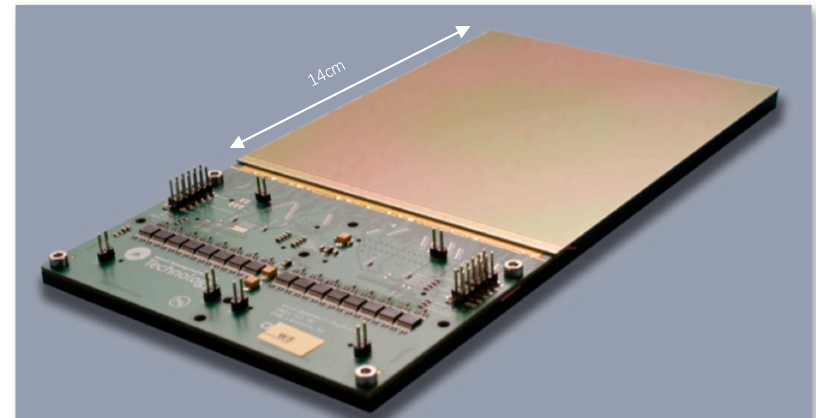
Plating and Re-Distribution Layers (RDL)

- Use RDLs to re-route signal/power connections to sensor edges
- Explore processing on thin and large area sensors
- Plating of contact pads for alternative interconnection techniques

Large area modules with minimum material for routing and interconnection

Wafer level RDLs (PacTech.com)





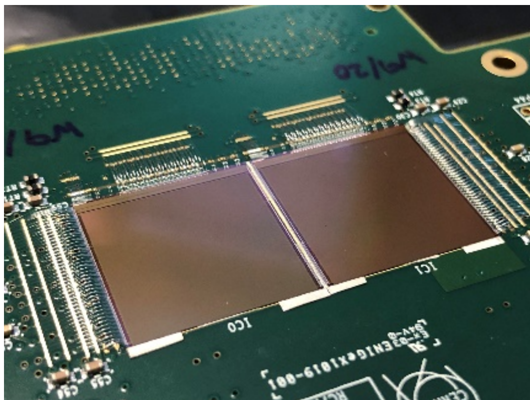
CMOS wafer scale pixel sensor (RAL)

Interconnection

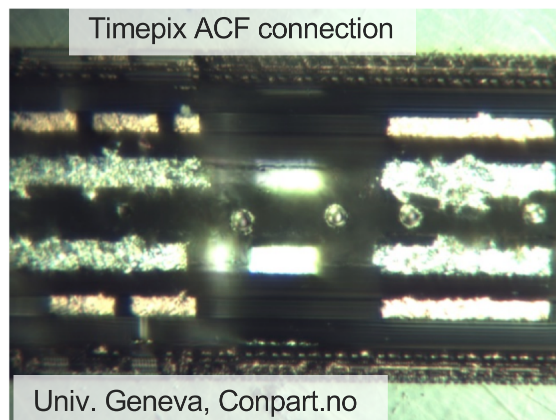
Interconnection techniques

- Chip-2-chip connections – exploring known and alternative interconnection techniques (wire bonding, ACF, Cu-studs,..) to build large area modules with low material budget
- Anisotropic Conductive Film (ACF) as interconnection alternative to fine pitch bump bonding

Chip-2-chip interconnections for large area CMOS modules – chip-2-sensor interconnection for hybrid pixels

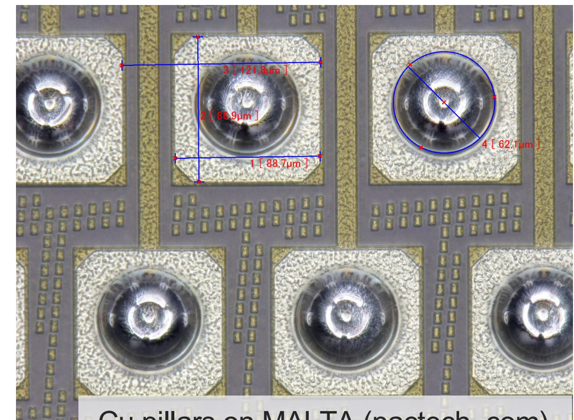


Chi2chip data transfer via wire bond



Timepix ACF connection

Univ. Geneva, Conpart.no



Cu pillars on MALTA (pactech..com)

Integration

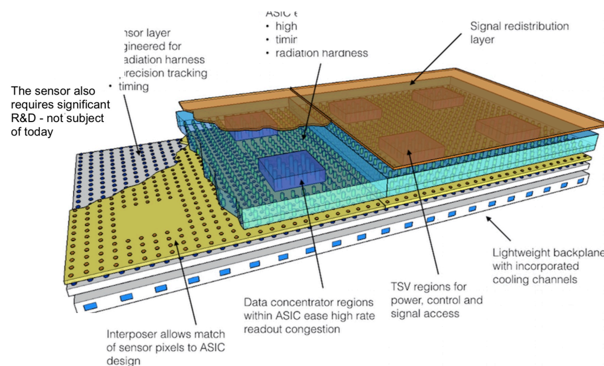
Glue studies

- Glue studies for flex-silicon connections
- Collect available information from the community and extend where needed by testing new glues

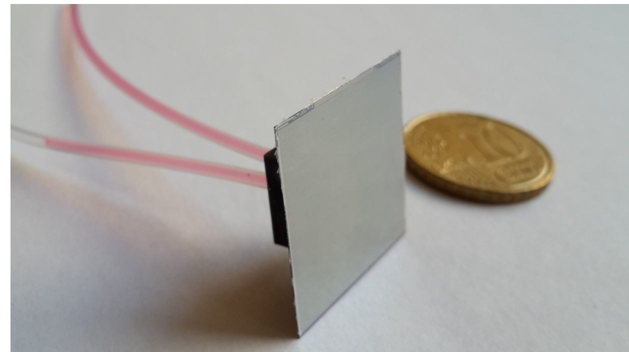
Integration

- Combine electrical and/or cooling/mechanical structures (e.g. embedded channels in silicon sensors, embedding of sensors, …) to build highly integrated modules in a second step - depends also on other WP

Knowledge base for glues – highly integrated modules combining electrical and mechanical/cooling aspects



Embedded microchannels in CMOS (EP-DT)



WP 1.3 Modules

Foreseen manpower:

Fellows: 0.5 (2020) – 1 (2021) – 1.5 (2022) – 1.5 (2023) – 1 (2024)

Proposed supervisors: Petra Riedler, Dominik Dannheim

Doctorals: 1 (2020) – 1.5 (2021) – 2 (2022) – 2 (2023) – 1.5 (2024)

Proposed supervisors: Victor Coco, Dominik Dannheim, Magnus Mager, Heinz Pernegger, Petra Riedler

Doctorals partially funded assuming contributions from other sources (AIDA++, nat. programs, ...)

Infrastructure:

Set up small clean area in existing DT area to house basic equipment: table top grinder and scriber for large wafer sizes, visual inspection microscope, Spreading-Resistance-Profile (SRP) measurement system

Collaborations and industrial partners

Build on existing relations with institutes and industrial partners

Kick-off meeting end January 2020

Plan to have monthly meetings as platform of exchange