On MAPS-On-Diamond sensors and their potential as innovative devices

Servoli Leonello [1]

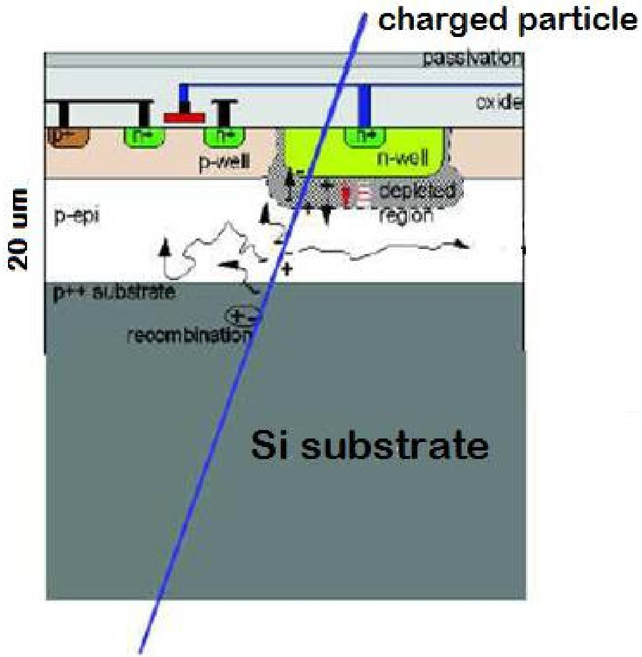
Alunni Solestizi L.[1], Kanxheri K.[1], Lagomarsino S.[2], Morozzi A.[1,3], Passeri D.[1,3], Sciortino S.[2,4].

[1] Istituto Nazionale di Fisica Nucleare – Sezione Perugia, Perugia, Italy
[2] Istituto Nazionale di Fisica Nucleare, Sezione di Firenze, Sesto Fiorentino, Italy
[3] Dipartimento di Ingegneria , Univ. Perugia, Perugia, Italy
[4] Dipartimento di Fisica e Astronomia, Universita di Firenze, Sesto Fiorentino, Italy

Outline

- Silicon-On-Diamond Concept
- MAPS-On-Diamond (MAPSOD) Prototypes
- MAPSOD Results for ionizing radiation detection
- Evaluation of potential performances
- Conclusions

CMOS process for Monolithic Sensors

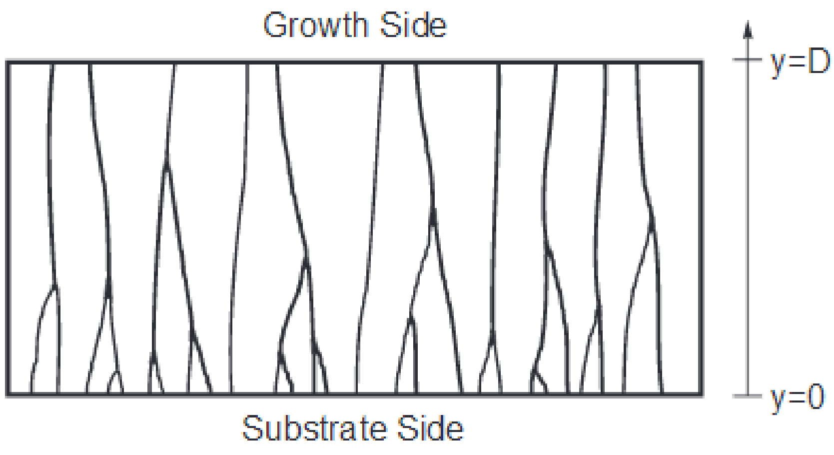


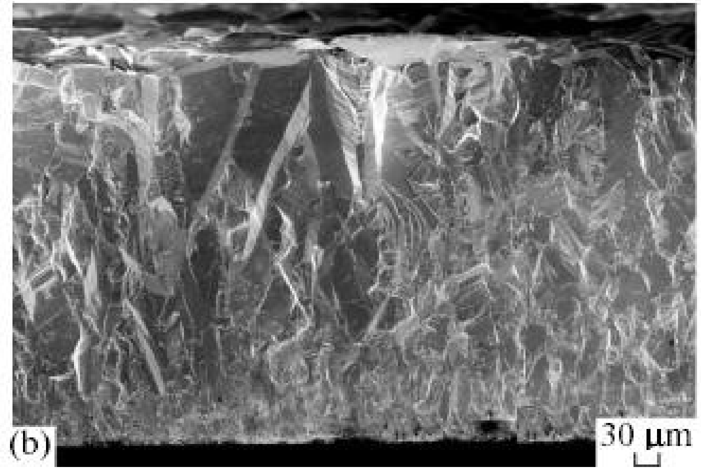
- *CMOS structures are implemented in a thin layer (~ μm)*
- *Sensitive layer thickness varies from 1-2 to 10-15 μm*
- *Silicon substrate used for mechanical support and handling*

For charged radiation detection applications:

- ***Charged particle detection in CMOS devices could use only e-h generated in thin epitaxial layer → small signal → needed small noise***
- ***CMOS devices suffer from radiation damage.***

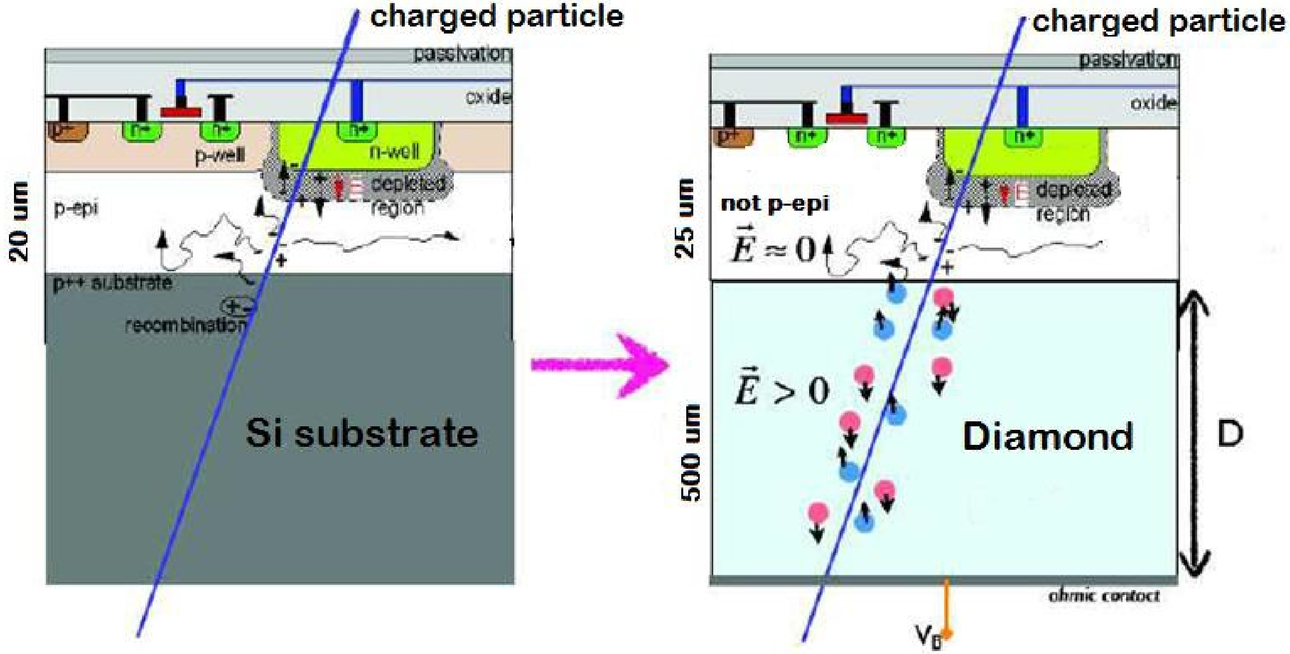
Silicon-On-Diamond Concept





- ***Diamond substrates are very radiation resistant***
- ***Human tissue equivalence (dosimetry)***
- ***Biocompatible substrate***
- ***Limited surface, (25x25 mm for pcCVD , 5x5 mm for scCVD)***
- ***Higher bangap →less e-h creation***
- ***For charge collection applications it's not easy to pixellize substrate surface.***

Silicon-On-Diamond Concept



- ***Substitute silicon bulk substrate with diamond substrate, with polarization.***
- ***Charged particle would create e-h pairs in both silicon and diamond.***
- ***Charges would cross the Si-Diamond interface and will be collected by instrumented CMOS part in silicon.***

→ ***How to “glue” together Si and Diamond?***

→ ***How to ensure CMOS structures integrity?***

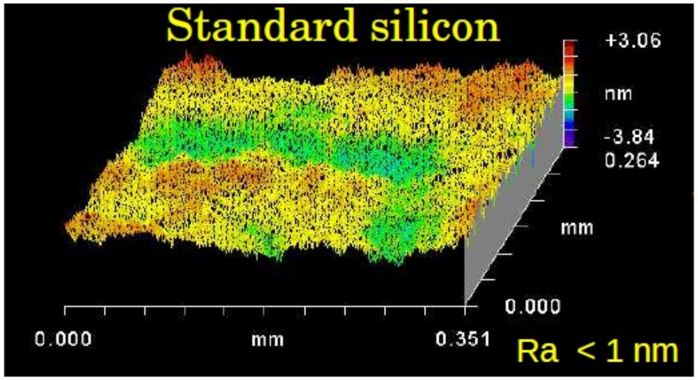
→ ***How to bias diamond without damaging CMOS?***

Si-diamond Laser Bonding Process

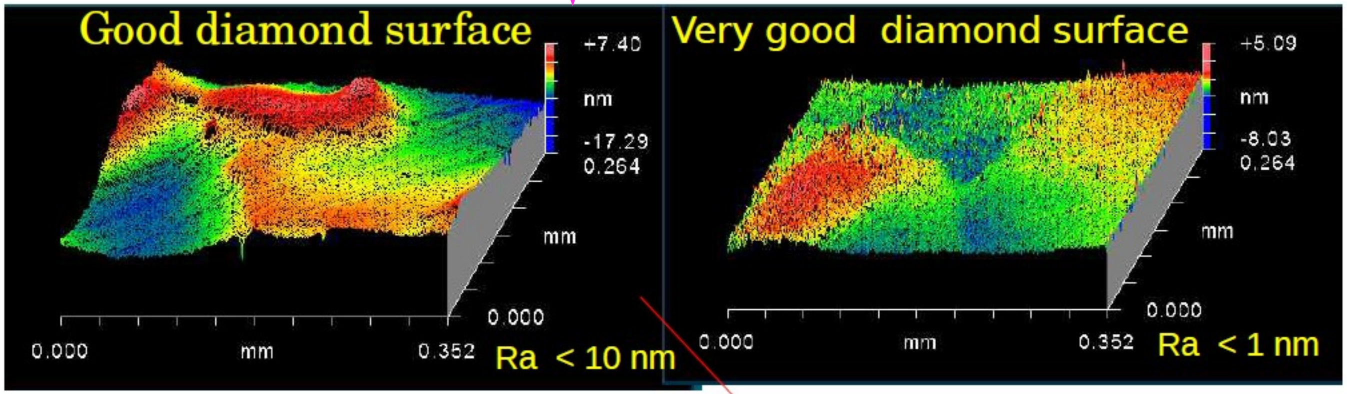
Bonding procedure:

→ **thin down silicon to few micrometers leaving ony a bit more than CMOS thickness**

→ **levigate silicon surface to few nm roughness**



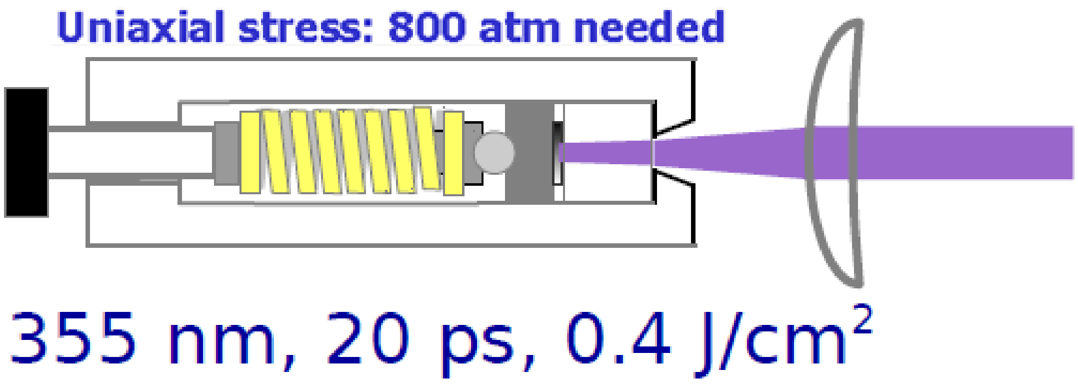
→ **levigate diamond surface to few nm**



Si-diamond Laser Bonding Process

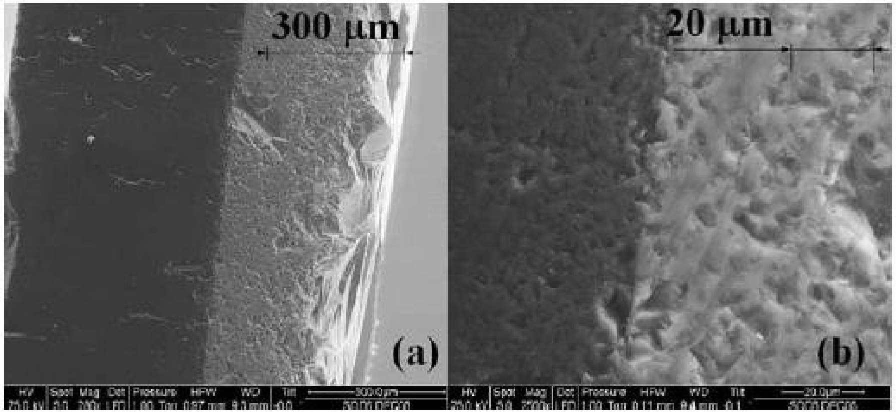
→ **press with 800 atm uniaxial stress the two surfaces**

→ **use pulsed laser (355 nm) entering from diamond side to deposit energy on the silicon surface**



→ **absorbed energy will flow back from silicon to diamond and will modify lattice and create bonds between the two materials**

→ **interface has a thickness of 80-100 nm**



Lagomarsino S., "Silicon-on-diamond material by pulsed laser technique' App. Phys. Lett. 96, 031901, 2010 , *doi:10.1063/1.3291043*

(INFN & UNIFI & LENS)

MAPS-ON-Diamond

Which kind of CMOS device would we use ?

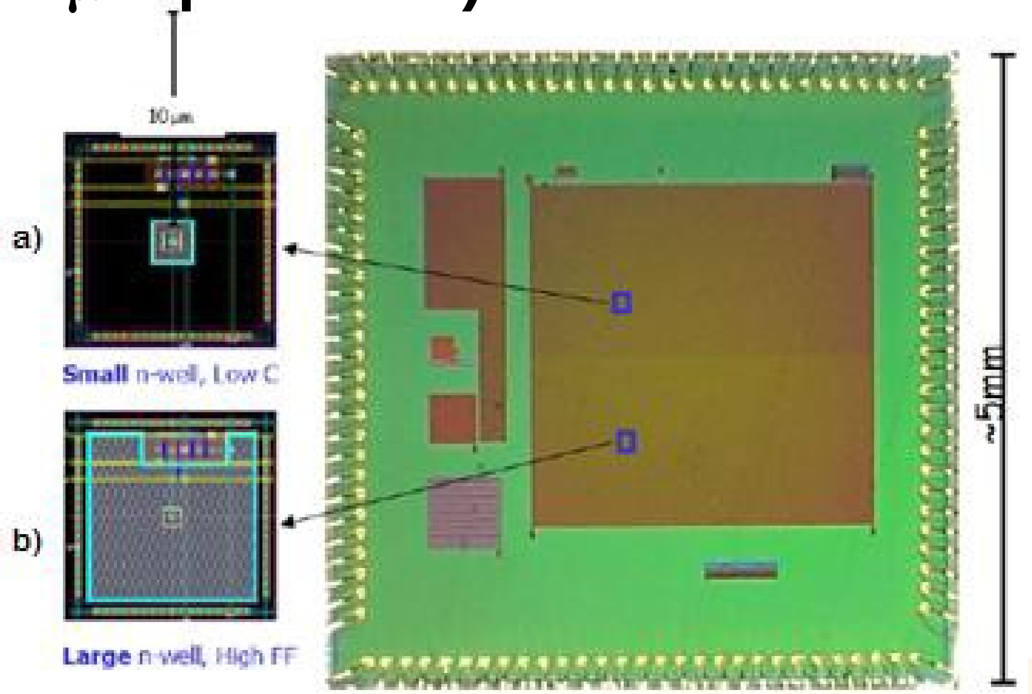
→ **Monolithic Active Pixel Sensors   (MAPS)**

→ **high pixel density (down to 2x2 μm pixel size)**

→ **small thickness of sensitive layer (~ 2 μm for epitaxial devices)**

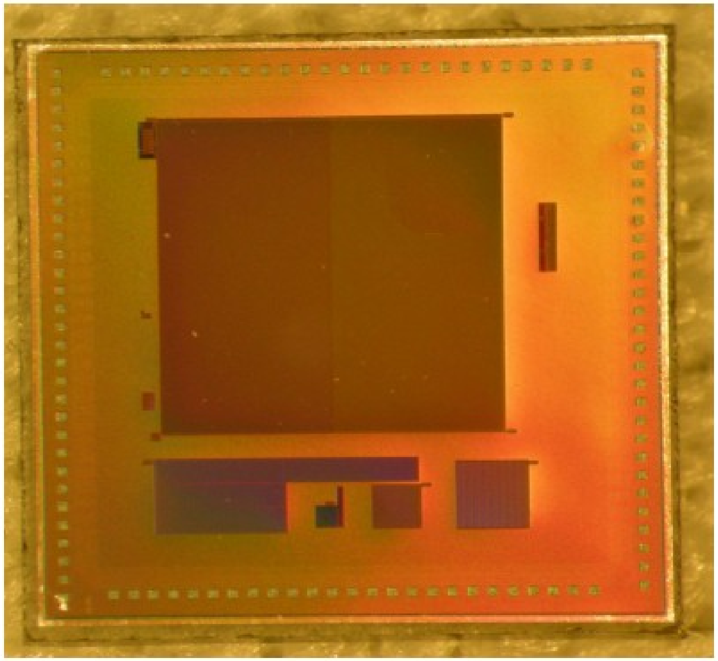
→ **high efficiency for charged particle detection (~ 100%)**

→ **RAPS03 device, 10x10 μm, 2 x 32768 pixels** ***(INFN & UNIPG)***



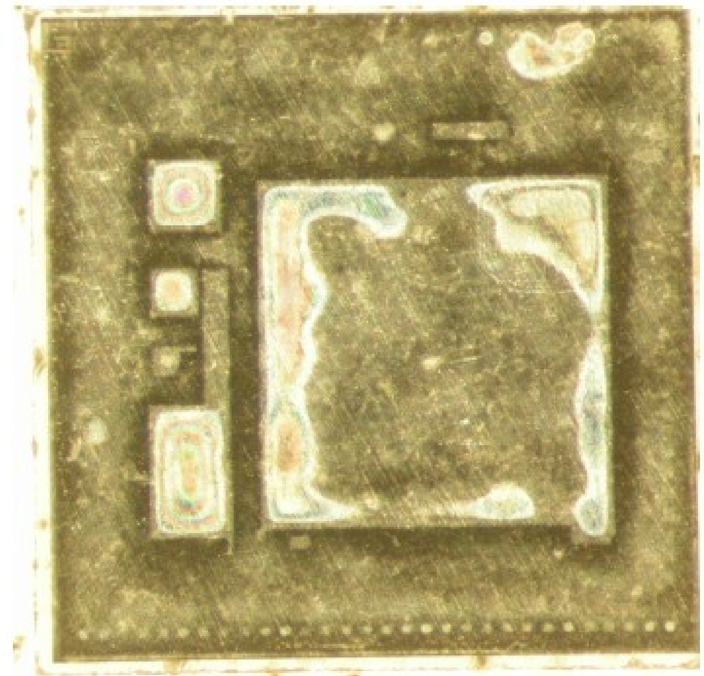
MAPS-ON-Diamond

Front view (silicon)



Si: 25 μm thickness
Diamond: 500 μm thickness

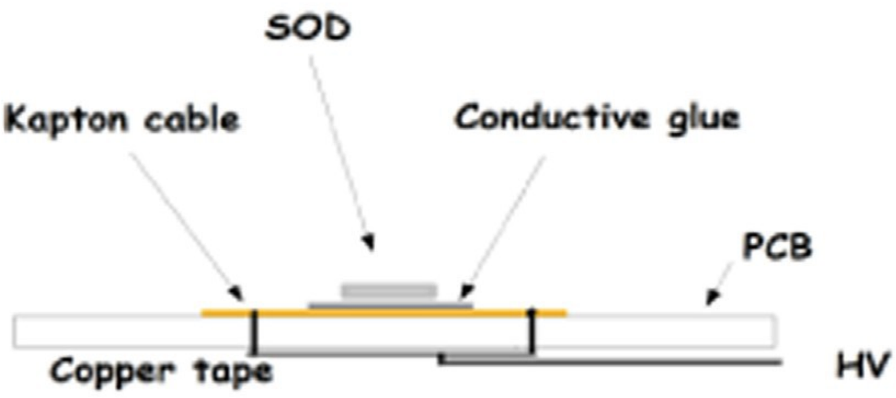
Rear view (diamond)



Adhesion not uniform.

MAPS-ON-Diamond

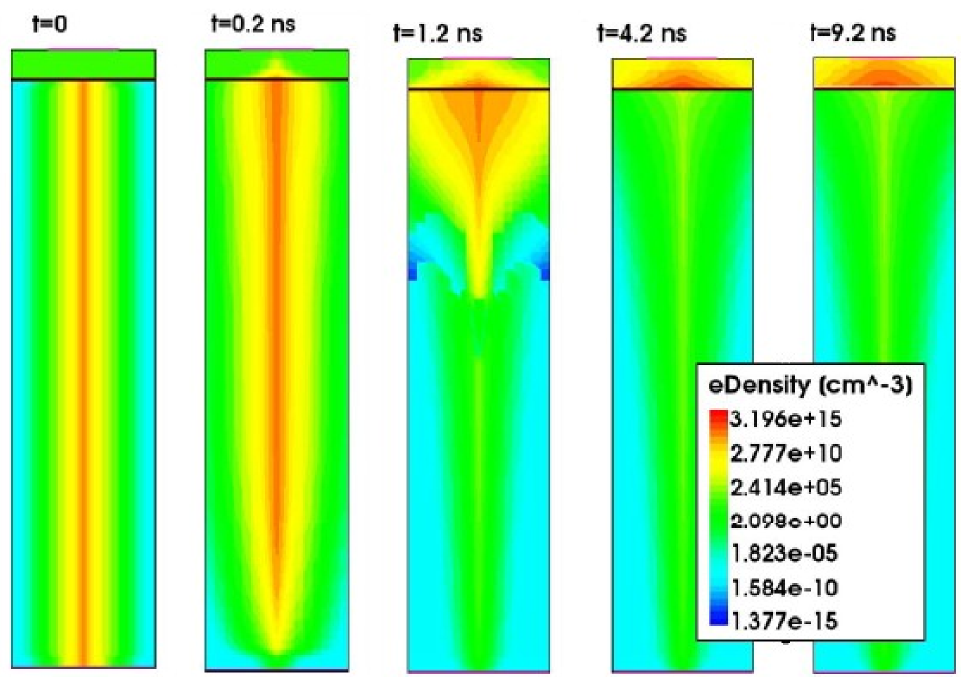
Bias scheme



Reference HV: same as CMOS reference.

HV Bias: negative to push electron in diamond toward silicon where photodiodes would collect them.

Simulation to check how much voltage would drop across diamond (almost all) and time evolution of generated electrons.

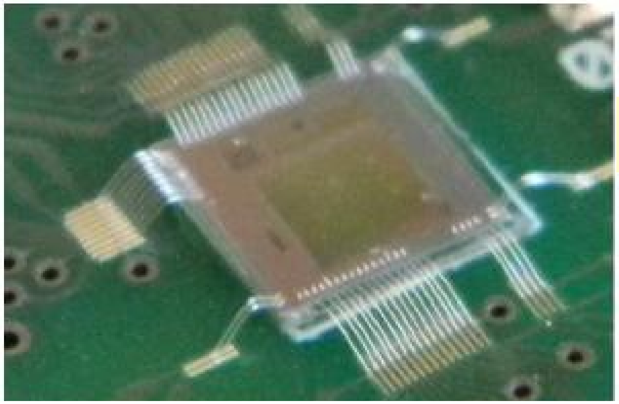


D. Passeri et al., Simulation and Test of Silicon-on-Diamond Sensors for Particle Detection. 10.1109/IWASI.2015.7184970 (2015)

CMOS circuits integrity

→ **Is bonding procedure damaging the CMOS properties?**

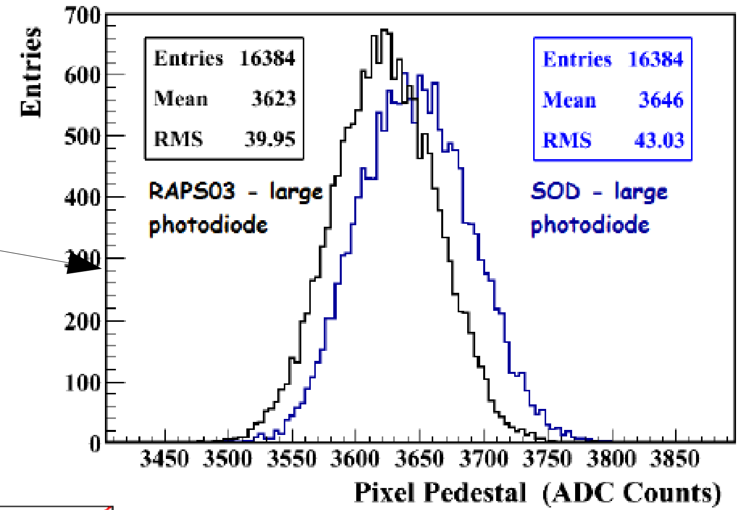
(pressure, energy absorption, lattice deformation….)

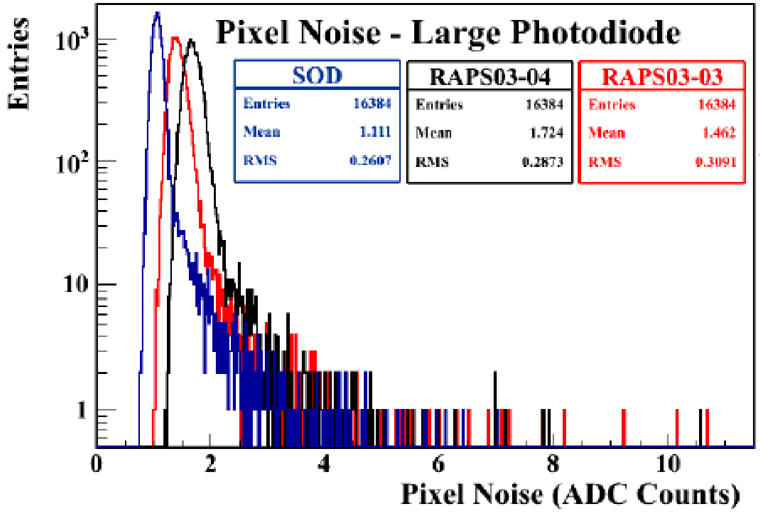


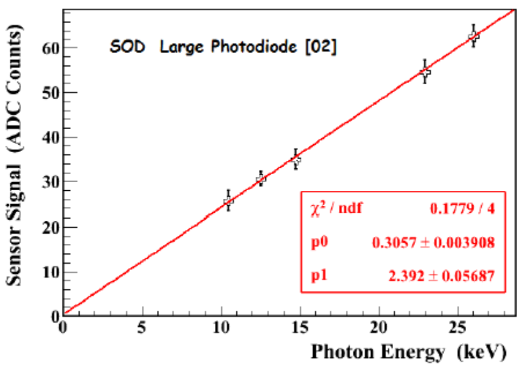
L. Servoli et al., Characterization of Silicon-On-Diamond chip with ionizing radiation. JINST 9 C04019 (2014)

Digital section working.

Same single pixel behaviour in absence of external stimula.







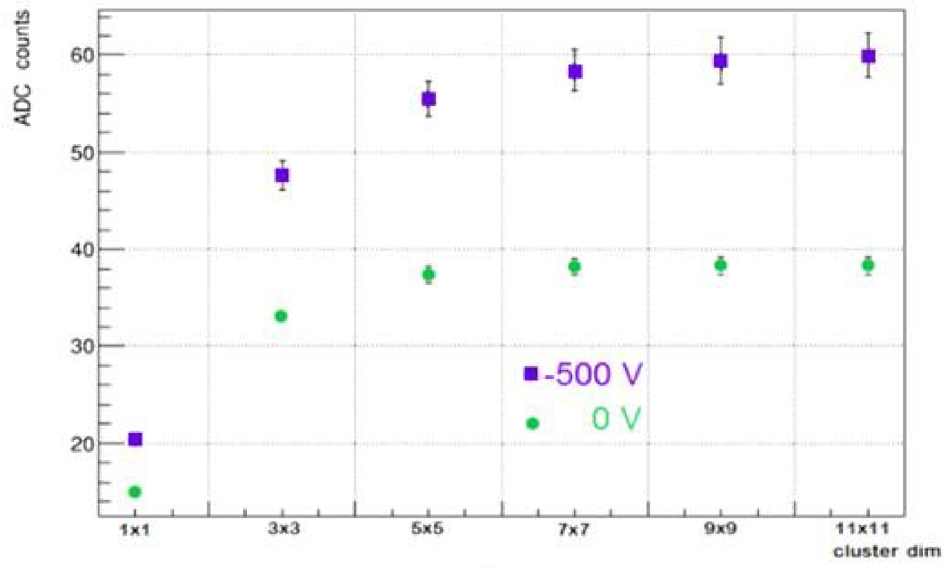
Same coefficients for X-ray fluorescence calibration procedure:

SOD: 2.39 ± 0.06 ADC/keV;

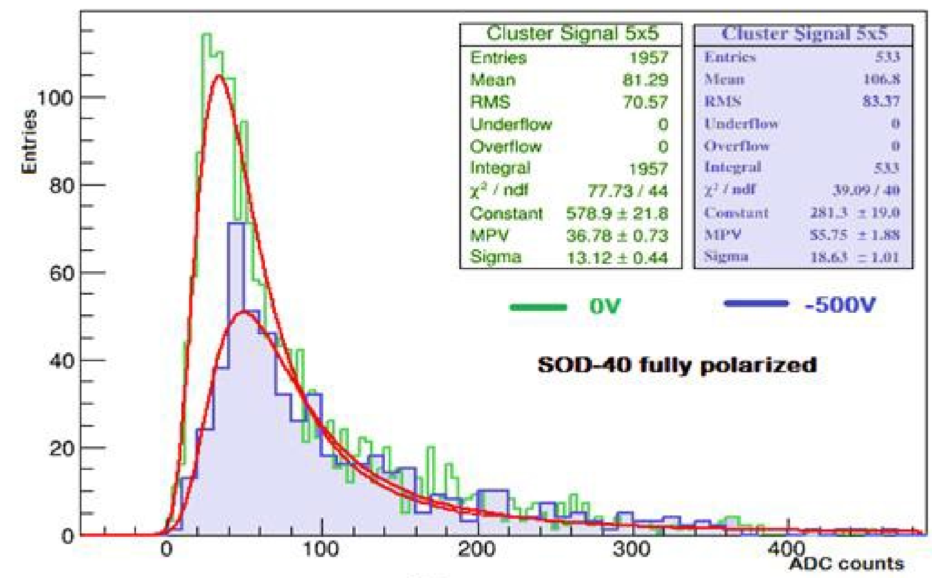
RAPS03: 2.48 ± 0.05 ADC/keV;

Ionizing radiation detection

We observed the diamond ionization contribution to signal collected by CMOS when diamond is polarized.



a)



b)

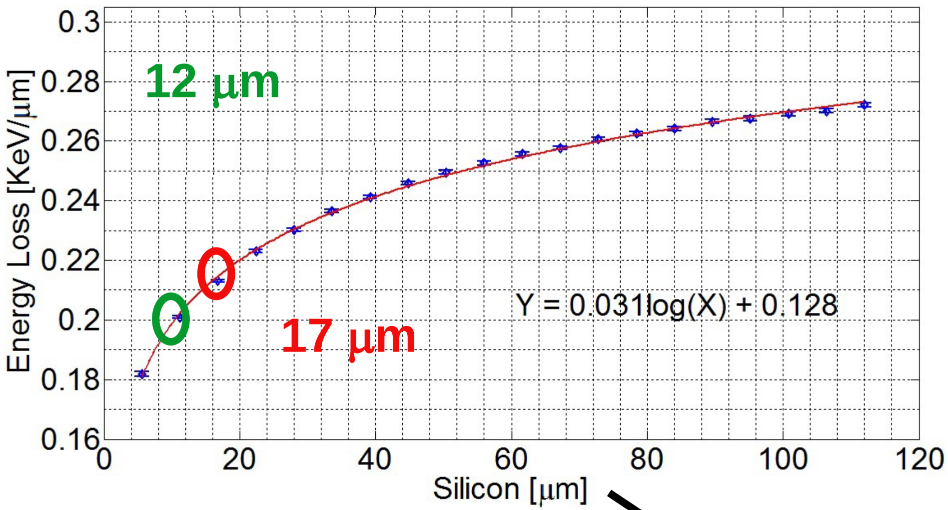
K. Kanxheri et al., First results on biased CMOS MAPs-on-diamond devices, Nucl. Instr. and Meth. in Physic s Research A 796 (2015) 47–50

Ratio = $S_{diamond}$ / S_{total} = $S_{diamond}$ /($S_{diamond}$ + $S_{silicon}$) = 20/60 = 33%

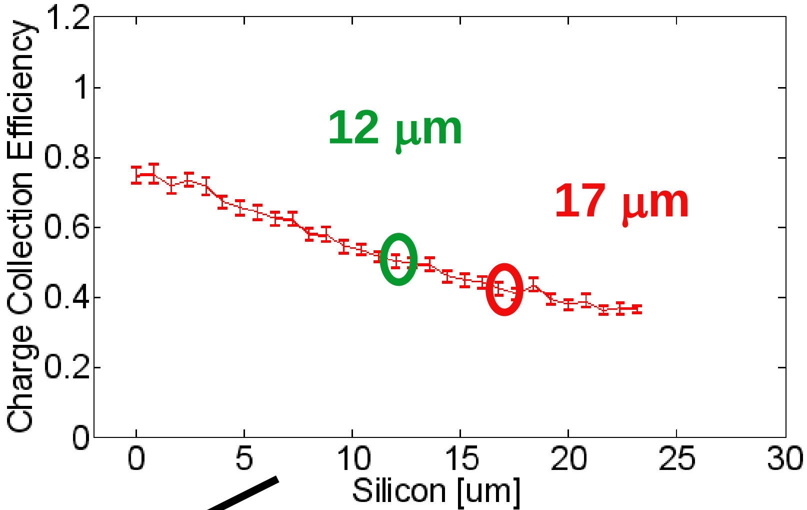
(in principle it should be more but we have inefficiencies due most likely to Si-diamond interface defects)

Silicon signal vs thickness

Number of e-h pairs created in silicon by MIP



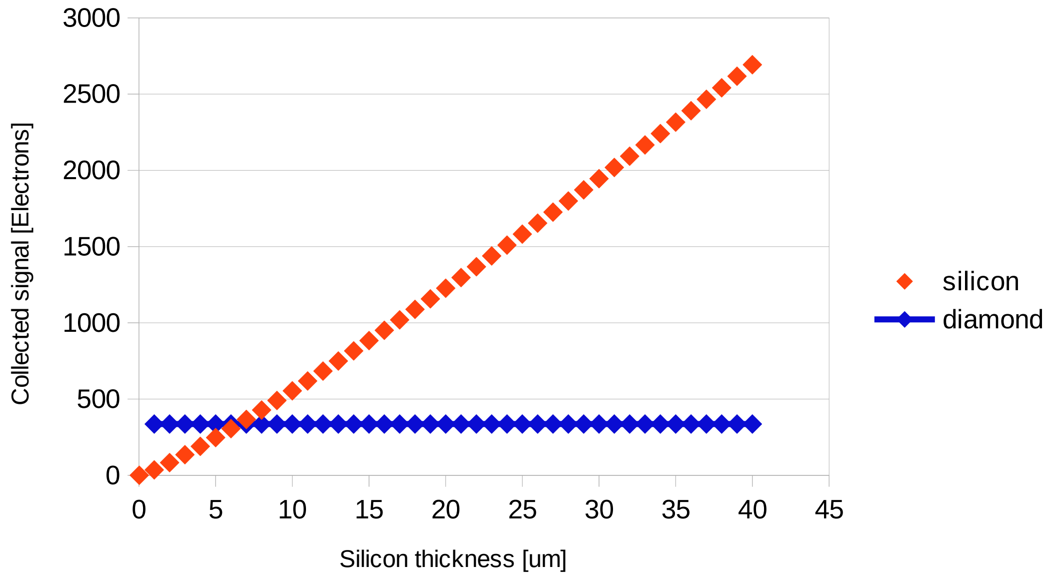
MAPS Charge Collection Efficiency vs depth from photodiode

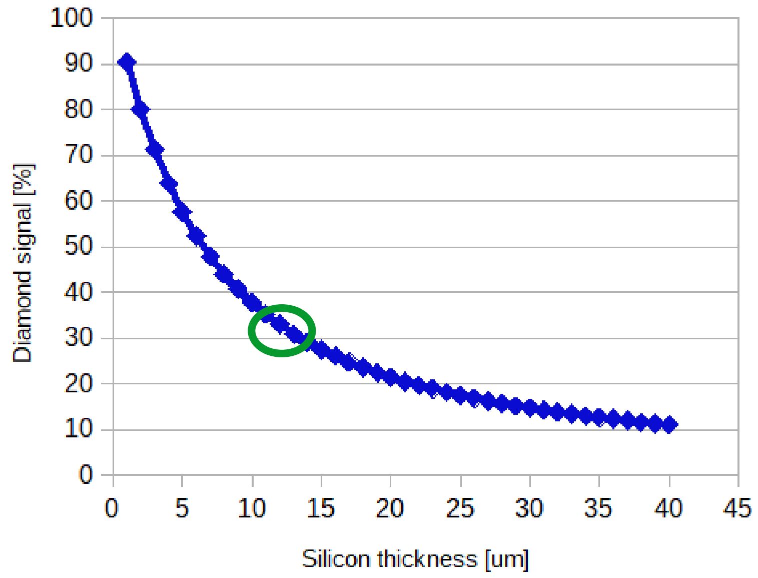


Total silicon signal

Calibration factor: [keV/ADC]

Signal on Silicon vs Diamond





To minimize silicon influence → reduce thickness as much as possible.

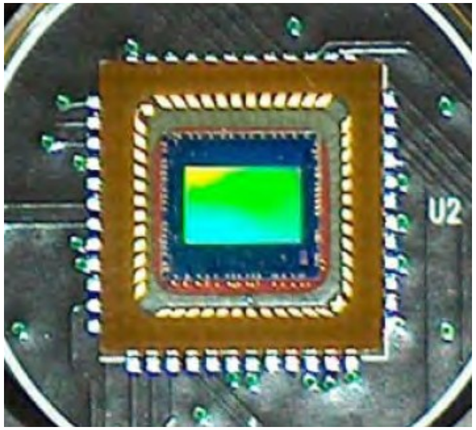
But: mechanical stability and CMOS layer thickness are two limits

→ very difficult to reach 2μm , impossible to go below 1 μm.

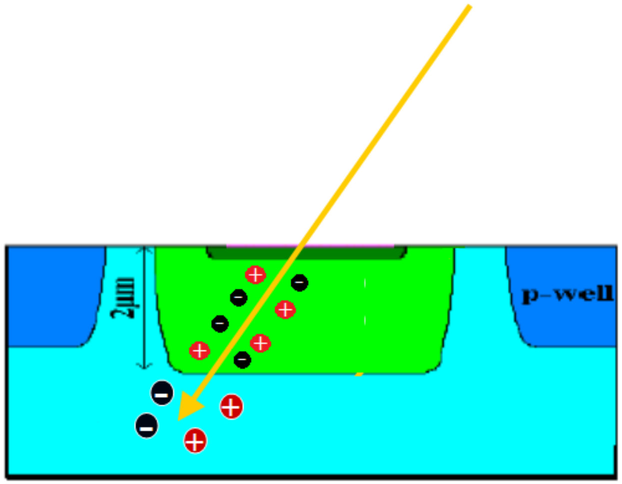
12 μm is the limit we have reached → Diamond signal < 50%.

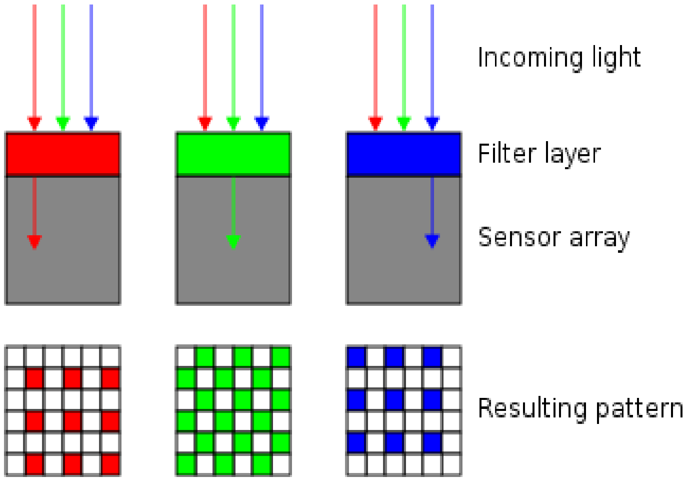
MAPSOD: Possible evolution….

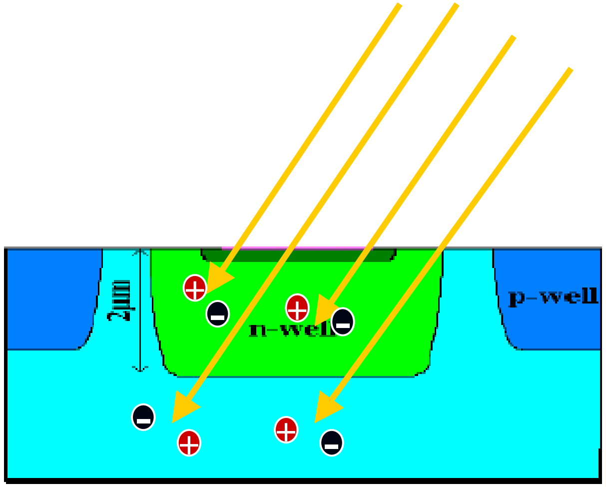
Use of commercial CMOS Imagers



- → *high quality device*
- → *small pixel size (2 µm or less)*
- → *wider area (5.5 x 6.5 mm for 10 Mpixel device)*
- → *investigation to use backside illuminated devices*
- → *low cost*





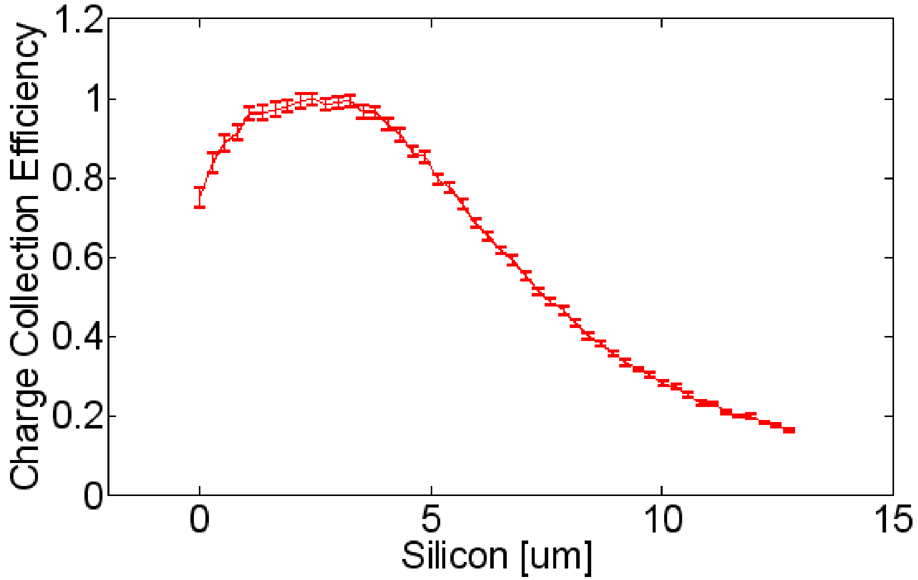


MAPSOD: Possible evolution….

Epitaxial layer →
better collection efficiency

→ 100% up to few µm

(4.5 µm nominal thickness)

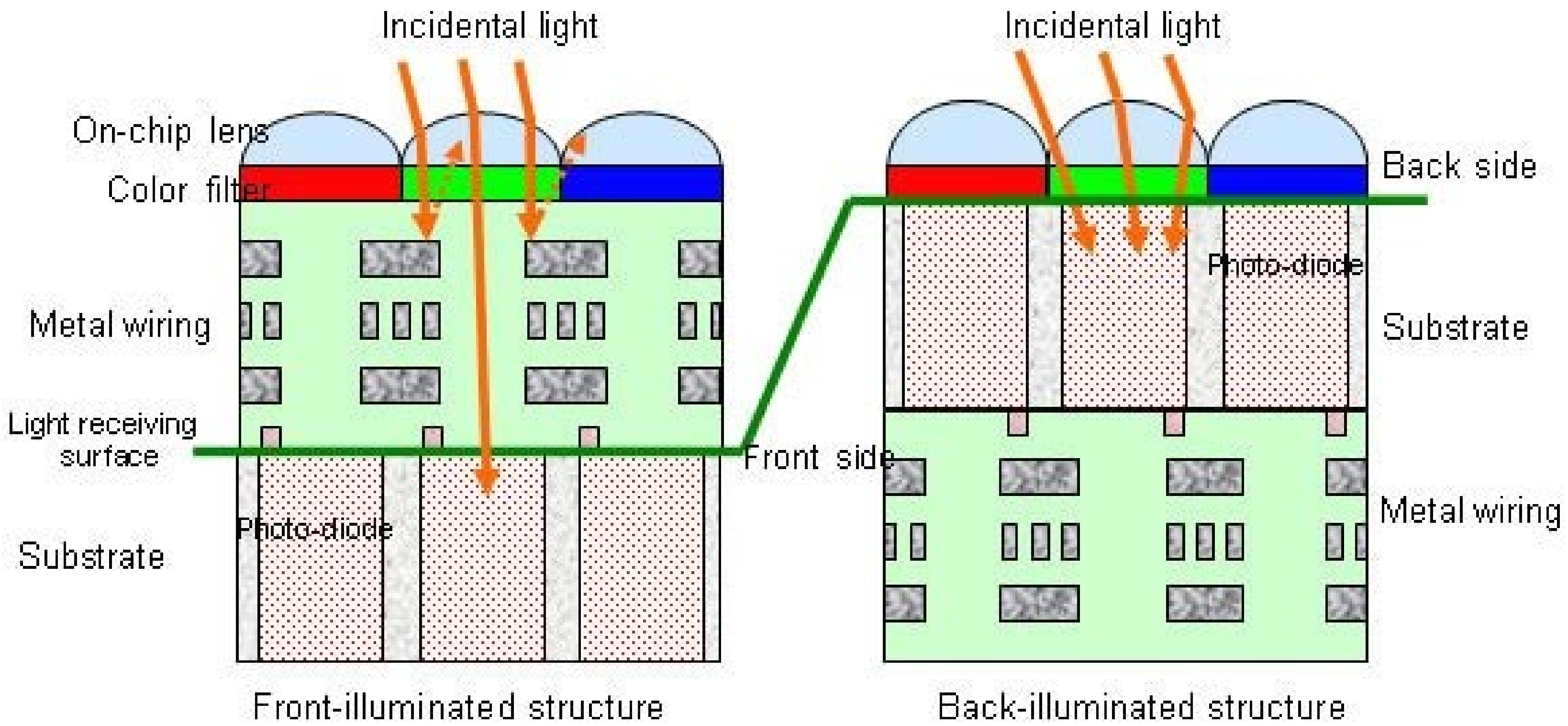


For one such device (MT9V011) , that has a collection range up to 38.000 electrons, if we stop @ 4 µm we have ~ 740 collected electrons in silicon (noise ~40 electrons)

→ a diamond signal would be 63% and S/N ~ 50.

Backside Illuminated imagers….

→ ***Back Side Illuminated devices***

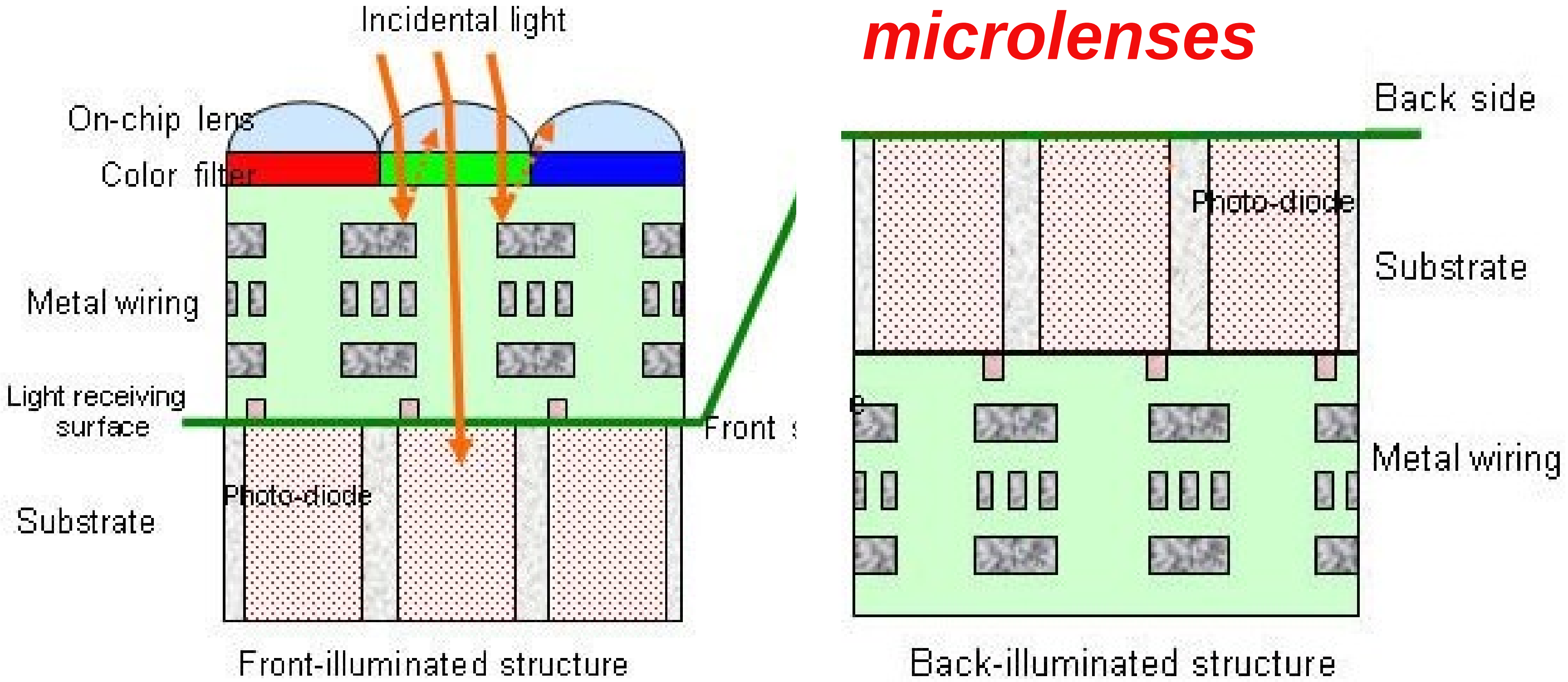


→ ***Monochromatic device (no μlenses, no filters) is a possibility.***

Backside Illuminated imagers….

→ ***Back Side Illuminated devices***

No filters, No microlenses



→ ***Discussion with producers to obtain such devices***

Ionizing radiation detection

For these devices, thickness could be 2.5 *µm.*

Using same values for diamond signal, and a guess of 90% average charge collection efficiency → 200 electrons in silicon

Single pixel noise scales with volume → pixel of 2x2x2.5 = 10 *µm*

→ (5.6 x 5.6 x 4.5) μm^3/(2 x 2 x 2.5) μm^3 = 141/10 = 14

→ SPN = 38 electrons / 14 = 3 electrons = 1 ADC (@ 33 ms)

Hence $S_{diamond}$ / ($S_{diamond}$ + $S_{silicon}$) = 2000 / (2000 + 200) = 91% .

S/N = 2200/3 = 730 !!!! (optimistic…> 100 feasible)

More issues…..

Cluster size:

- **using 10 *µm* pixel size, the size is essentially the one observed with only silicon (0 V bias for diamond) → fews pixels**
- **for MAPS of 2 *µm pixel size*, the cluster size remains confined to few *µm* radius.**

Radiation resistance:

- **Polycrystal CVD diamond is very radiation resistant;**
- **Few *µm* of silicon sensitive substrate should not produce a lot of dark current;**
- **for technology node < 100 nm also CMOS part should be radiation resistant;**
- **For MT9V011 device (120 nm node): device still working with fluence up to 10^{13} p/cm^2 with a shift of single pixel pedestal and a moderate increase of noise.**

Conclusions

- ***MAPS-On-Diamond devices allow us to instrument a diamond substrate with highly pixellized CMOS readout***
- ***CMOS circuits show no damage after the bonding procedure***
- ***Charge created in diamond part produces a signal on CMOS***
- ***To increase S/N due to diamond and reduce silicon contribution, very thin MAPS devices (BSI) are needed.***