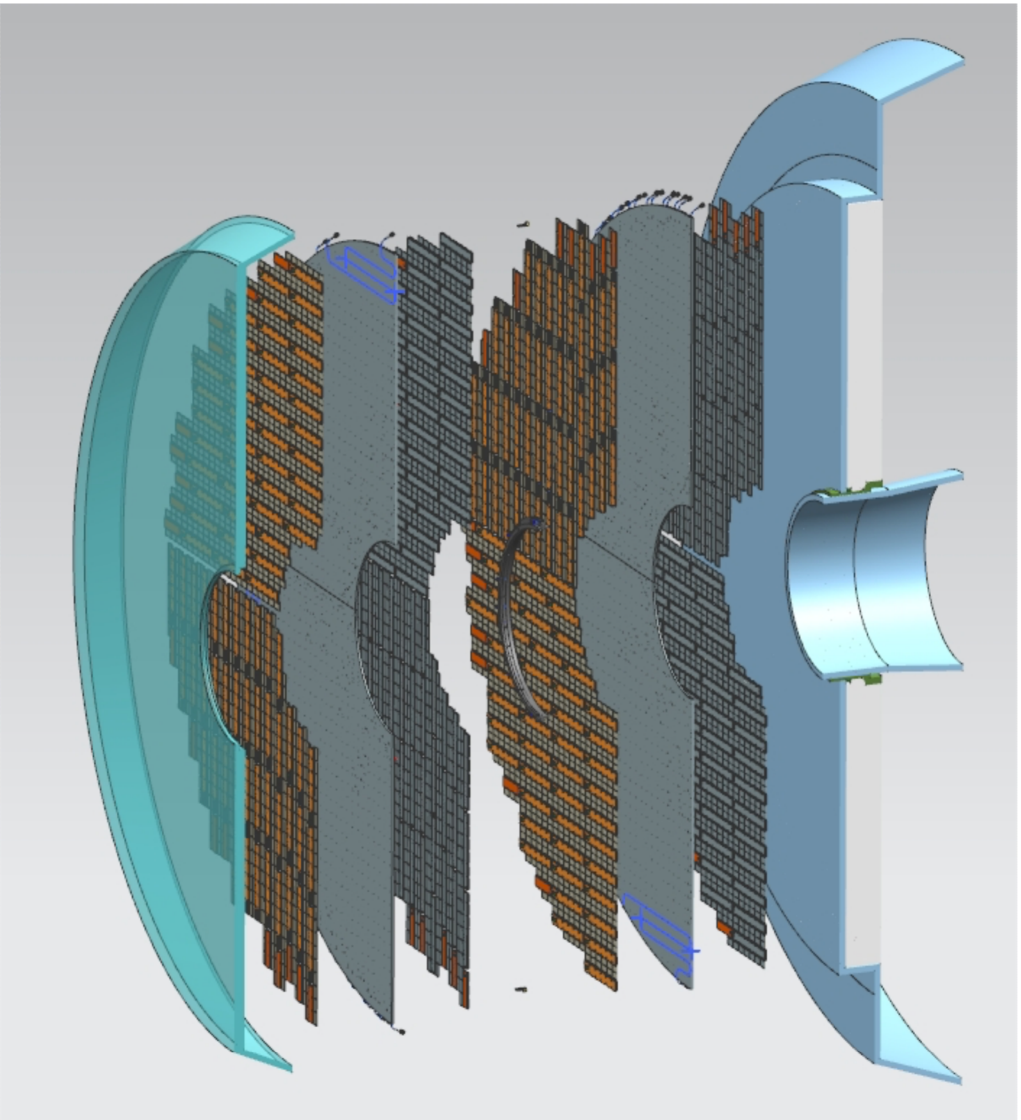


# Precision Timing with Low Gain Avalanche Detectors in the CMS MTD Endcap Timing Layer

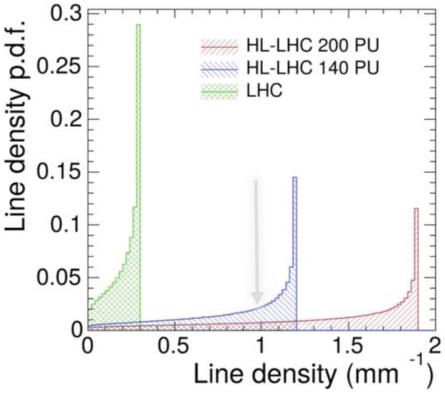
**Marco Costa**
INFN & University of Torino
On behalf of CMS Collaboration

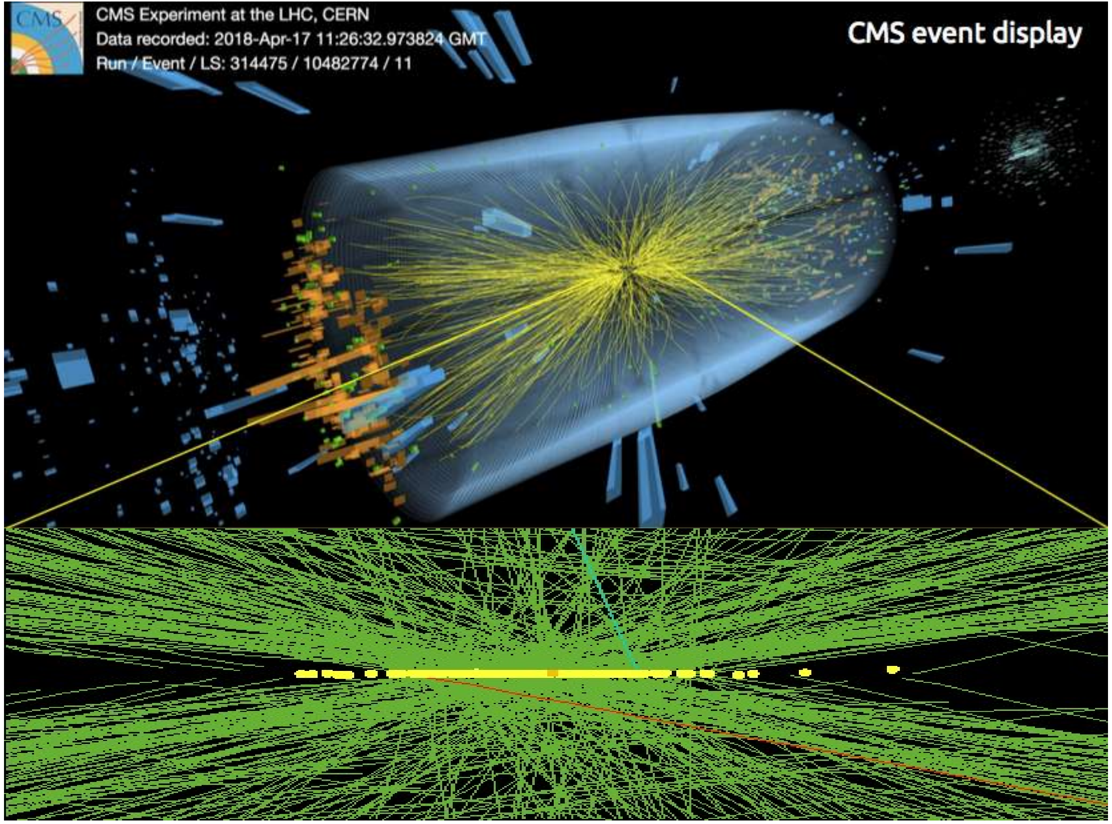
IPRD19- 15th Topical Seminar on Innovative Particle and Radiation Detectors – Siena – October 2019

# The High-Lumi LHC challenge

| | Inst. Lumi (cm$^{-2}$s$^{-1}$) | Peak pileup (PU) |
|---|---|---|
| **LHC** | 1.7 x $10^{34}$ | 60 |
| **HL-LHC** | 5-7.5 x $10^{34}$ | 140-200 |

- Up to **5x higher vertex density**
- **Track-vertex compatibility cut** is @ 1mm



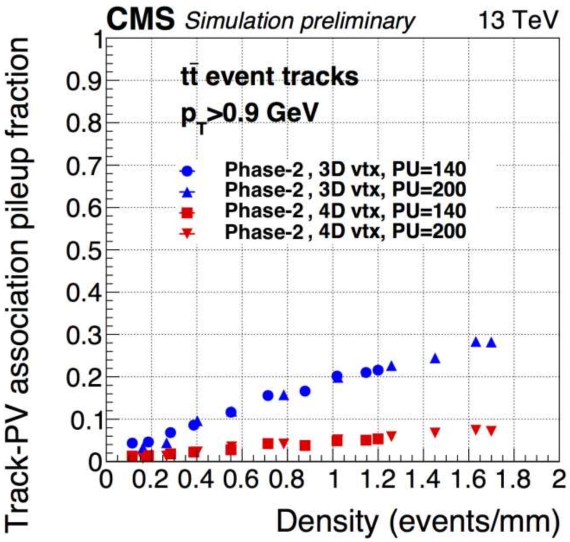


**At HL-LHC: without extra info on the track 15-20% luminosity loss**

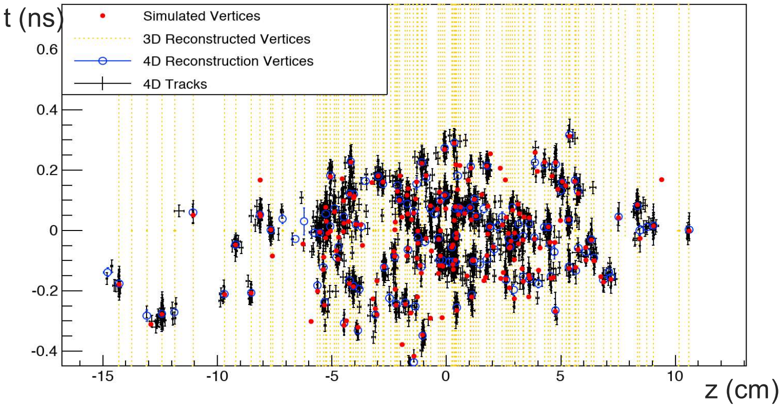
# Timing resolution requirements

***HL-LHC:***

- According to CMS simulations:
- $\langle t_{vertex} \rangle_{RMS}$= **153 ps**
- Average distance between two vertexes: **500 um**
- Fraction of overlapping vertexes: **15-20%**
- Of those events, a large fraction will have significant degradation of the quality of reconstruction



200 pileup interactions in 4D space



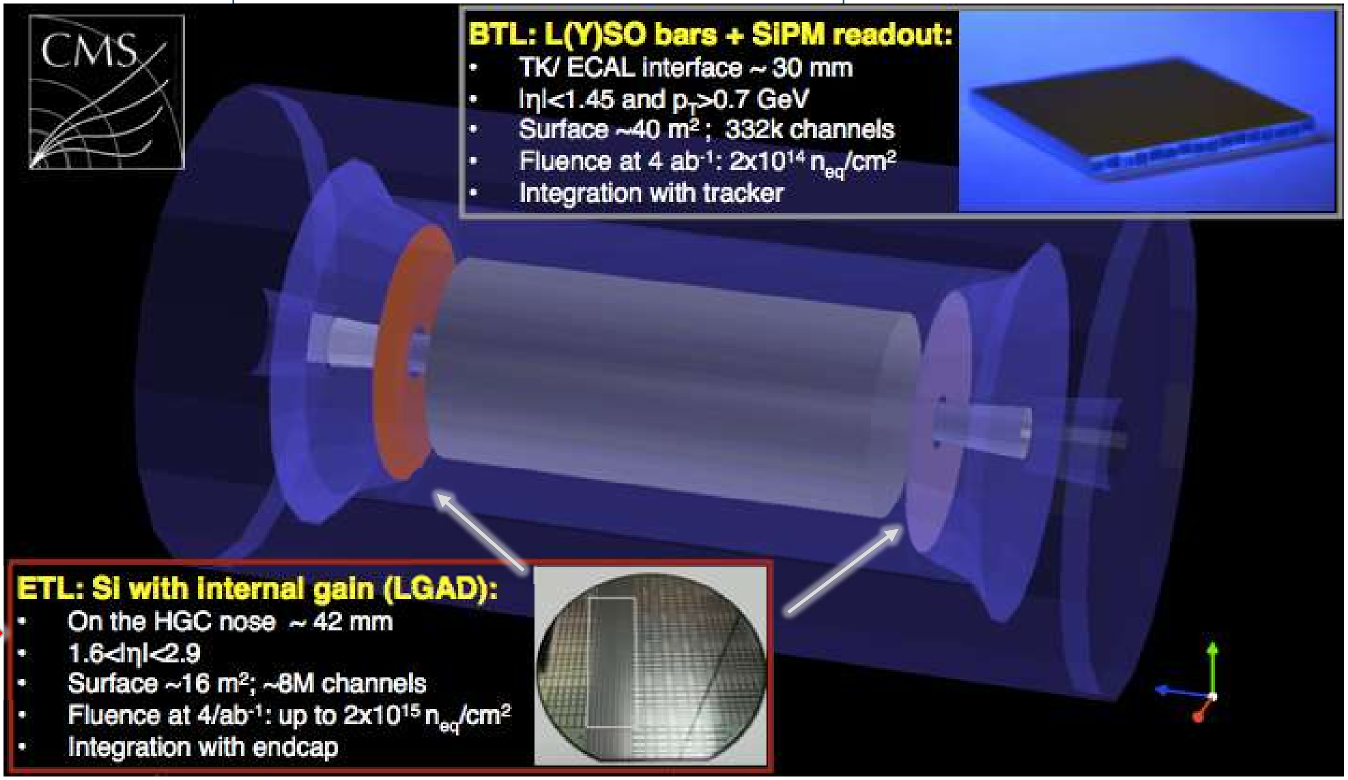
With **30ps time resolution**, instances of vertex merging are reduced from 15% in space to 1% in space-time

**Mip Timing Detector** in CMS to consolidate particle flow performance at 140PU events, and extend it to 200PU

# CMS MIP Timing Detector

A precise timing detector can be used for Particle Identification or for pile-up suppression

30-40 ps timestamp for every track



**BTL: L(Y)SO bars + SiPM readout:**

- TK/ ECAL interface ~ 30 mm
- $|\eta|<1.45$ and $p_T>0.7$ GeV
- Surface ~40 m²; 332k channels
- Fluence at 4 ab$^{-1}$: $2\text{x}10^{14}$ $n_{eq}/cm^2$
- Integration with tracker

**ETL: Si with internal gain (LGAD):**

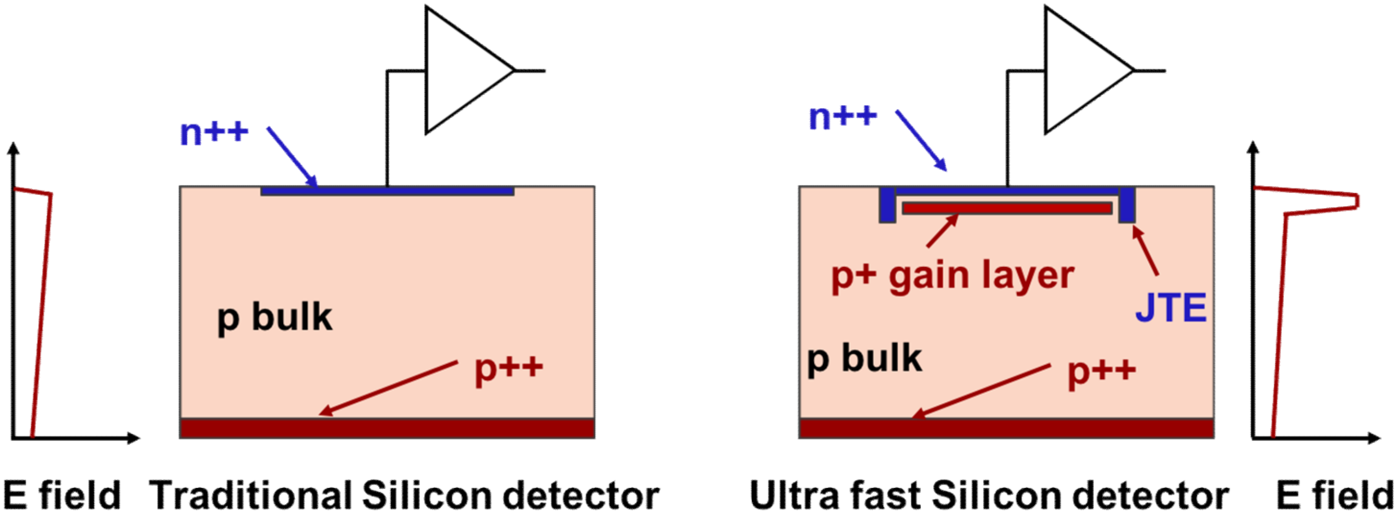
- On the HGC nose ~ 42 mm
- $1.6<|\eta|<2.9$
- Surface ~16 m²; ~8M channels
- Fluence at 4/ab$^{-1}$: up to $2\text{x}10^{15}$ $n_{eq}/cm^2$
- Integration with endcap

Endcap
Timing
Layer

**MTD TDR Fully Approved https://twiki.cern.ch/twiki/pub/CMS/MTDTechnicalDesignReport/MTD_TDR_final_20191002.pdf**

# ETL instrumented with Ultra Fast Silicon Detectors

Ultra Fast Silicon Detectors (UFSDs) are Low Gain Avalanche Diodes (LGADs) optimized for timing employing a thin multiplication layer to increase the output signal at the passage of a particle of a factor ~ 10 - 20

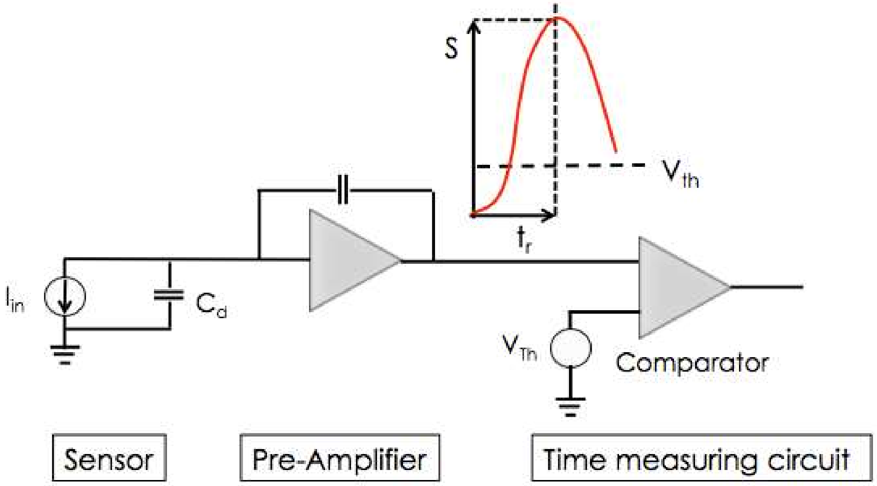


The low-gain mechanism, obtained with a moderately doped p-implant, is the defining feature of the design.

The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

# Silicon time-tagging detector

(a simplified view)



**Time is set when the signal crosses the comparator threshold**

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning.

**Strong interplay between sensor and electronics**

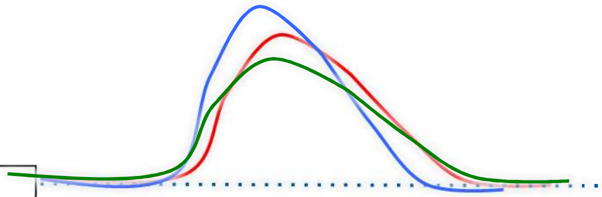
# Good time resolution needs very uniform signals

Signal shape is determined by Ramo’s Theorem:

$$i \propto q v E_w$$

**Drift velocity**

**Weighting field**



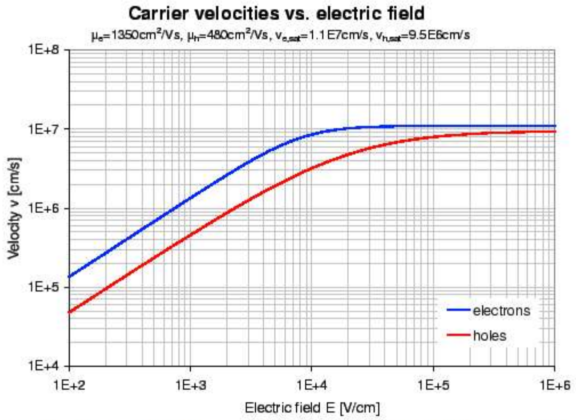
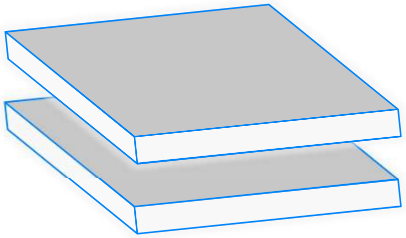


**Figure:** Electron and hole velocities vs. the electric field strength in silicon.

**The key to good timing is the uniformity of signals:**

Drift velocity and Weighting field need to be as uniform as possibl

**Basic rule:** **parallel plate geometry**

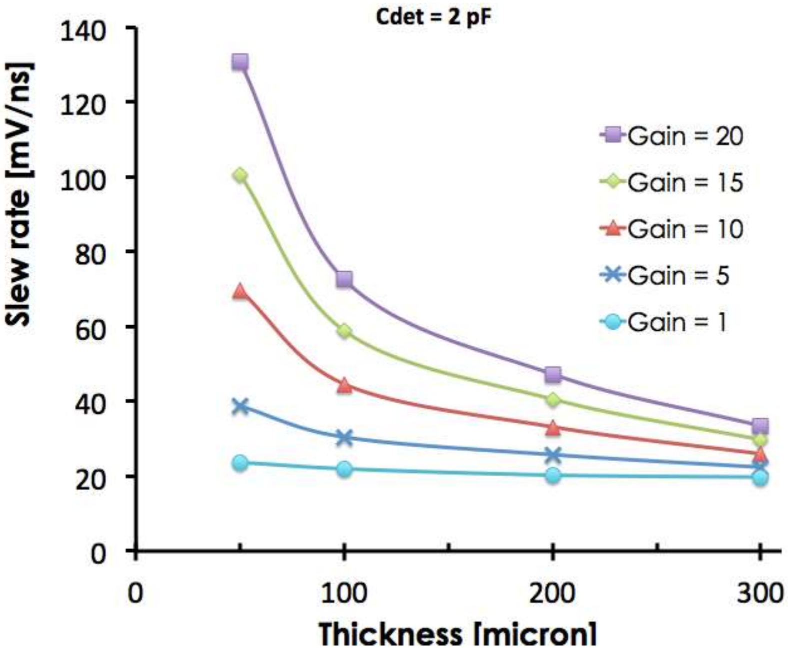


# Gain current vs Initial current

$$\frac{di_{gain}}{i} \propto \frac{dN_{Gain} q v_{sat} \frac{k}{d}}{k q v_{sat}} = \frac{75(v_{sat} dt) G q v_{sat} \frac{k}{d}}{k q v_{sat}} \propto \frac{G}{d} dt$$

**!!!**

➔ **Go thin!!**



(Real life is a bit more complicated, but the conclusions are the same)

Full simulation

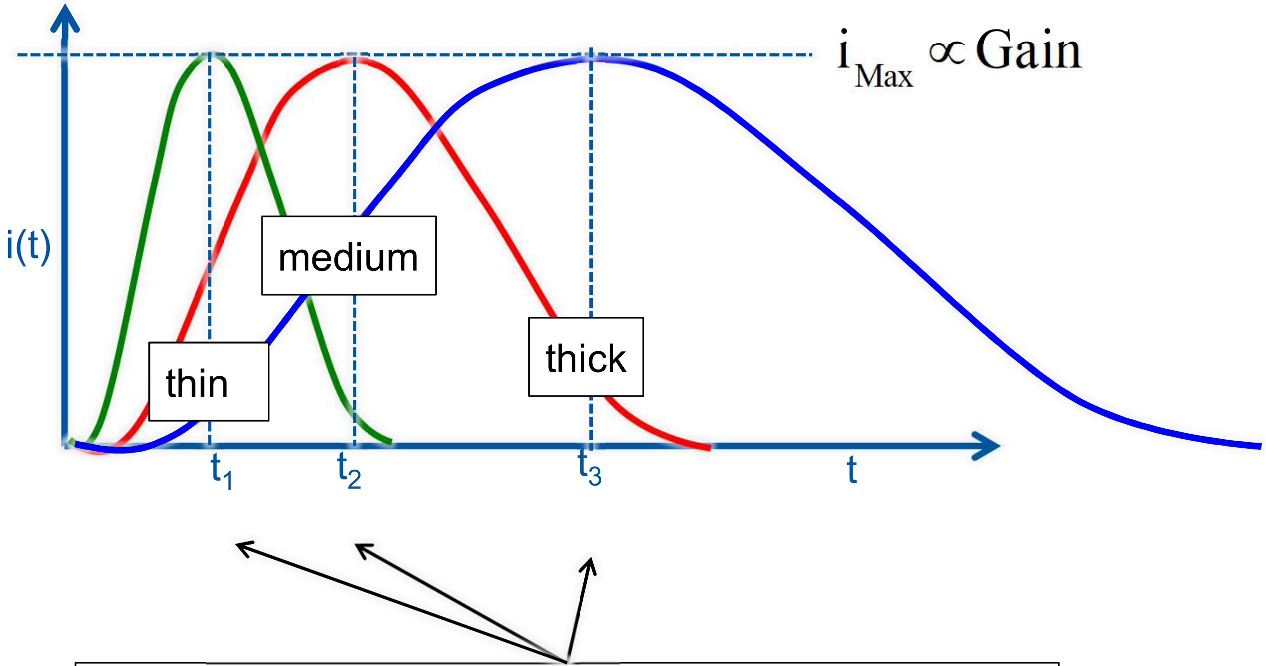
(assuming 2 pF detector capacitance)

**300 micron:**
~ 2-3 improvement with gain = 20

**Significant improvements in time resolution require thin detectors**

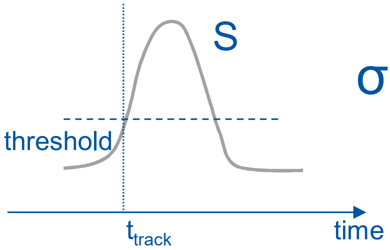
# Gain and Signal current

$$\frac{dV}{dt} \propto \frac{G}{d}$$



**The rise time depends only on the sensor thickness ~ 1/d**

# Time resolution

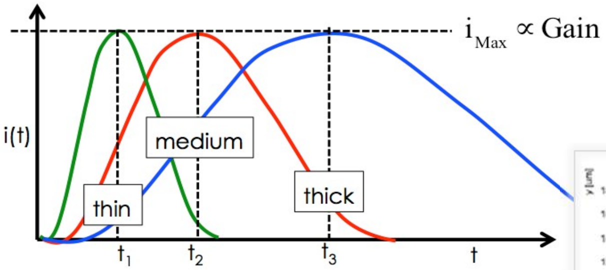


$$\sigma^2_t = \sigma^2_{Jitter} + \cancel{\sigma^2_{Time\ Walk}} + \sigma^2_{Landau\ Noise} + \sigma^2_{Distortion} + \cancel{\sigma^2_{TDC}}$$

Negligible
Optimize FE electronics

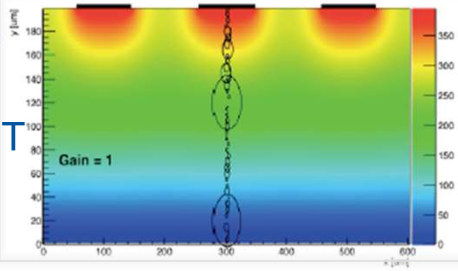
Negligible
Optimize RO electronics

$\sigma_{Jitter} \approx N/(dV/dt) \approx t_{rise}/(S/N)$
➔needs **Gain** to increase S/N
➔needs **thin detector** to decrease $t_{rise}$



NB: signal amplitude DOES NOT depend on detector thickness

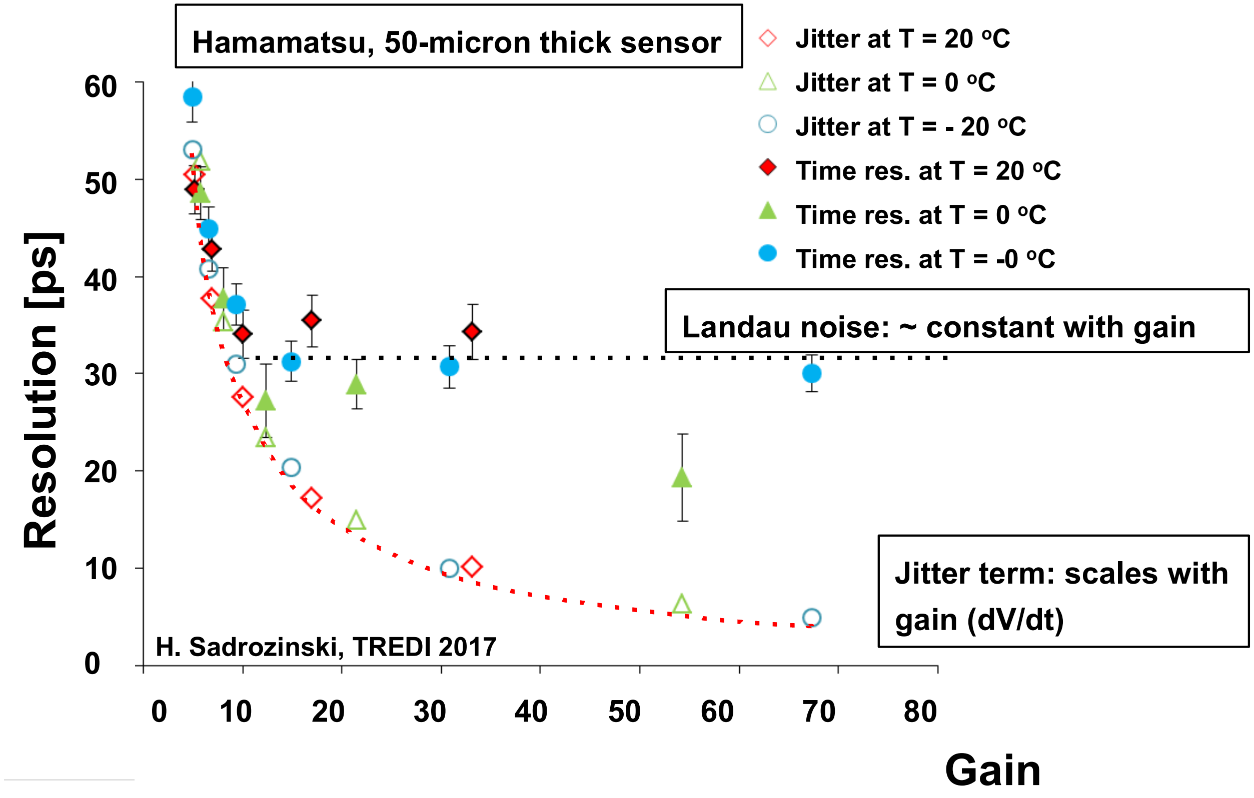
$I_{Ramo} \approx q\ v_{drift}\ E_w$
Requires **uniform $v_{drift}$ and $E_w$**
↓
parallel plate geometry
strip implant ~ pitch



Decreases with detector thickness
Intrinsic Limit $\sigma_{Landau\ Noise} \approx 25ps$

# UFSD  time resolution

**UFSD from Hamamatsu: 30 ps time resolution,**



Hamamatsu, 50-micron thick sensor

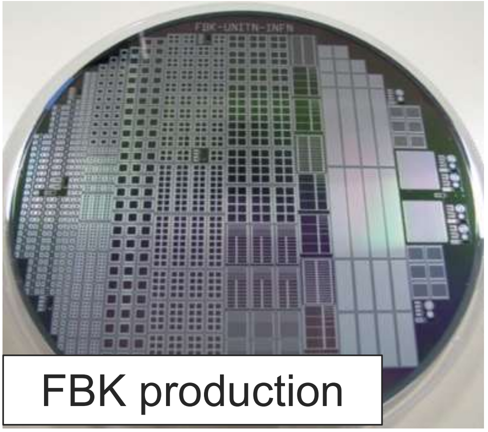
Landau noise: ~ constant with gain

Jitter term: scales with gain (dV/dt)

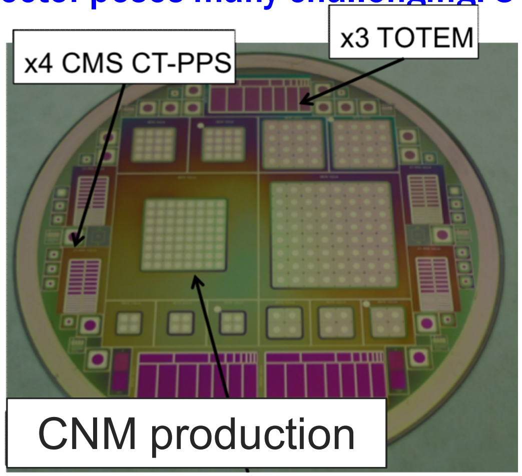
H. Sadrozinski, TREDI 2017

# Foundries Producing LGADs for the MTD

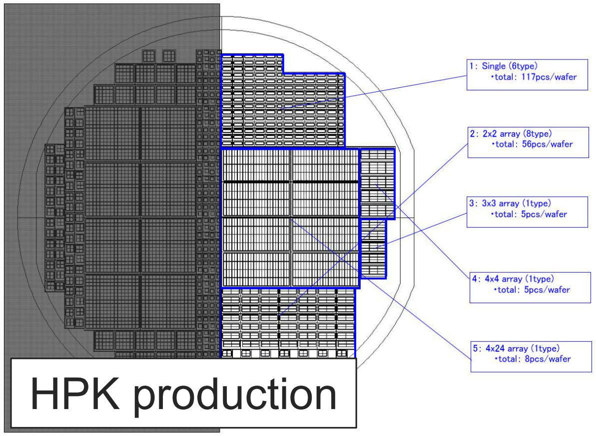
**Using LGADs for a “CMS size” detector poses many challenging: 3 sensor producers considered**



FBK production



CNM production



HPK production

Producers have different approaches for radiation damage mitigation, but all vendors can fulfil the CMS requirements, **including a factor of 2 safety margin**

**CMS1 delivered in Q3 2018**

**Next production: Q4 2019/Q1 2020**

**CMS1 production is due to arrive in Q4 2019 /Q1 2020**

**Next production: Q4 2019/Q1 2020**

- **Q3 2021: Sensor vendor qualification and final geometry selection**
- **Q3 2022: Sensor vendor selection and pre-production start**

**ON SCHEDULE**

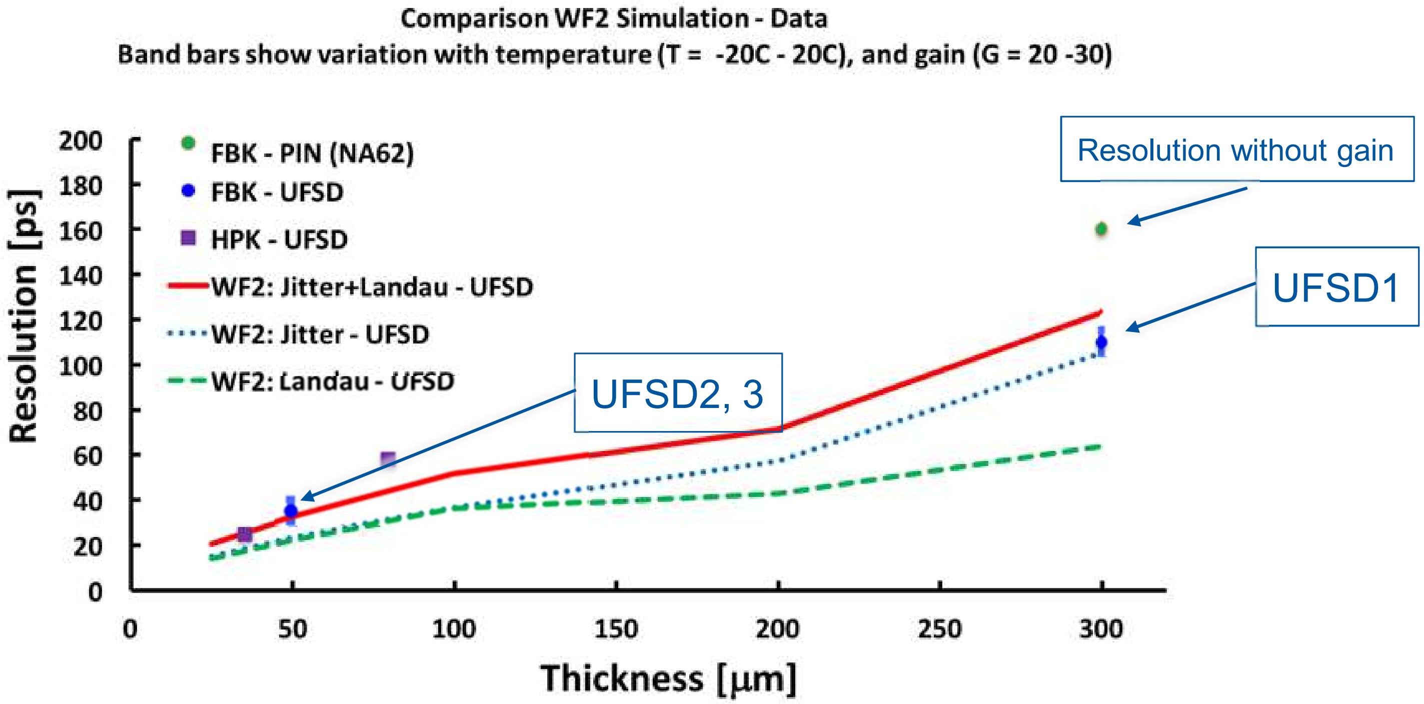
# UFSD time resolution summary

The UFSD advances via a series of productions.

For each thickness, the goal is to obtain the intrinsic time resolution

**Achieved:**

- **20 ps for 35 micron**
- **30 ps for 50 micron**



**Comparison WF2 Simulation - Data**

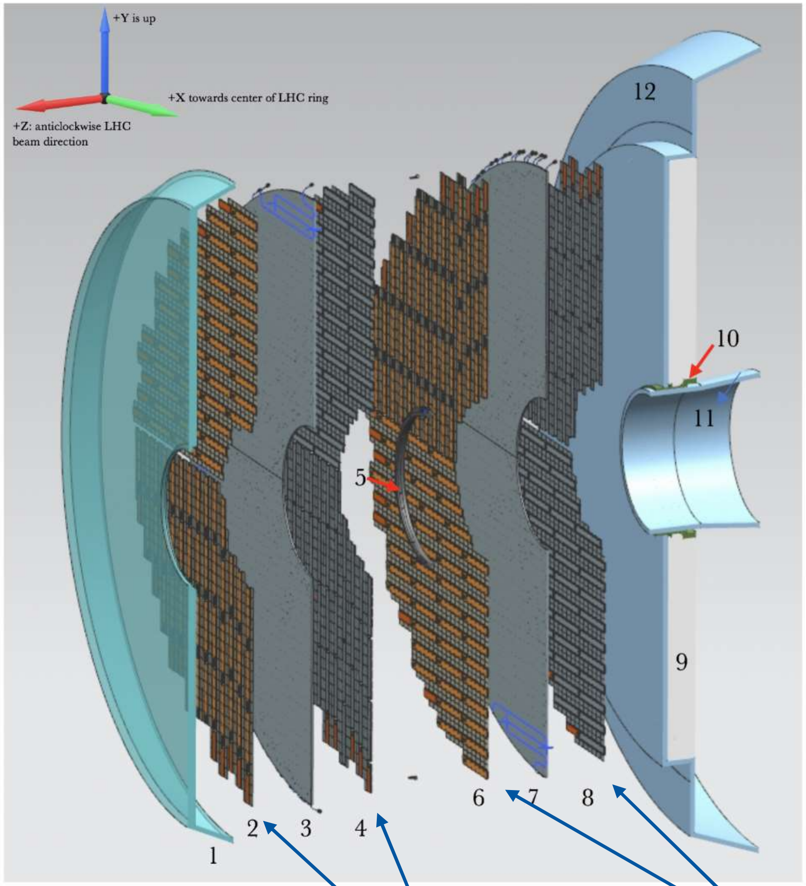
**Band bars show variation with temperature (T = -20C - 20C), and gain (G = 20 -30)**

Resolution without gain

UFSD1

UFSD2, 3

# ETL Structure



Disk 1: 2 faces

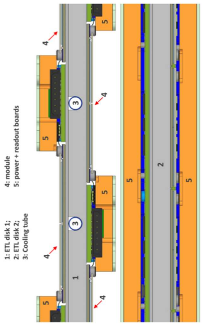
Disk 2: 2 faces

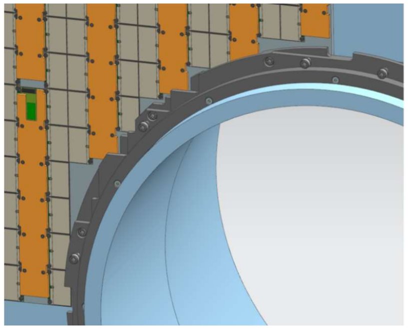
Two disks of UFSDs (per side) $1.6 < |\eta| < 2.9$ :

Average 1.8 hits per track

Designed for σ < 50 ps per hit

1: ETL Thermal Screen
2: Disk 1, Face 1
3: Disk 1 Support Plate
4: Disk 1, Face 2
5: ETL Mounting Bracket
6: Disk 2, Face 1
7: Disk 2 Support Plate
8: Disk 2, Face 2
9: HGCal Neutron Moderator
10: ETL Support Cone
11: Support cone insulation
12: HGCal Thermal Screen





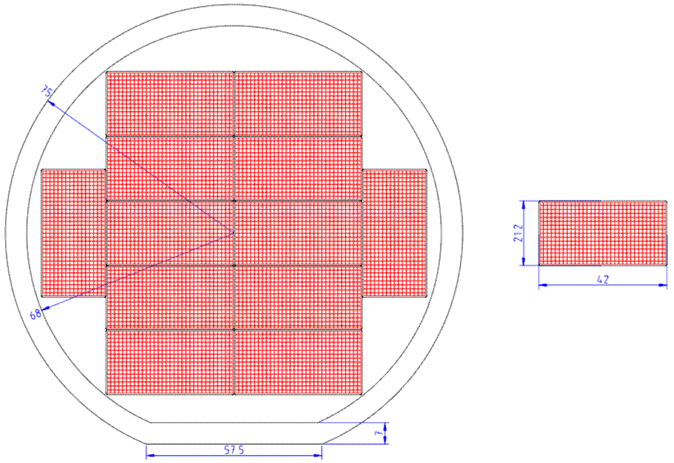
Sensors are mounted in rows on each face of Aluminum cooling disks, staggered wrt opposite face to host readout boards without loosing coverage

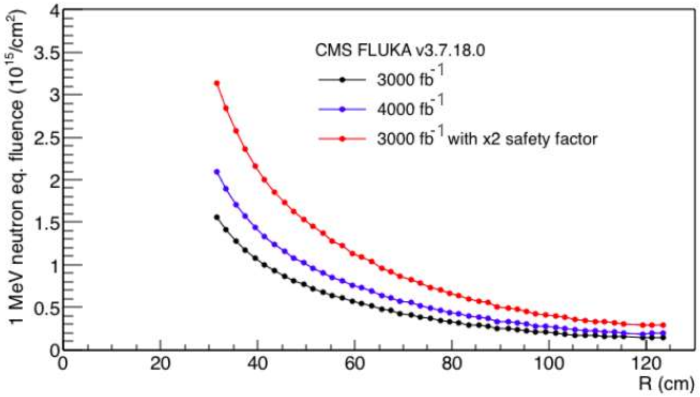
# UFSDs for the ETL

## Using UFSDs for a “CMS size” detector poses many challenging

Sensor specifications:

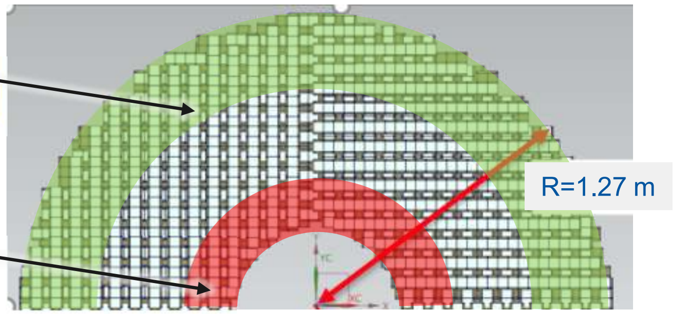
- Intrinsic Gain: 10-20
- Pad size: 1.3 x 1.3 mm$^2$
- High fill factor (>85% per layer)
- 2-disk x-y layout
- Number of sensors: ~18000 (~ 16 m$^2$, ~2k 6-inch wafers)
- Sensors of 2x4 cm$^2$
- Radiation hardness





Less than 4x10$^{14}$ n$_{eq}$/cm$^2$ for 50% of sensors

Up to 2x10$^{15}$ n$_{eq}$/cm$^2$ for 15% of sensors

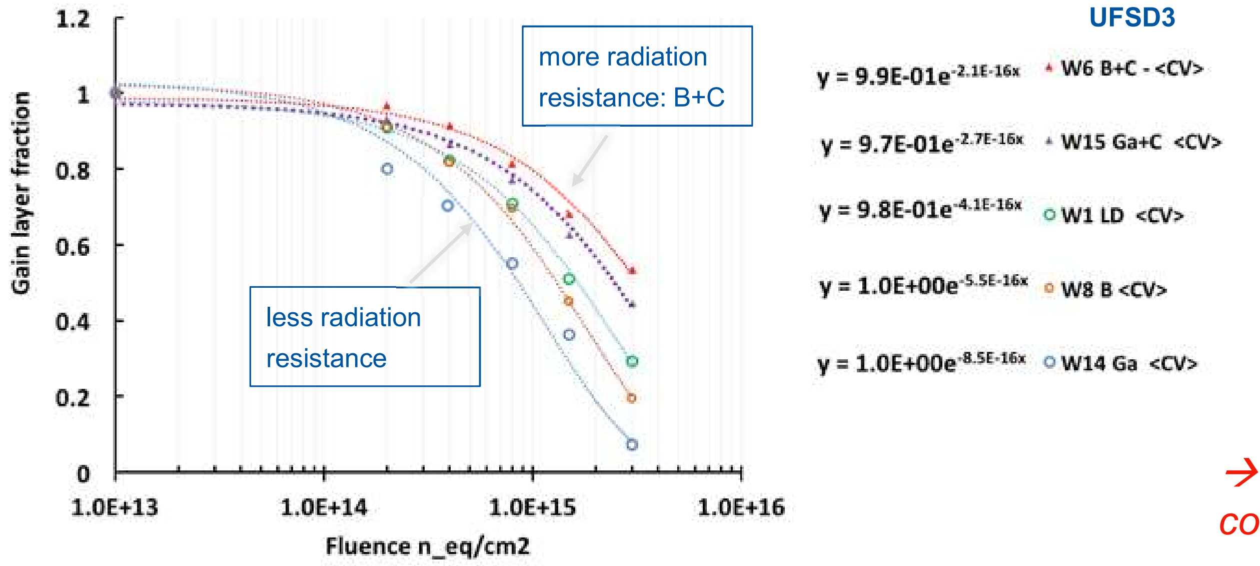


# Irradiation effects

**Irradiation causes 3 main effects:**

- Decrease of charge collection efficiency due to trapping
- **Doping creation/removal (the Gain fades)**
- Increased leakage current, shot noise

But…



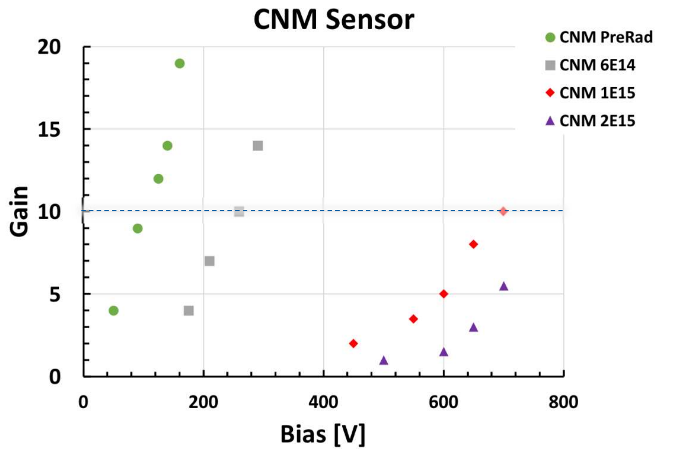
more radiation resistance: B+C

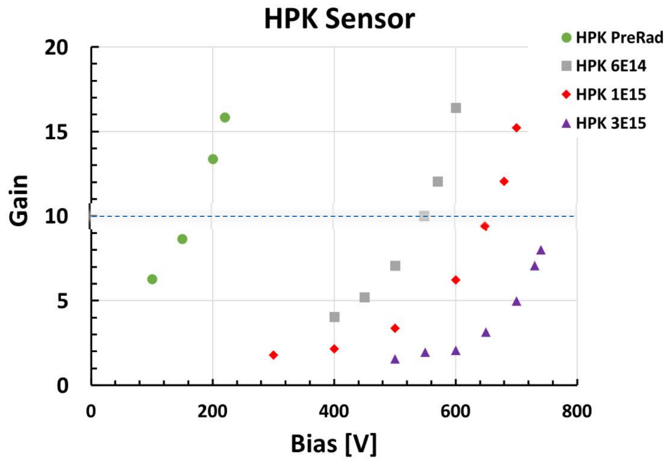
less radiation resistance

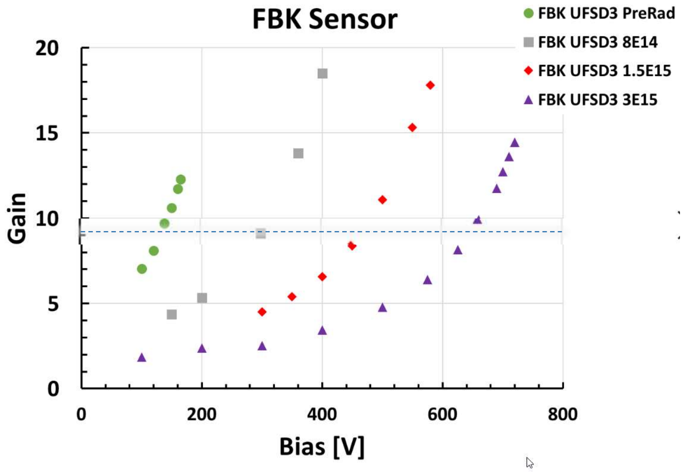
**Carbon addition works really well, increasing by a factor of 2-3 the radiation hardness**

*→ more details in Marco Ferrero contribution in poster session*

# Vendors performances…so far


CNM Sensor

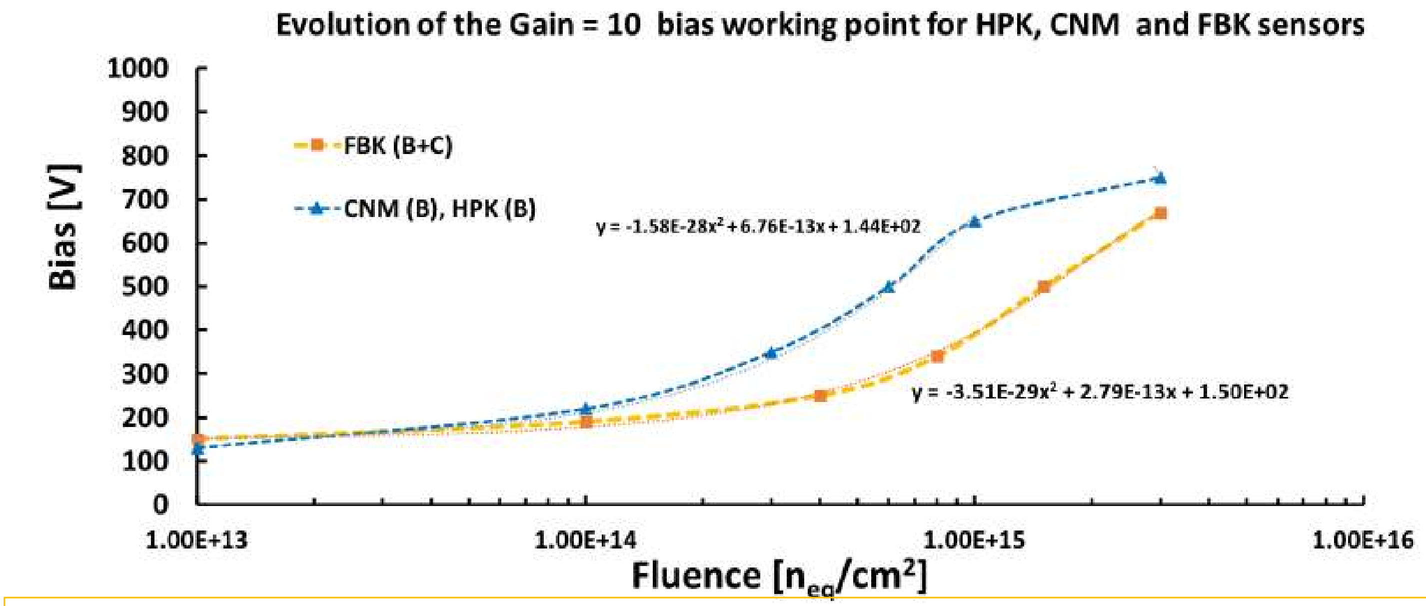

HPK Sensor


FBK Sensor

- **All vendors successful in delivering G = 10 till the end of HL-LHC**
- CNM HPK similar behavior, while
- FBK, can reach G = 10 at lower Bias

Refs:
https://arxiv.org/abs/1804.05449v2,
https://arxiv.org/abs/1707.04961,
https://doi.org/10.1016/j.nima.2018.08.040

# On the detector sensor biasing scheme

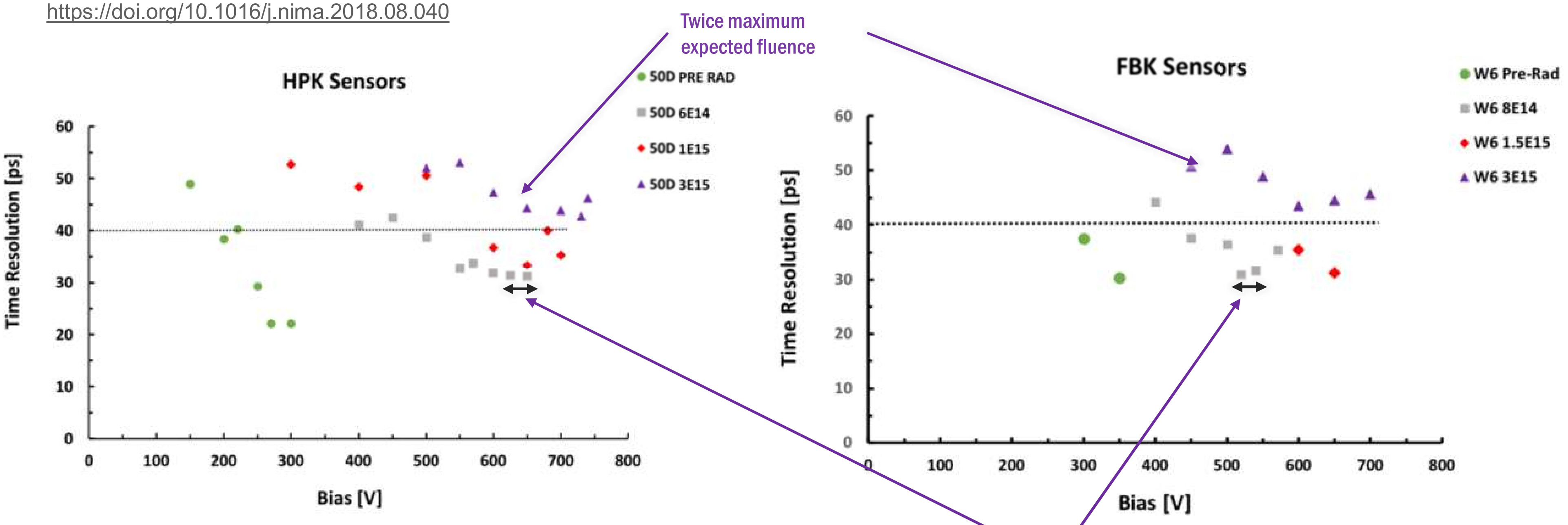


- Strong Bias increase needed to maintain G = 10 as a function of the irradiation level (FBK lower Bias than CNM,HPK)
- Detectors at different rapidity (radius) work at different Bias

# Vendors performance … so far

Refs:
https://arxiv.org/abs/1804.05449v2,
https://arxiv.org/abs/1707.04961,
https://doi.org/10.1016/j.nima.2018.08.040

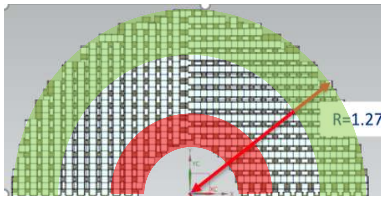
## Time resolution



Twice maximum expected fluence

Both HPK and FBK sensors achieve 30-35 ps up to $1.5\times10^{15}\ n_{eq}/cm^2$

and 40-45 ps for 2x max fluence



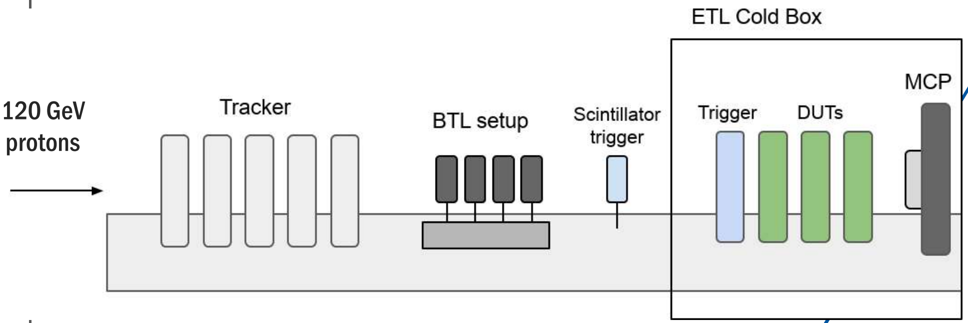
Non uniform irradiation problem mitigated:

50V “undervolt” (we expect <30V) is not

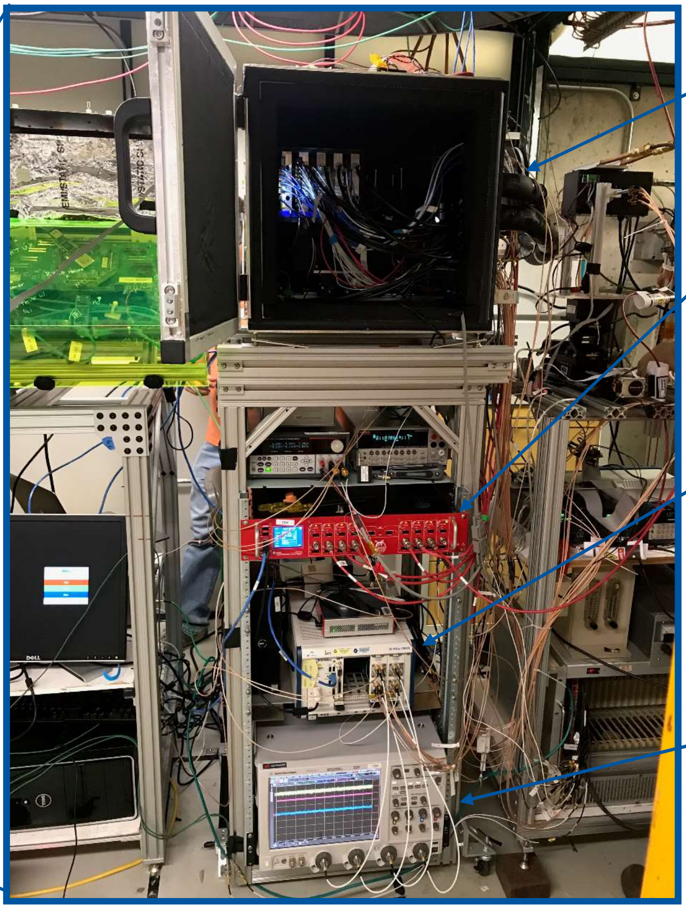
significantly affecting timing performance

# FNAL Test Beam

**LGADs were tested at FNAL using an MCP-PMT as time reference and a silicon tracker to measure efficiency and uniformity**



Permanent mechanical structure: ETL cold box can slide in and out of beamline as needed



Cold box (5 boards)

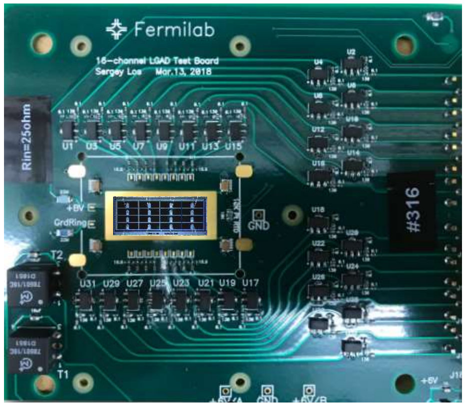
High Voltage

High BW multiplexer

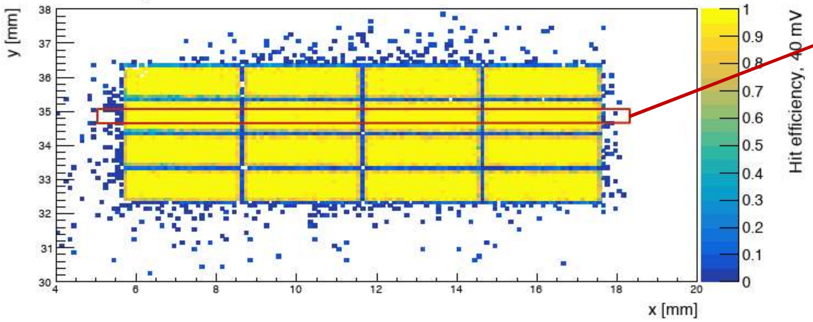
40 Gsa/s
100k events per spill
(possibility of using Sampic with 32/64 ch)

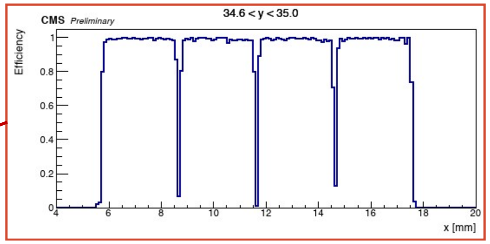
# FNAL Test Beam: from single pad to arrays

## Uniformity has been studied on 16 pads arrays using a 16ch readout board



### Hit Efficiency



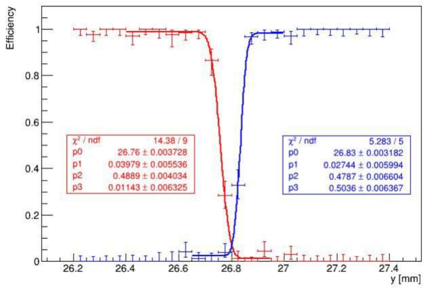


Efficiency >99% (except gaps)

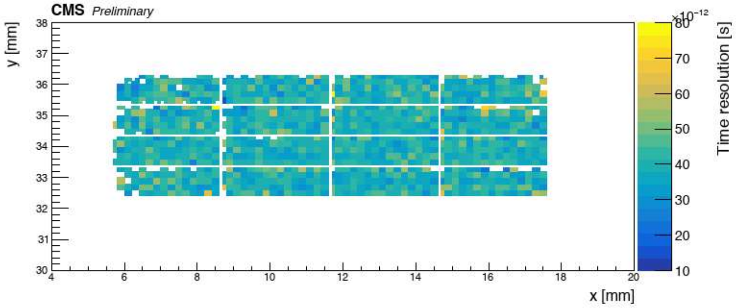
Interpad distance investigated:

Fill Factor >85% per layer

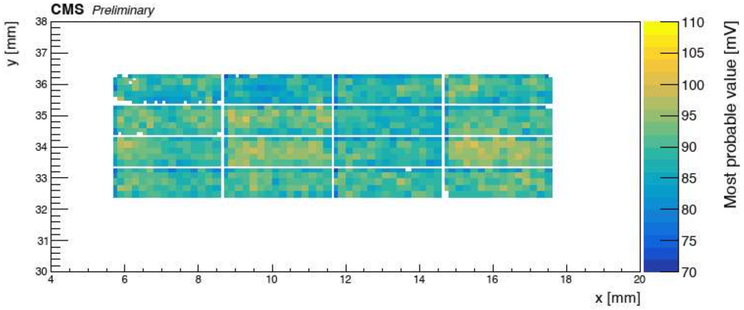
Interpad HPK 2X2 IP3 185V - 76 ± 5 µm



### Time Resolution



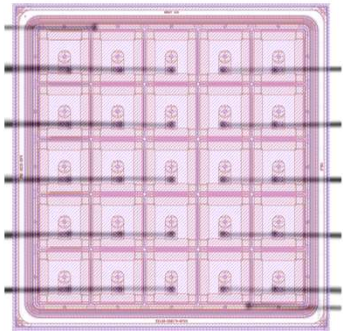
### Most Probable Amplitude



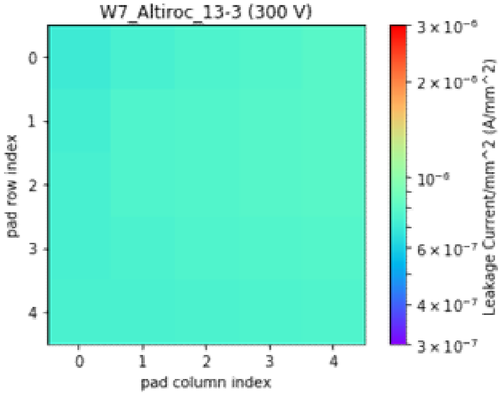
# IV sensor characterization

## It is impossible to test several m$^2$ of sensors using a particle beam: uniformity checks using automated systems

Using a probe card it is possible to measure automatically 25 pads



All pads have a similar current @300V



Very few channels have a leakage current away from the mode:

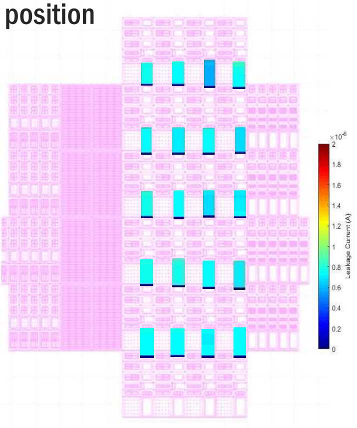
Table 3.4: Summary of the uniformity studies on the latest sensor productions.

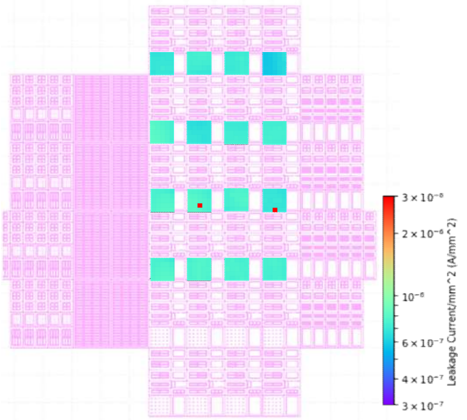
| Foundries | Sensor type | # Sensors tested | # Warm pads | # Bad pads | Comments |
|---|---|---|---|---|---|
| FBK | 4 × 24 pads | 152 | 14 (0.1%) | 0 | bias = 100 V |
| FBK | 5x5 pads | 23 | 4 (0.7%) | 0 | bias = 300 V |
| HPK | 4 × 24 pads | 15 | 20 (1.3%) | 0 | bias = 250 V |

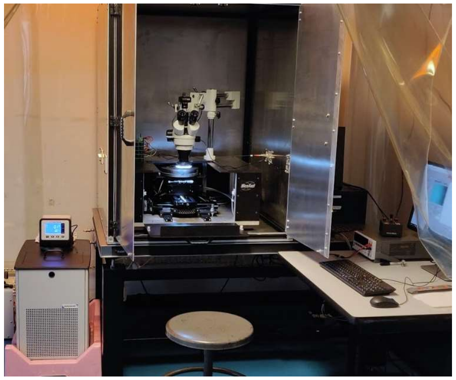
Leakage current > 10x the mode

Leakage current too high: sensor failure

Same test performed on sensors in different position on the wafer



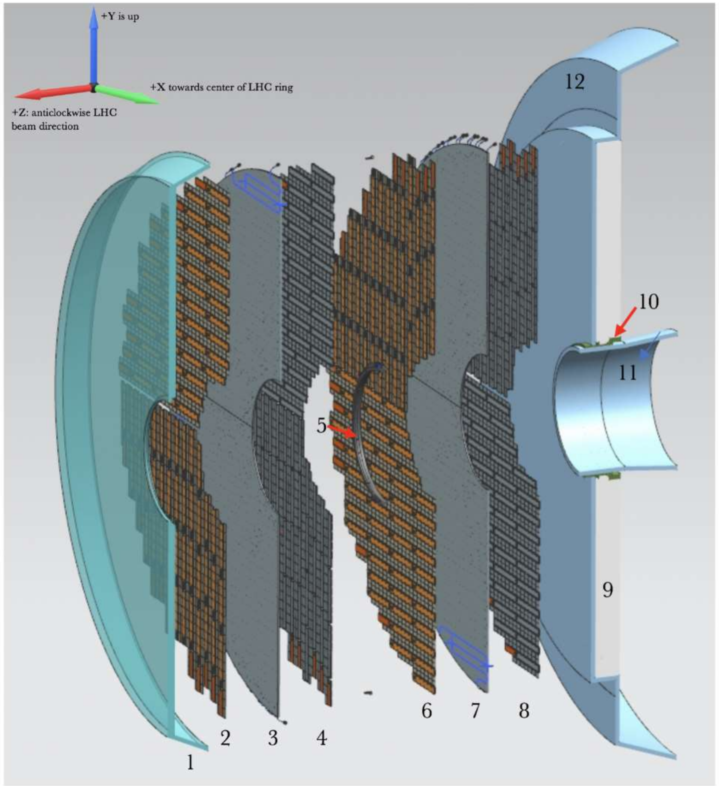




Fully automated **visual checks** and **IV characterization** of the 5-10% wafer under development

# ETROC: read-out ASIC for ETL

ETROC, currently under design at FNAL, will be able to read out 16 m$^2$ of UFSDs, measuring the time of arrival with a precision better than 50 ps per hit (<30 ps per track)

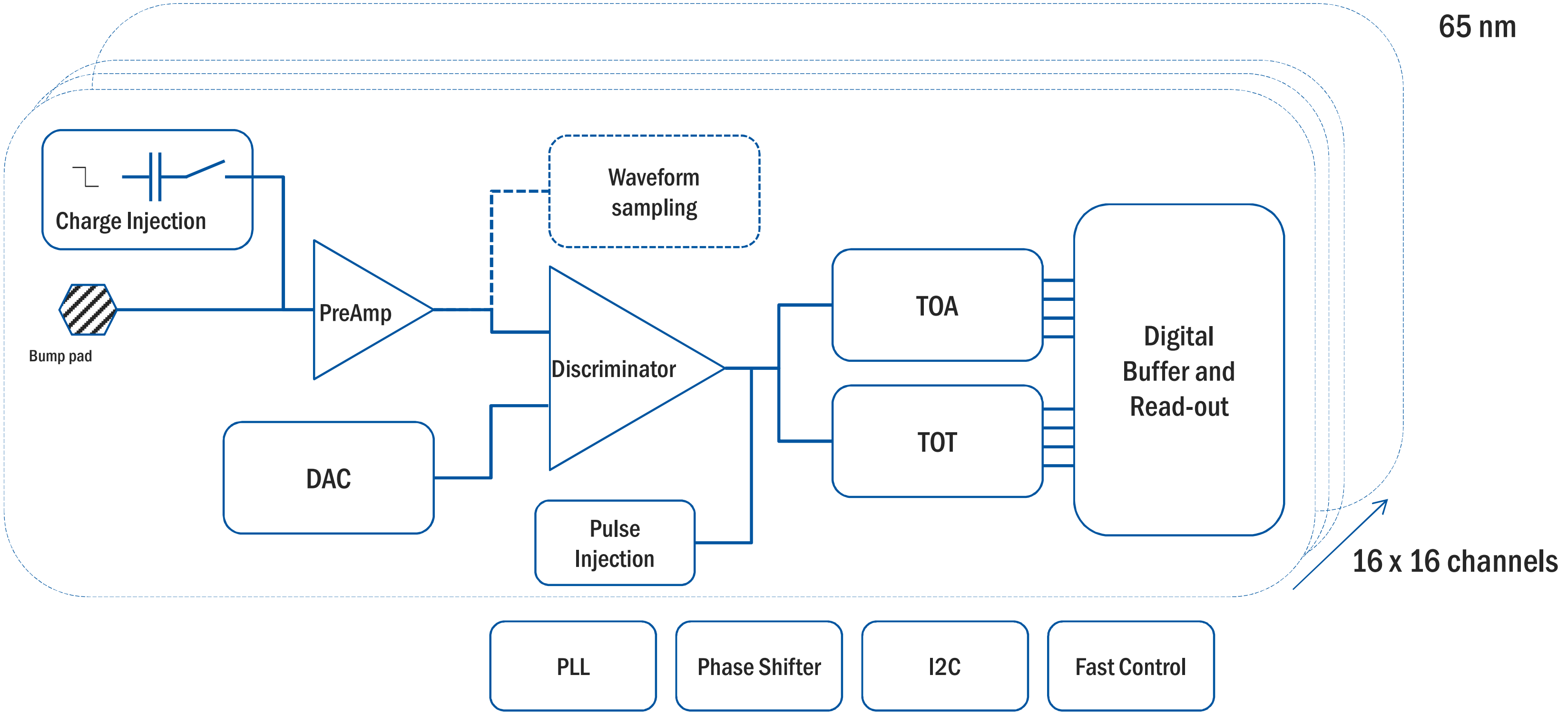


Requirements:

- < 50 ps per hit: ASIC contribution <40 ps
- Pad Size: 1.3x1.3 mm$^2$
- Input capacitance: 3.4 pF
- MPV for MIP: ~6 fC for UFSD @ $10^{15}$ neq/cm$^2$
- Buffer latency :12.5 μs
- Trigger rate: Up to 1 MHz
- Time Of Arrival: ~ 5 ns windows
- Time Over Threshold: ~ 10 ns windows
- Power consumption: <4 mW/ch (80 kW total)

# ETROC0 Design

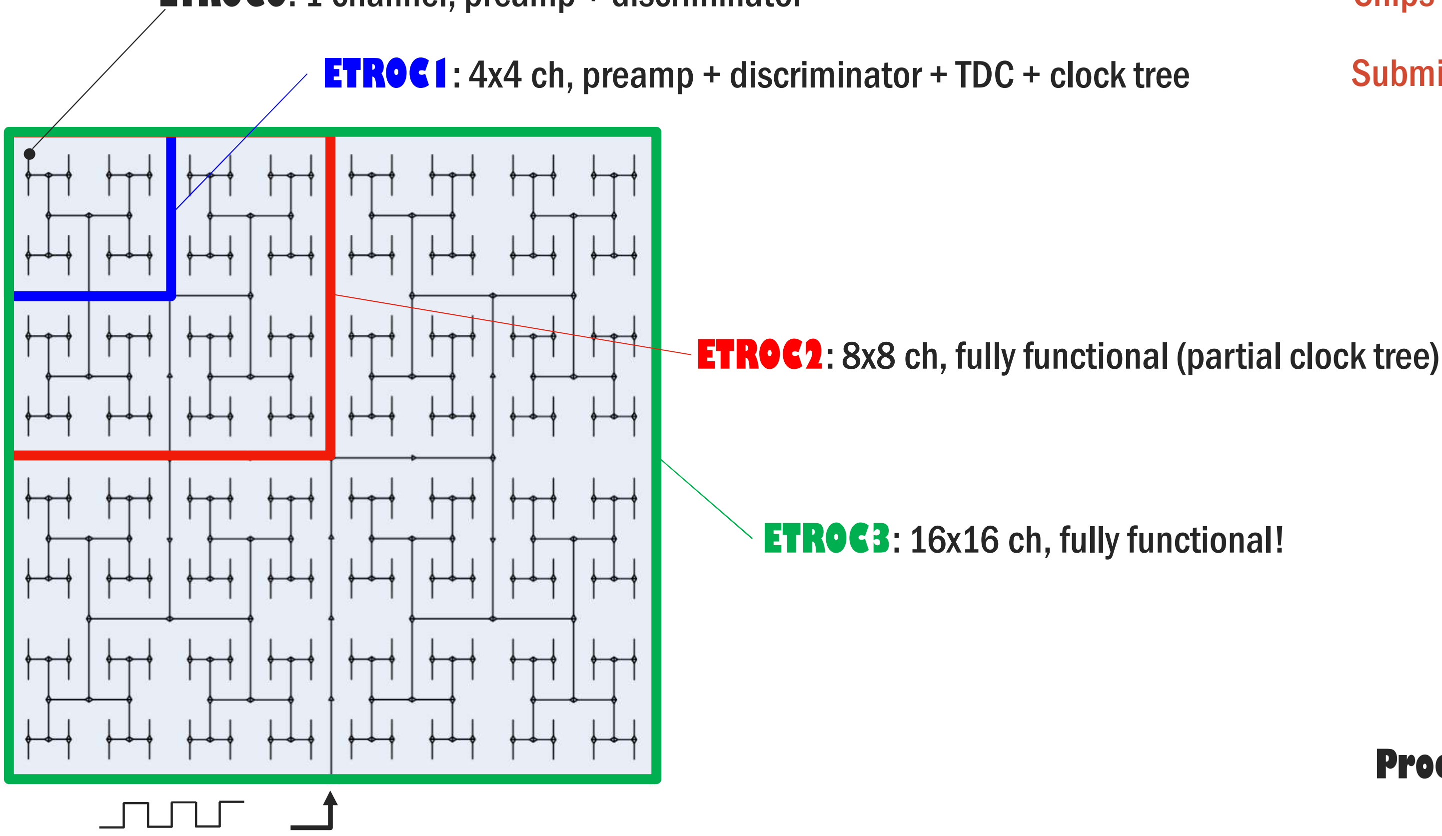
**The front-end has an analog part optimized for UFSDs; 2 time to digital converters per channel; digital buffers and I&O**



.... <4 mW/ch

# ETROC Schedule

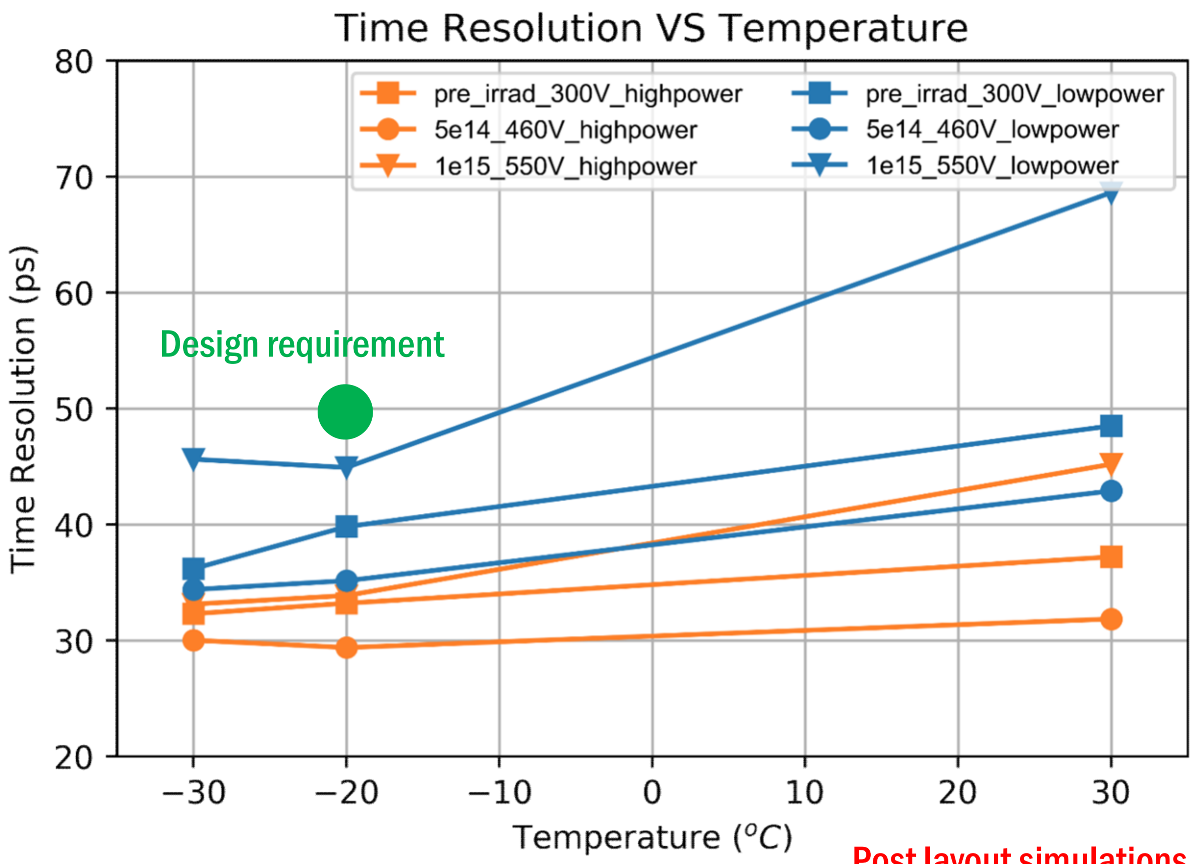
The first test is to test the analog part; to then add the TDC and finally increase the number of channels.



| | |
|---|---|
| **ETROC0**: 1 channel, preamp + discriminator | Chips received and being tested |
| **ETROC1**: 4x4 ch, preamp + discriminator + TDC + clock tree | Submitted august 2019 |
| **ETROC2**: 8x8 ch, fully functional (partial clock tree) | Q4 2020 |
| **ETROC3**: 16x16 ch, fully functional! | Q1 2022 |
| **Production** | Q4 2022 |

# ETROC Preamplifier + Discriminator

**The analog part of the front-end is capable of performing according to the design requirements**



**preamp @ low power:**

~ 35 ps @5e14

**preamp @ high power:**

~ 35ps @1e15

**Post layout simulations: being validated with lab tests of ETROC0**

# ETL expected performance

The expected time resolution per track (2 hits) is expected to be better than 30 ps

$$\sigma_t^2 = \underbrace{\sigma_{sensor}^2 + \sigma_{jitter}^2 + \sigma_{digit}^2} + \sigma_{clock}^2 + \sigma_{walk}^2 \qquad \approx 41\ \text{ps}$$

Sensor + preamplifier + discriminator + TDC:< 35 ps

Time walk correction residual:< 10 ps

Internal + system clock distributions:< 18 ps

Expected time resolution per track (2 hits): $\frac{41\ \text{ps}}{\sqrt{2}} \approx 29\ \text{ps}$

# Conclusions

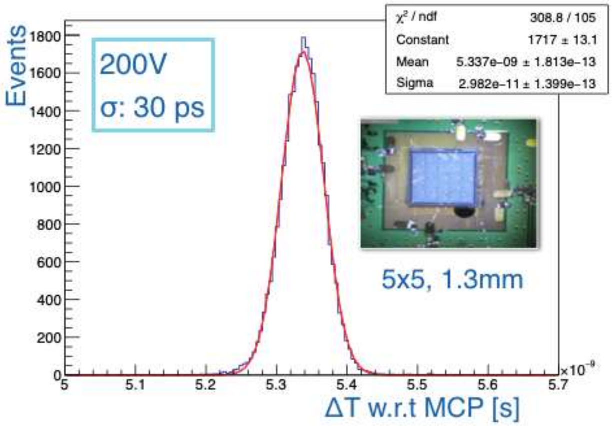
- **Sensor on schedule**

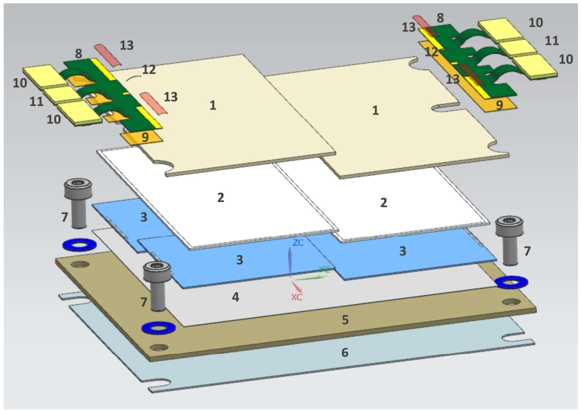
- LGAD is a mature technology
- Ultra fast silicon detector design choices nearing completion
- Received good sensors capable of satisfying  ETL requirements
- <40 ps time resolution at the end of life is achievable
- Test of large arrays proved
- Test of “very large” number of sensors under development

- **ASIC on schedule**

- ETROC0 with analog part produced and test on going
- Good agreement with simulations
- ETROC1 submitted this summer

- Test with sensors (on bench and with beam) planned in Q1 2020 .......... STAY TUNED





1: AlN module cover
2: LGAD sensor
3: ETL ASIC
4: Mounting film
5: AlN carrier
6: Mounting film
7: Mounting screw
8: Front-end hybrid
9: Adhesive film
10: Readout connector
11: High voltage connector
12: LGAD bias voltage wirebond
13: ETROC wirebonds

**M.Costa** – 15th Topical Seminar on Innovative Particle and Radiation Detectors


THANK YOU !

# Backup

# ETROC details

## Summary

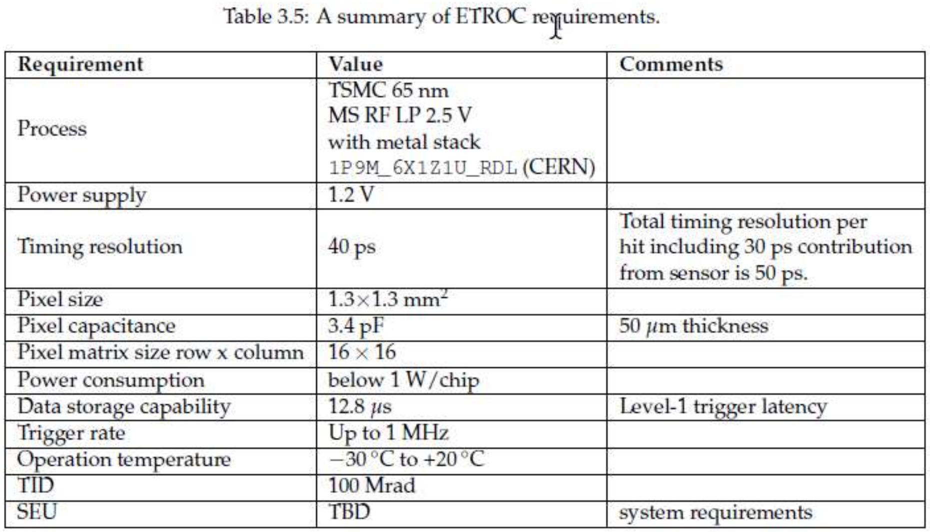


Table 3.5: A summary of ETROC requirements.

| Requirement | Value | Comments |
|---|---|---|
| Process | TSMC 65 nm<br>MS RF LP 2.5 V<br>with metal stack<br>`1P9M_6X1Z1U_RDL` (CERN) | |
| Power supply | 1.2 V | |
| Timing resolution | 40 ps | Total timing resolution per hit including 30 ps contribution from sensor is 50 ps. |
| Pixel size | 1.3×1.3 mm$^2$ | |
| Pixel capacitance | 3.4 pF | 50 $\mu$m thickness |
| Pixel matrix size row x column | $16 \times 16$ | |
| Power consumption | below 1 W/chip | |
| Data storage capability | 12.8 $\mu$s | Level-1 trigger latency |
| Trigger rate | Up to 1 MHz | |
| Operation temperature | $-30$ °C to +20 °C | |
| TID | 100 Mrad | |
| SEU | TBD | system requirements |

## Power consumption

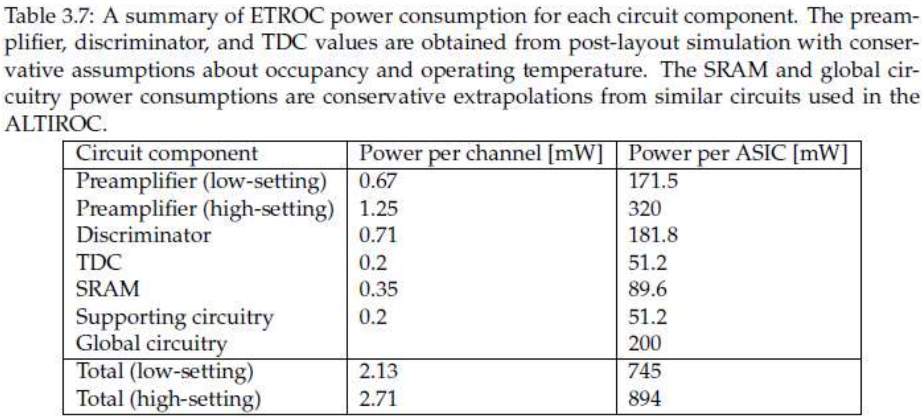


Table 3.7: A summary of ETROC power consumption for each circuit component. The preamplifier, discriminator, and TDC values are obtained from post-layout simulation with conservative assumptions about occupancy and operating temperature. The SRAM and global circuitry power consumptions are conservative extrapolations from similar circuits used in the ALTIROC.

| Circuit component | Power per channel [mW] | Power per ASIC [mW] |
|---|---|---|
| Preamplifier (low-setting) | 0.67 | 171.5 |
| Preamplifier (high-setting) | 1.25 | 320 |
| Discriminator | 0.71 | 181.8 |
| TDC | 0.2 | 51.2 |
| SRAM | 0.35 | 89.6 |
| Supporting circuitry | 0.2 | 51.2 |
| Global circuitry | | 200 |
| Total (low-setting) | 2.13 | 745 |
| Total (high-setting) | 2.71 | 894 |