# Upgrade of the CMS electromagnetic calorimeter for precision timing and energy measurement at the High Luminosity phase of the LHC

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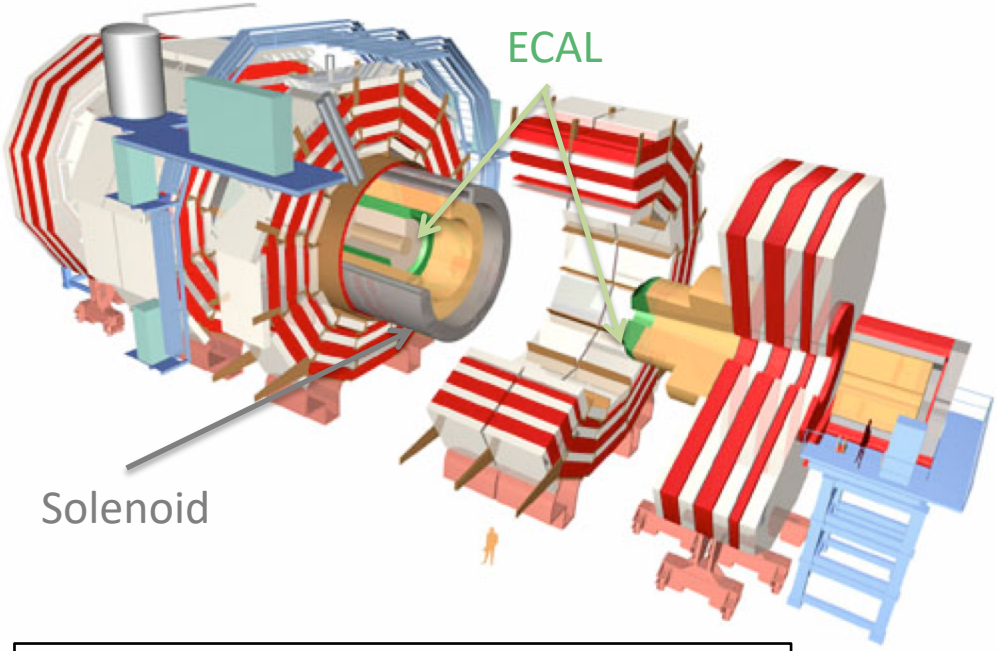
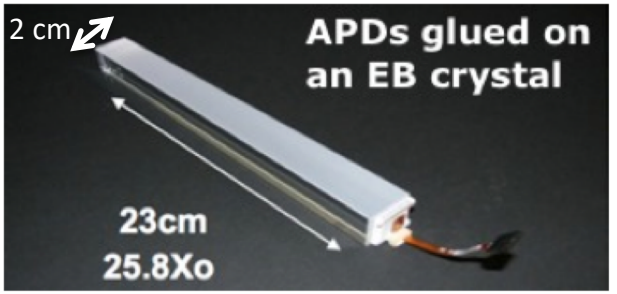
for the CMS Collaboration

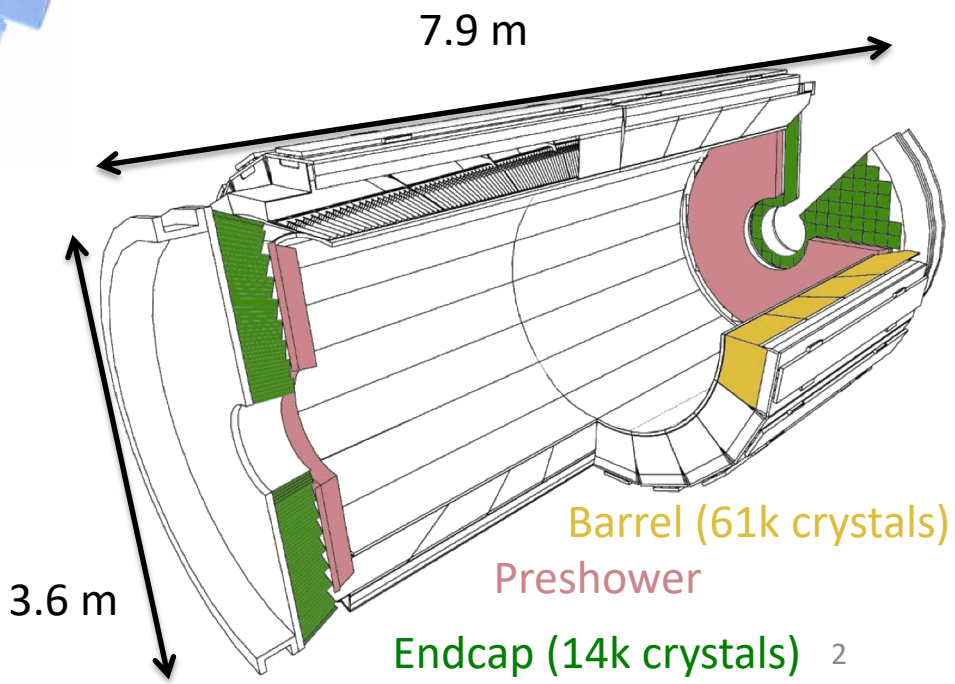


# The CMS EM Calorimeter




Lead tungstate crystals



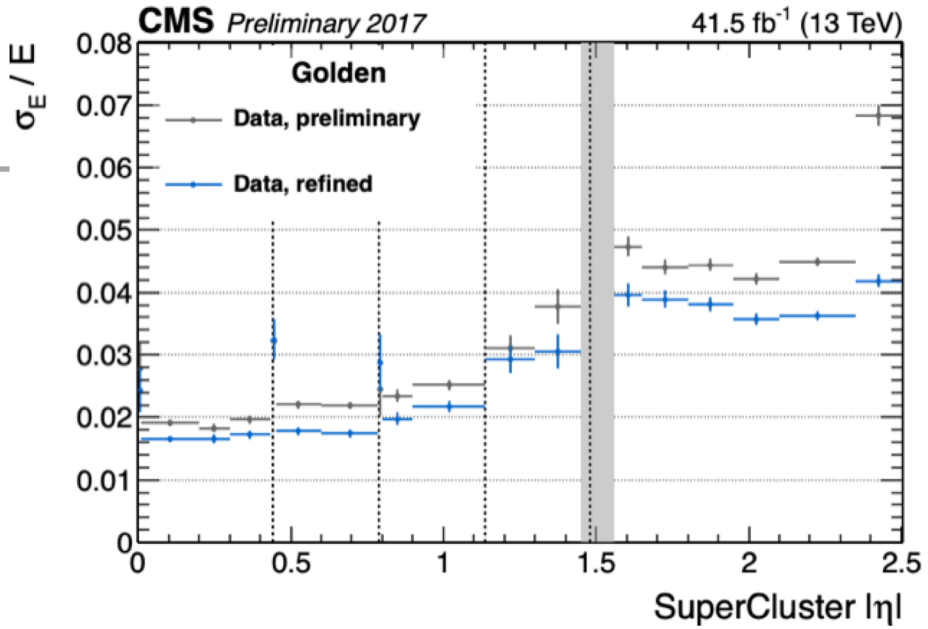

Ecal numbers

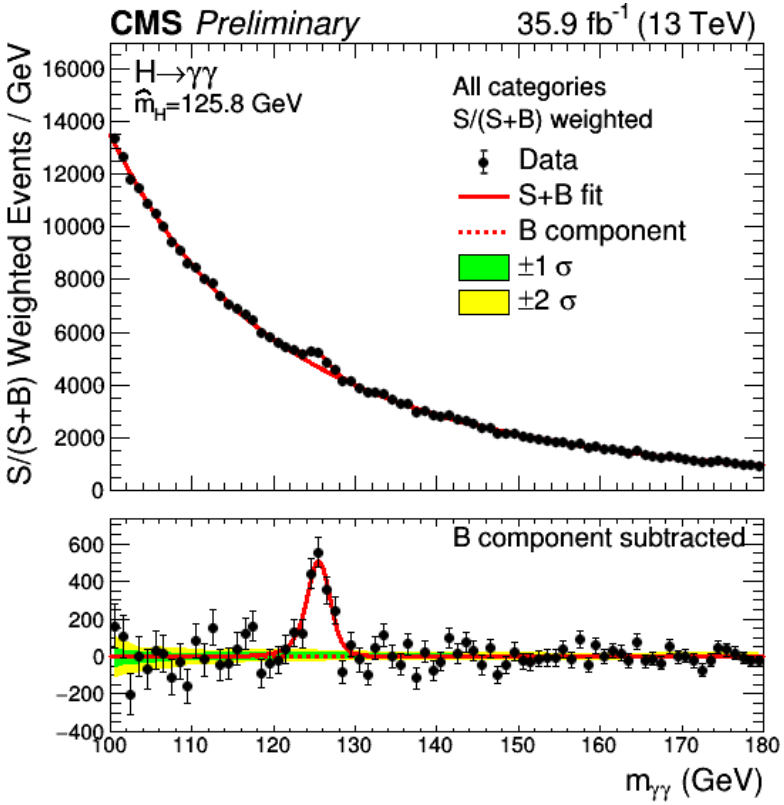
- 61200 + ~14k $PbWO_4$ crystals
- $r_M$= 2.19 cm
- $t_{75\%}$ = 25 ns
- ρ= 8.28 g/cm$^3$

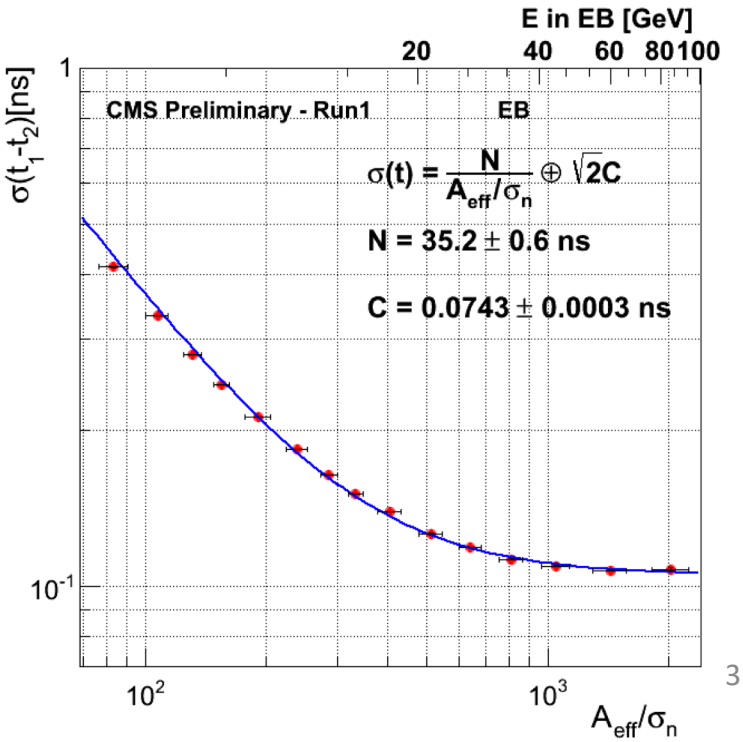
APD photosensors (Barrel)

# Performance

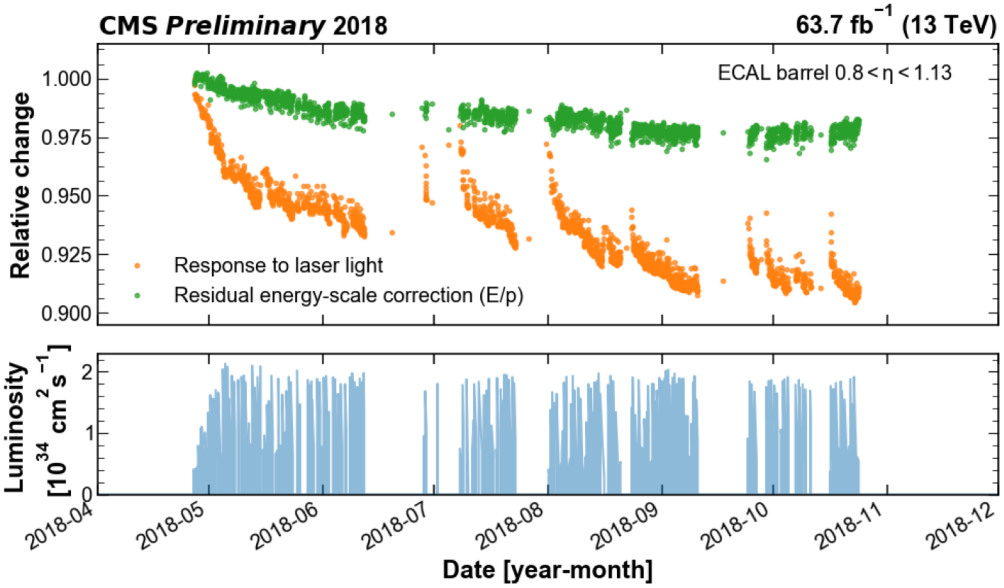
**Excellent Energy Resolution**
**Good Time Resolution**
**Good stability**
**Prominent Role in CMS physics program**

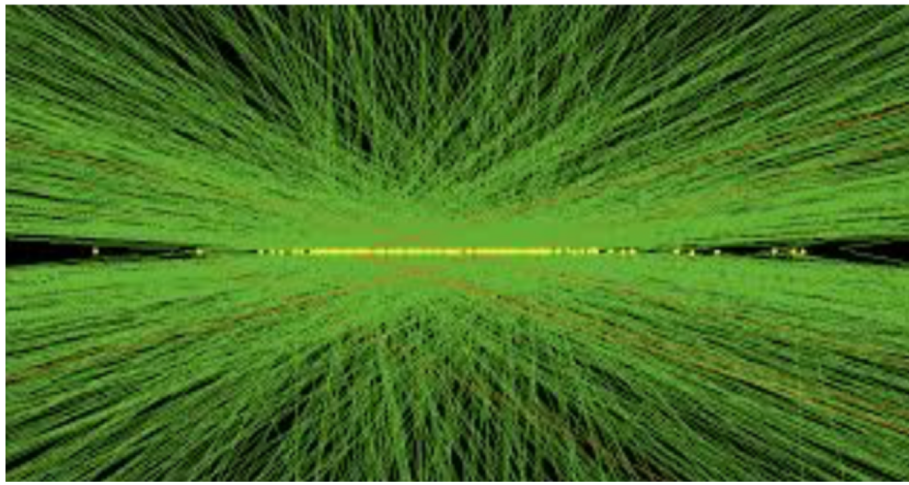


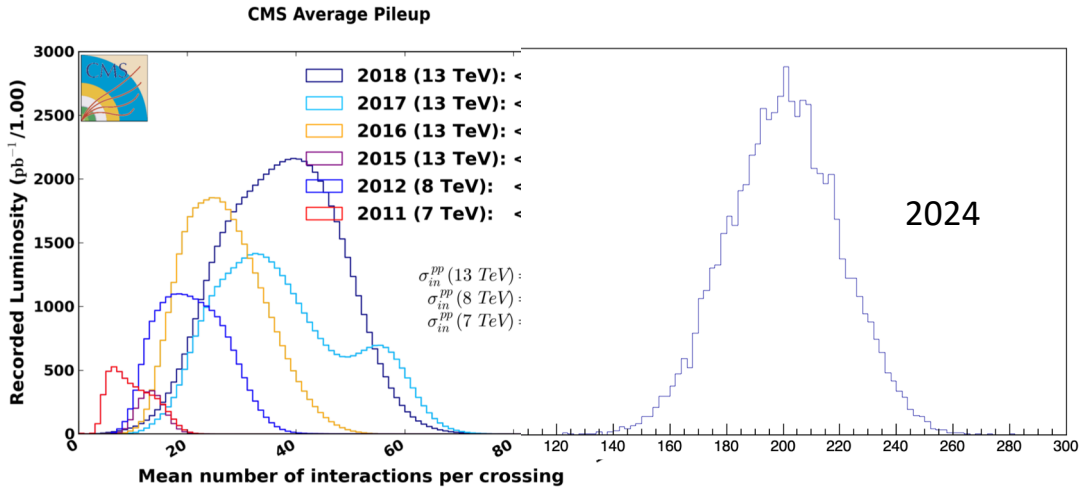
# HL-LHC Upgrade



Challenges:

- Detector ageing affects transparency and APD noise
- Harsher conditions : number of concurrent interactions per bunch crossing (pileup) increases 4-5-fold
- To obtain the same physics performance a detector upgrade is needed



# HL-LHC ECAL Upgrade Scope

The ECAL Endcaps will not be able to maintain adequate performance at HL-LHC and will be replaced by HGCal

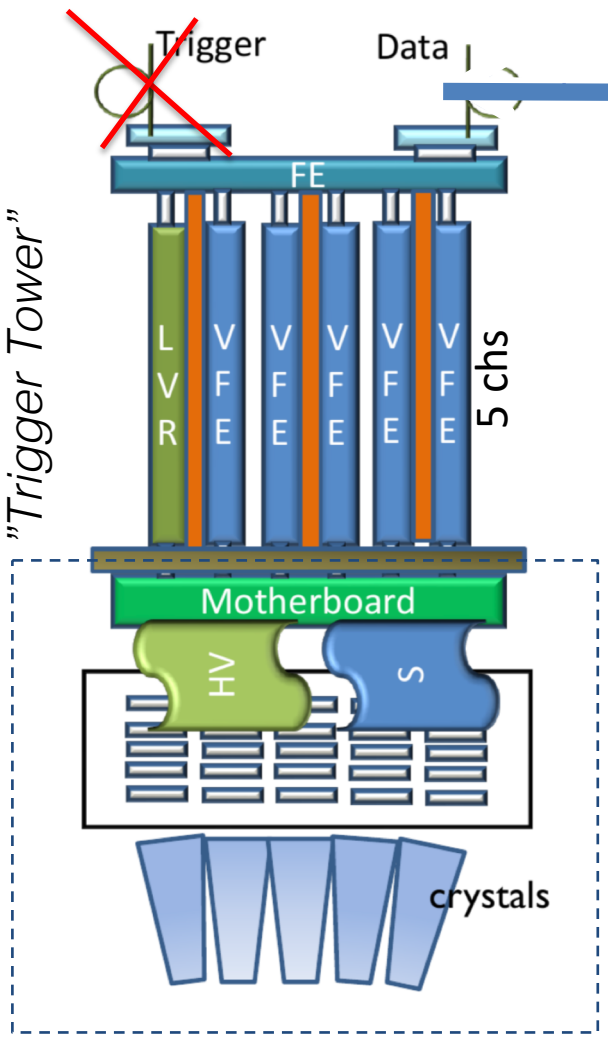
ECAL Barrel reloaded:

1 Reduction of operating temperature from 18 C to 9 C
- To mitigate APD leakage current and increase light yield

2 Faster front-end electronics
- To improve timing resolution and vertex identification
- Improve the discrimination between scintillation light from EM showers and direct hits in the APD (“spikes”)

3 New, off-detector L1 trigger and readout electronics
To improve trigger flexibility and cope with increased CMS-wide L1 trigger latency (from 3.5 us to 12.5 us) and rates (from 100 kHz to 750 kHz)

# Front-End Electronics



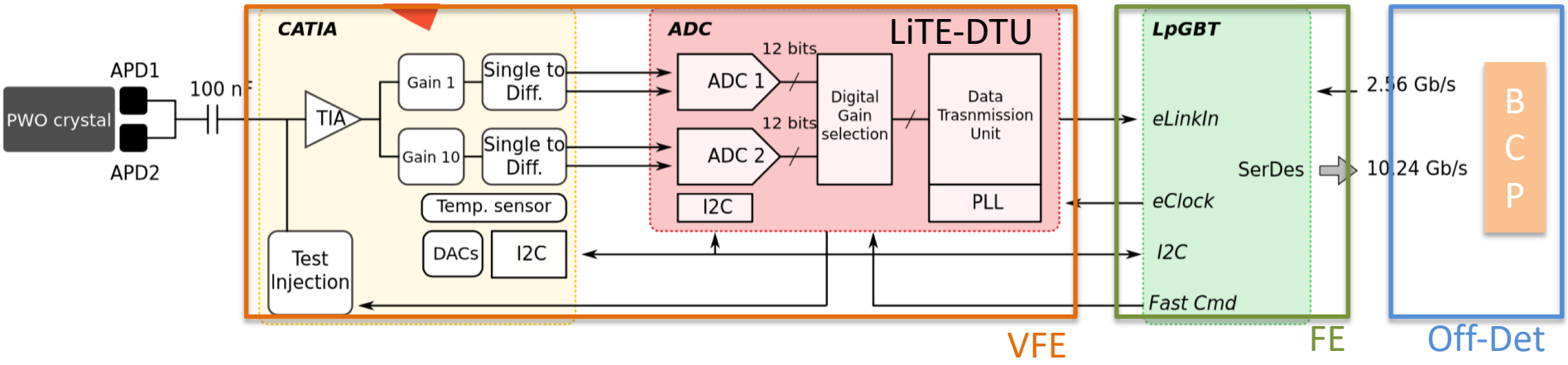

Same as current

Off-detector electronics:
L1 trigger primitive formation
Readout

In the upgraded scheme the APD output is sampled and every sample is shipped out to the off-detector electronics via high-speed optical links

- Faster analog electronics
- 12 bit, 160 MHz sampling
- Improves spike discrimination and time resolution at the cost of higher bandwidth occupation -> data compression

# Upgraded readout scheme




VFE

Reads out 5 APDs, at two pre-amp gains to match dynamic range

Analog ASIC : **CATIA**. A 35 MHz transimpedance amplifier

Digital ASIC: **LiTE-DTU**. 12-bit, 160 MHz ADC, Data Transmission Unit with gain selection and compression, PLL, in 65 nm.

FE

Optical transmission using lpGBT. Serves 5 VFEs. Clock distribution and control

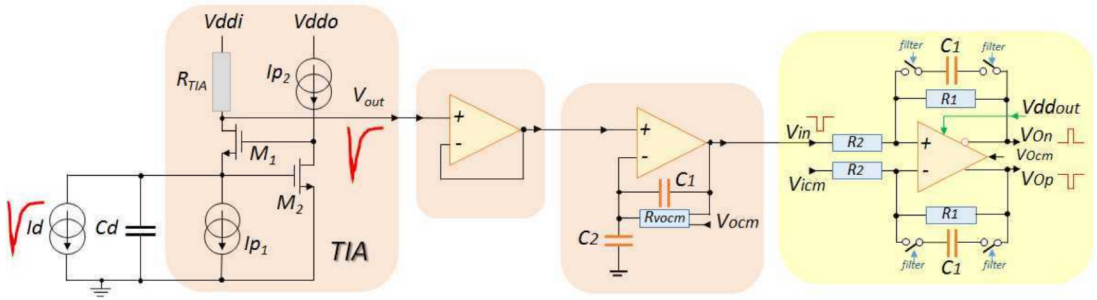
LVR

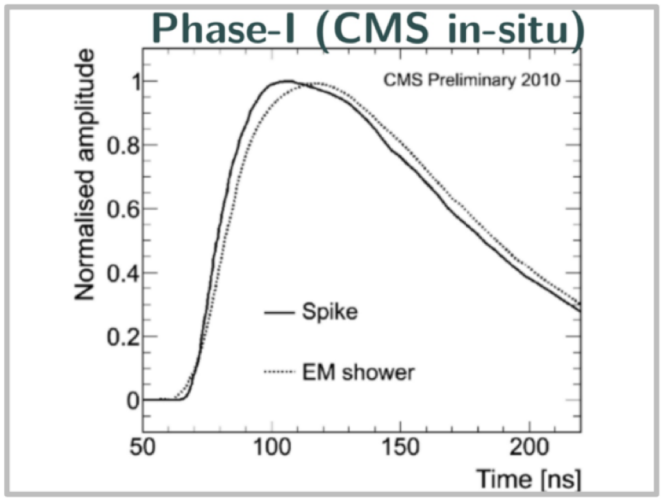
Rad-hard voltage regulator cards based on the Feast DC-DC converter

BCP

Barrel Calorimeter Processor. FPGA-based L1 primitive formation and readout cards (number, granularity)

# CATIA



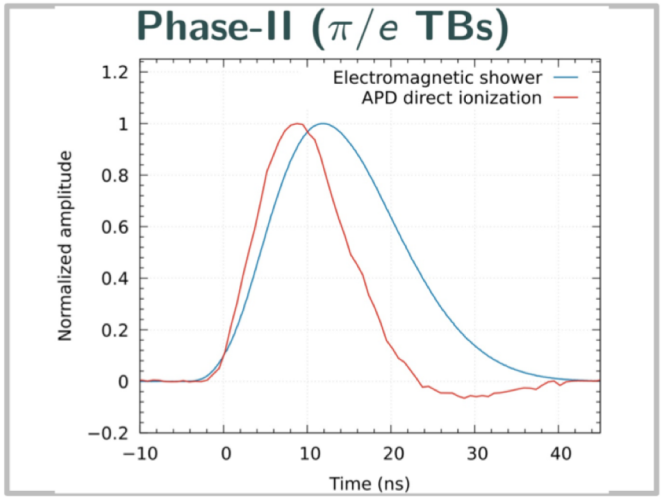




A Transimpedence Amplifier readout scheme

- 35 Mhz bandwidth
- 130 nm CMOS
- Each chip comprises a high-gain and a low-gain channel, test pulse injection, ADC calibration circuits.

V0 and V1 Tested with beam

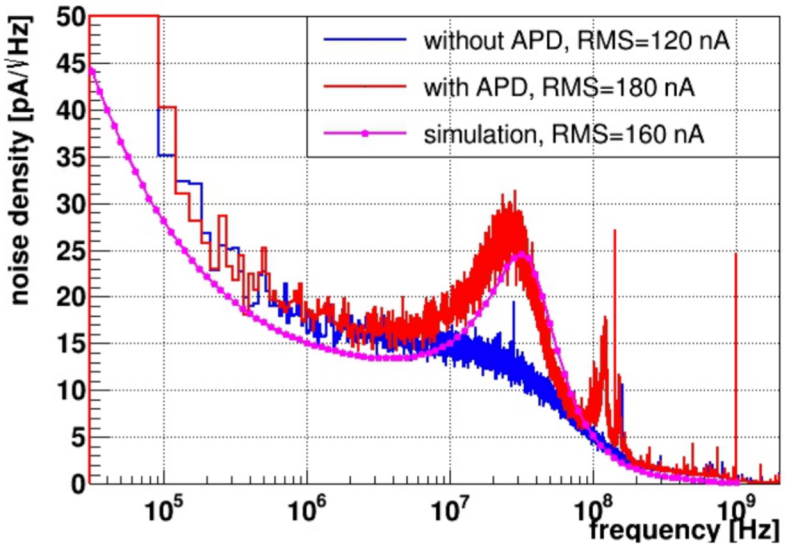
Faster response will allow for better spike identification and rejection and improve timing capabilities.

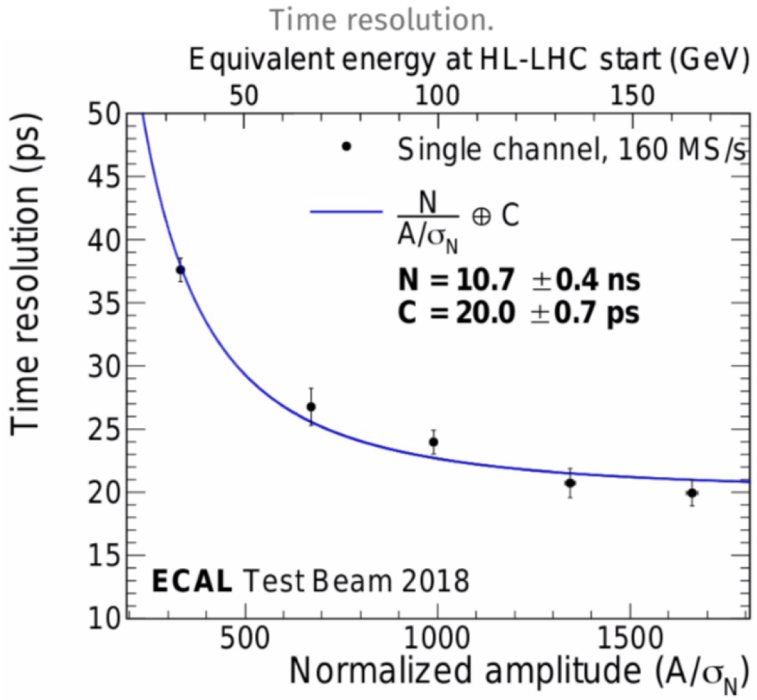


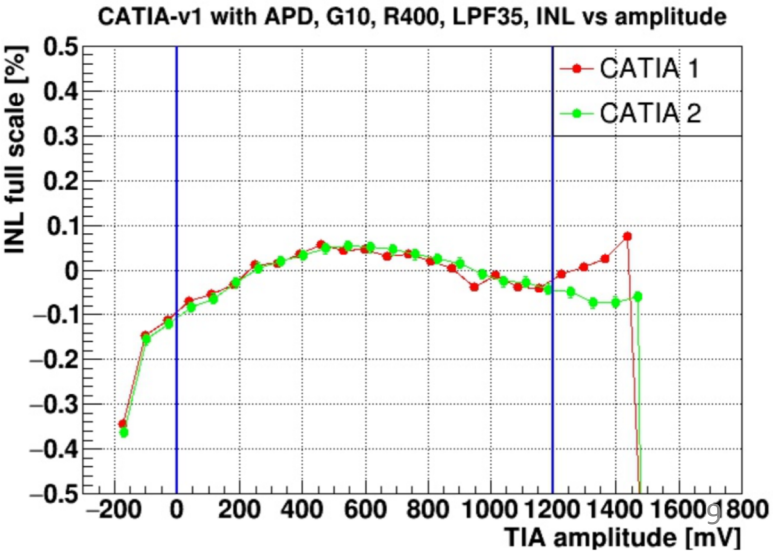
# CATIA results

Excellent performance has been obtained in terms of:

- Noise
- Linearity
- Time resolution

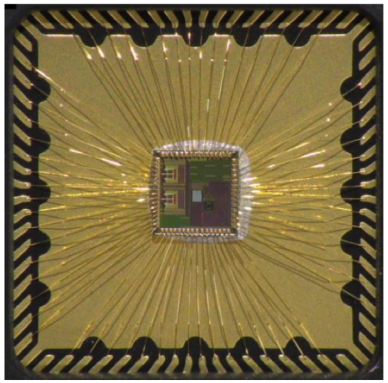


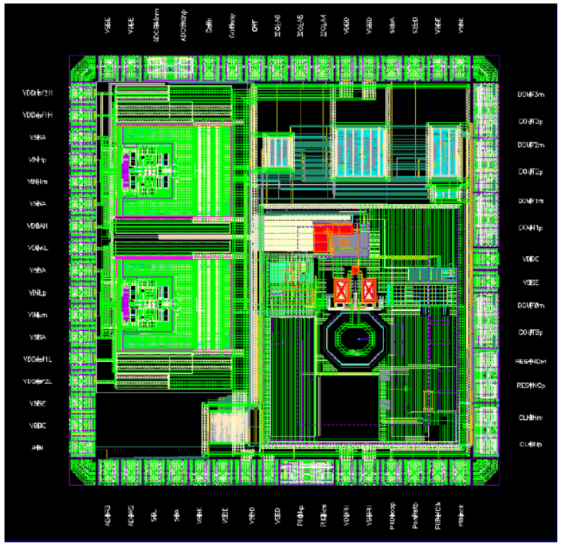



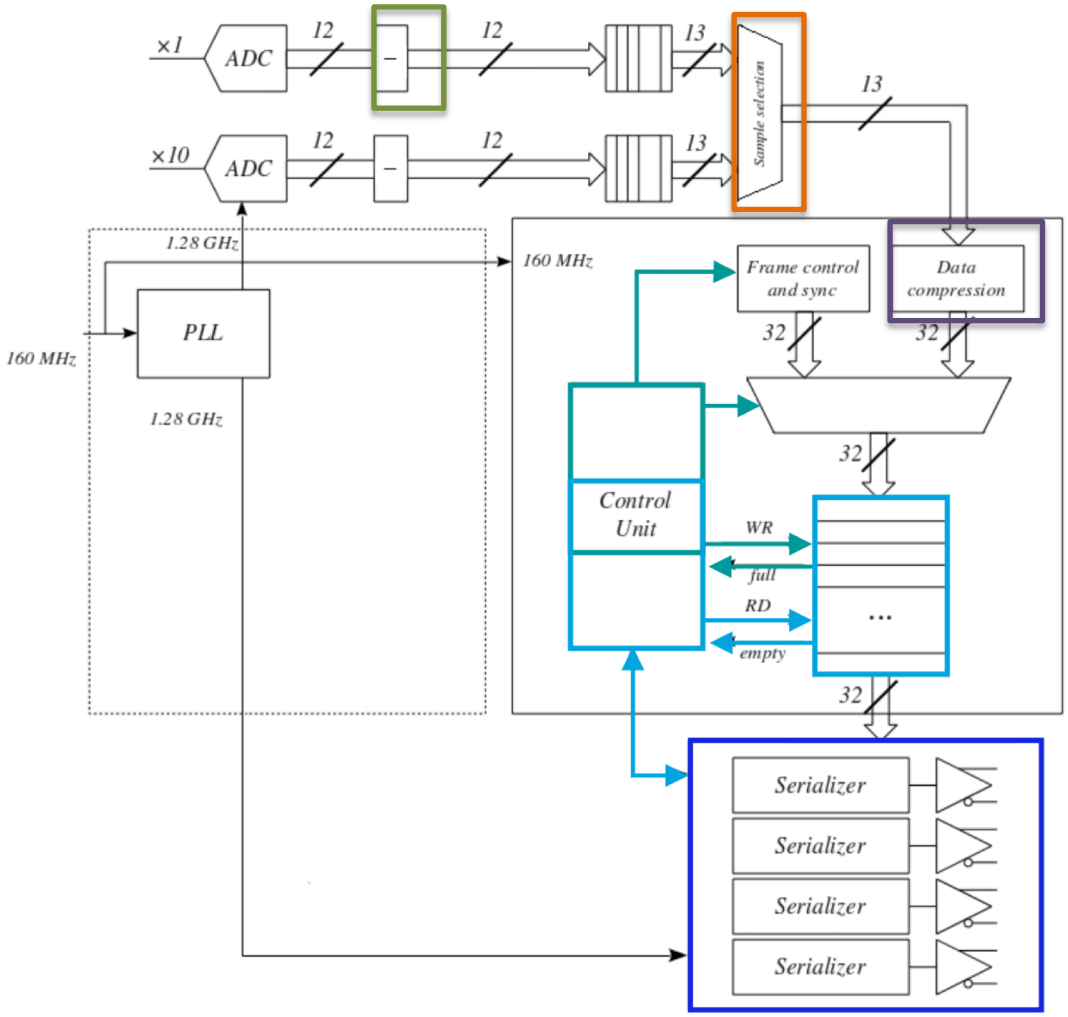
# LiTE-DTU

- Digital ASIC in 65 nm  CMOS technology
- 2x2 $mm^2$, 63 pads
- Includes 2x 12 bit, 160 Mhz ADC. IP block acquired from commercial company, specified for ENOB> 10.2 @ 50 MHz
- Data Transmission Unit implements baseline subtraction, gain selection, serialization and data compression logic
- PLL block from lpGBT
- TID Tolerance up to 100 kGy
- SEU-protected control logic

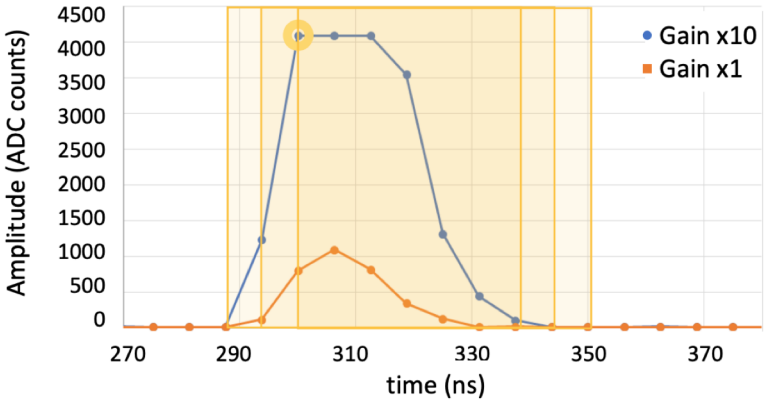




# LiTE-DTU



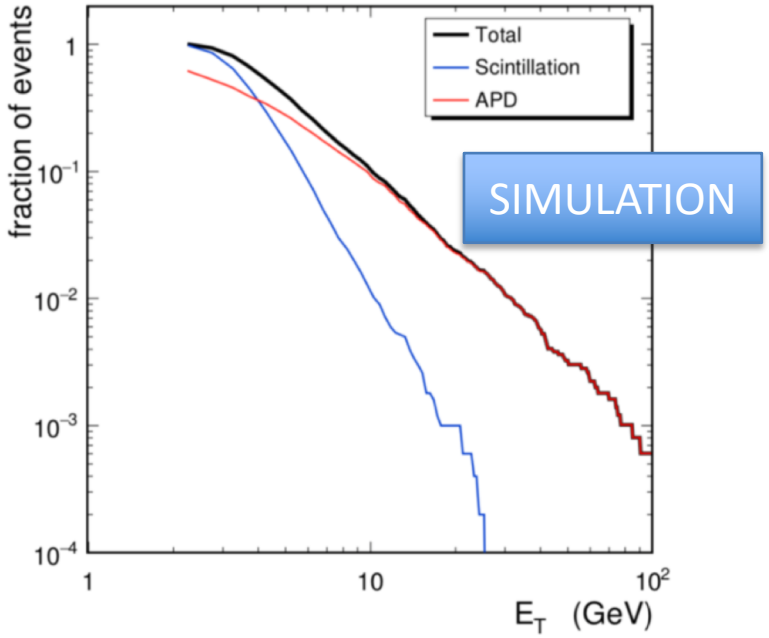

Arithmetic Baseline subtraction
Look-ahead gain selection
Data compression
Frame generation
Serial transmission



# LiTE-DTU: Data compression

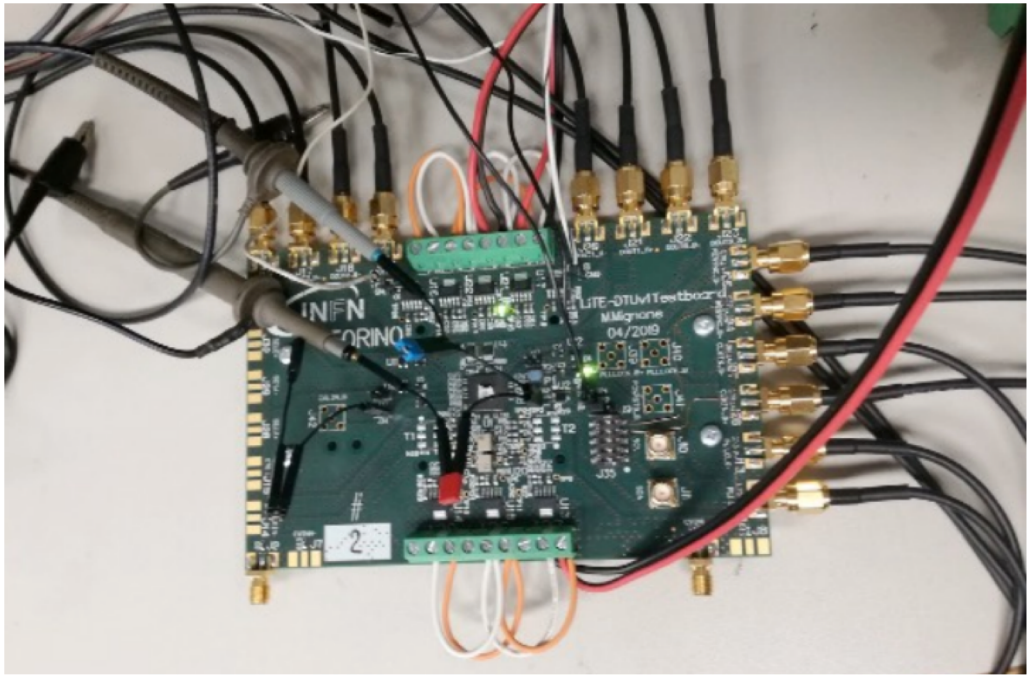
- With 12+1 bit words @ 160 MHz, the bandwidth occupation would be 2.08 Gb/s
- lpGBT e-link rate is 1.28 Gb/s
- The compression algorithm reduces the occupation down to 1.08 Gb/s
- Simplified Huffman encoding

The hit energy spectrum falls very rapidly, the majority of the transmitted samples will consist of noise or low-energy signals.
The compression algorithm uses 6 bits to encode signals of up to 2.5 GeV of energy, 12 bits above, while keeping latency < 350 ns



# LiTE-DTU: Status and tests

LiTE-DTU v1 currently under test




PLL

- Clock quality and jitter

ADC

- ADC noise and linearity
- TID irradiation tests
- SEU tolerance

Full ASIC

- Validation of the selection and compression algorithms
- Full system test with analog front-end
- “Vertical slice tests” foreseen for end 2020 with v2

# Front-End card prototype

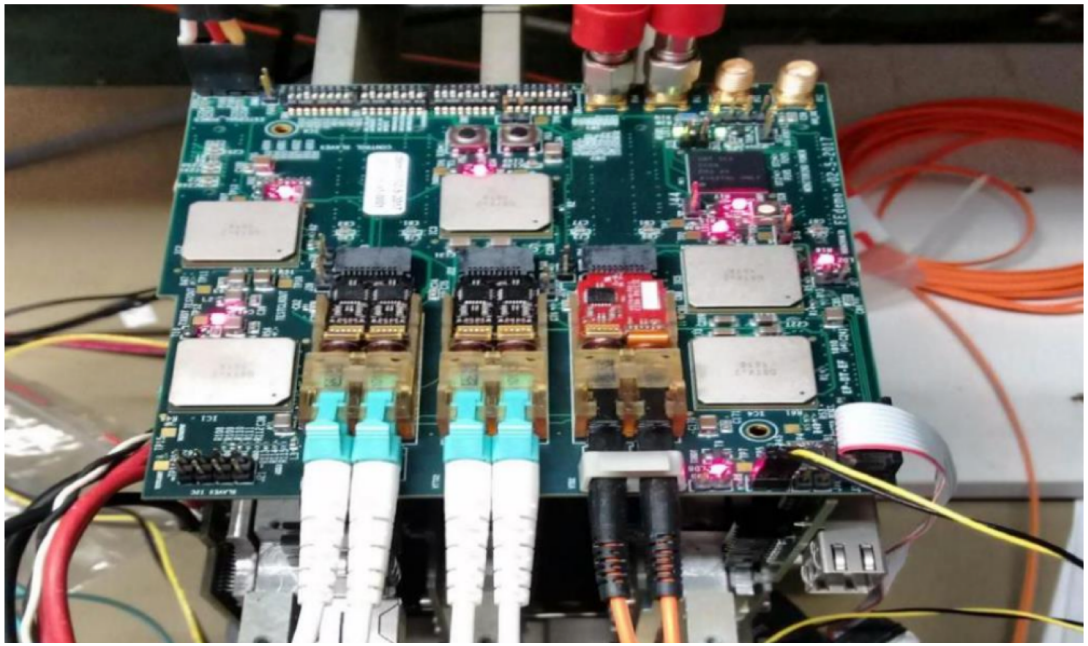
- Streaming of digitized data generated on the VFE cards to the CMS ECAL back-end electronics
- System initialization and control of all VFE components
- Precise clock distribution to all the VFE cards

**FE**

- 4 uplinks at 10.24 Gb/s (data links)
- 1 downlink at 2.56 Gb/s (control link)
- eLink serial interface to ADC, clock, and i2C interface

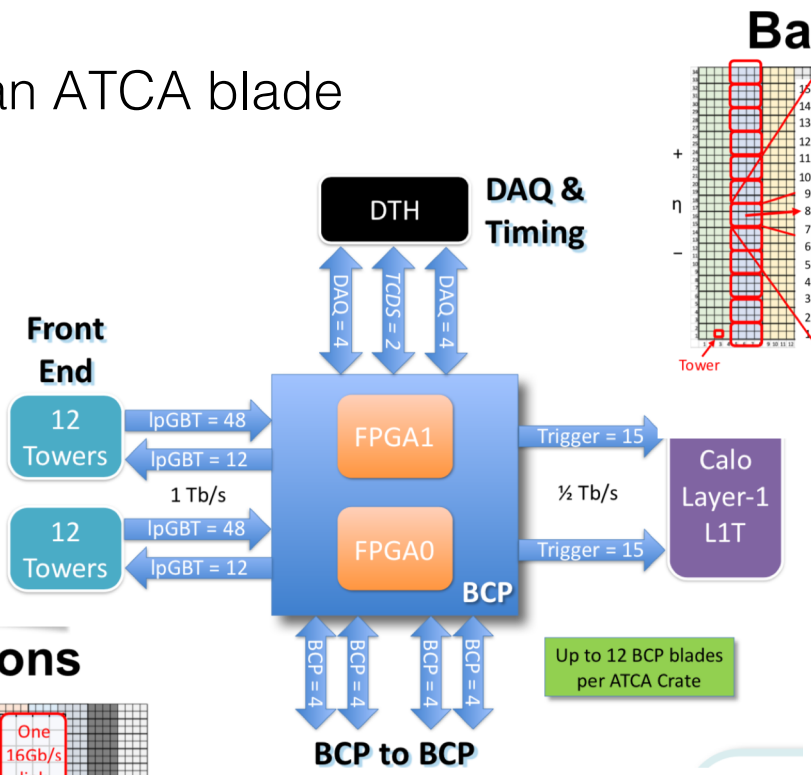
**v1 demonstrator**

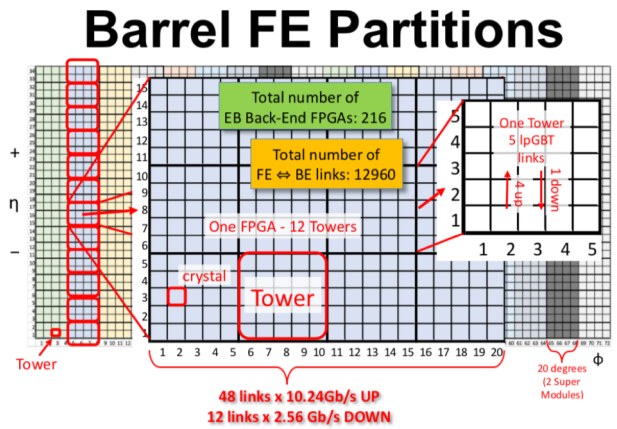
5 Gb/s links, GBTx based
1 VTRx + 2 VTTx VL modules

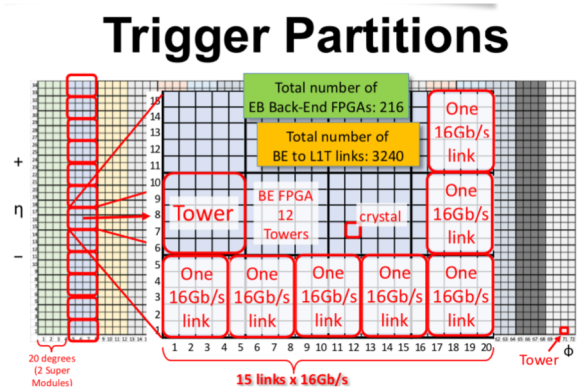


# Off-detector: Barrel Calorimeter Processor

- Trigger Primitive Formation, Clock distribution, Control and data readout, common for ECAL and HCAL
- Implemented as an ATCA blade
- FPGA-based



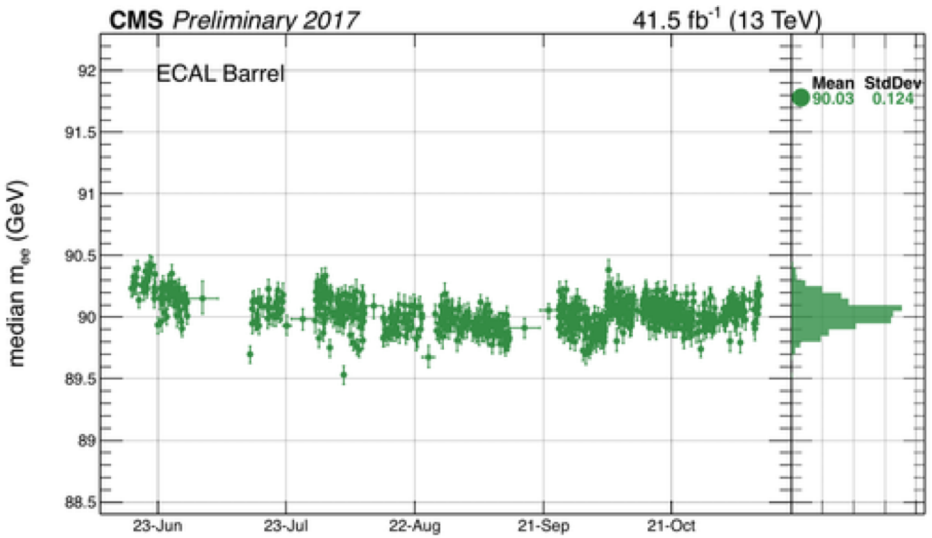



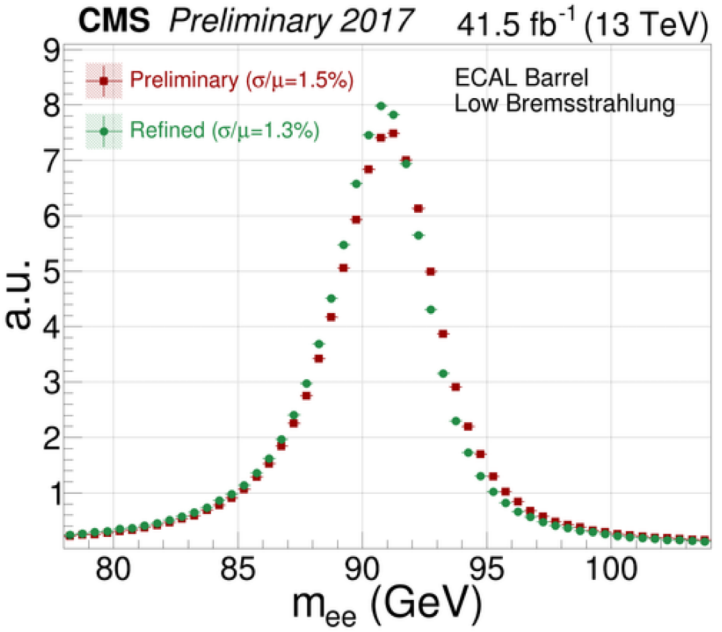



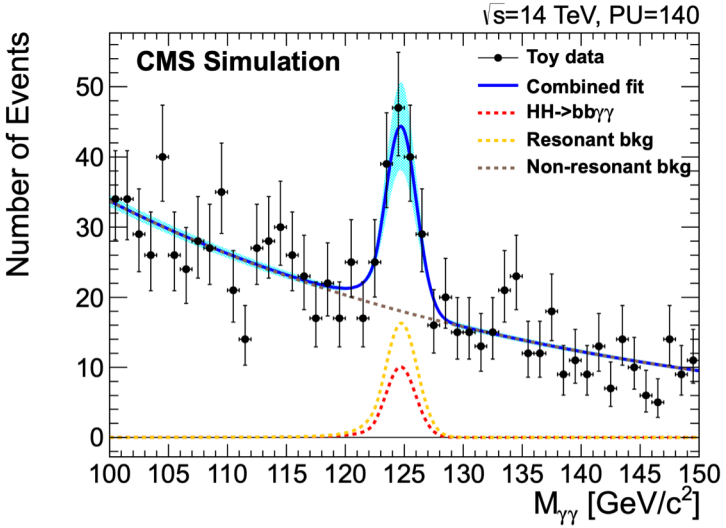
# Summary

- HL-LHC poses challenging demands on detectors, with a 4-5 fold increase in occupancy
- To maintain adequate performances, the ECAL Barrel readout must be improved with better time resolution and trigger flexibility
- For HL-LHC the readout will be completely replaced, while keeping the photosensors:
  - Faster analog electronics
  - Higher sampling rate
  - Full off-detector trigger primitive formation
- The upgrade project is well defined and prototypes have been extensively tested or are currently under test

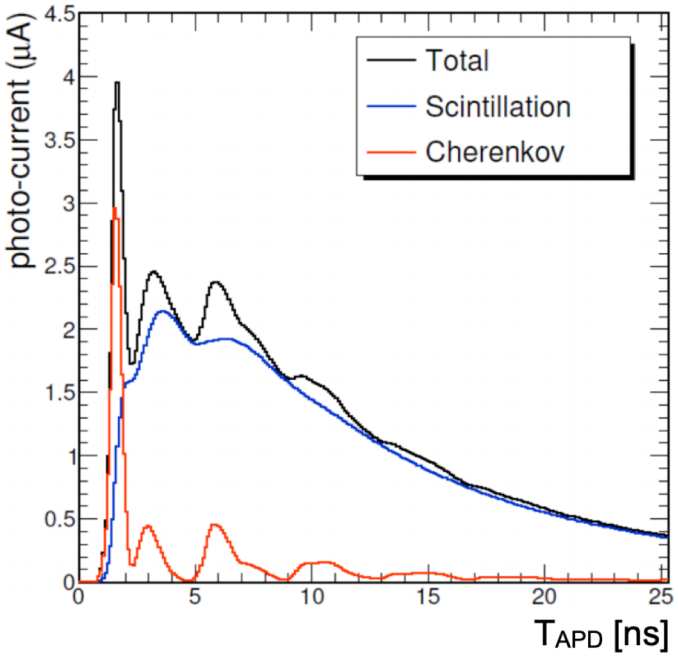
# Current and future performance

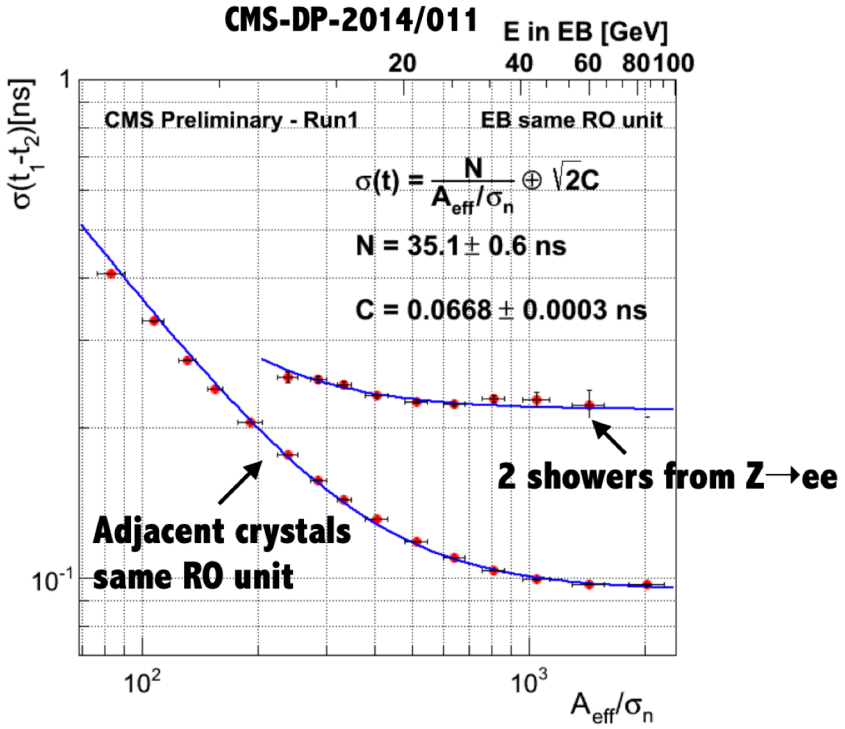


# Timing Performance



# APD dark current