Reliability studies for the Switching Core Board of the White Rabbit Switch: FIDES and Highly Accelerated Life Test

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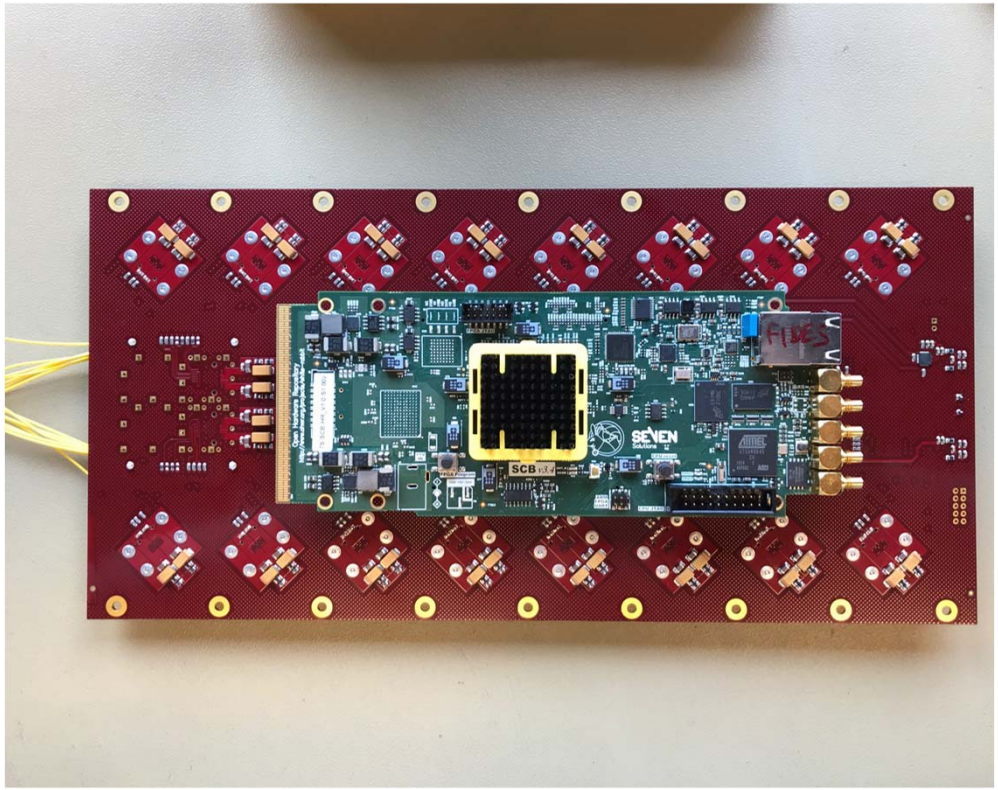
Validating the viability of standard White Rabbit technology in KM3NeT:

- Simplify the optical network
- Reducing the amount of electro-optical cables needed
- Easing the maintenance of the White Rabbit firmware and software

Switching Core Board and its carrier at the bottom of the DU Base.

High reliability -> Reliability assessment

SCB: Switching Core Board. Main board of the WRS.
Last version of the carrier: Modified for KM3NeT



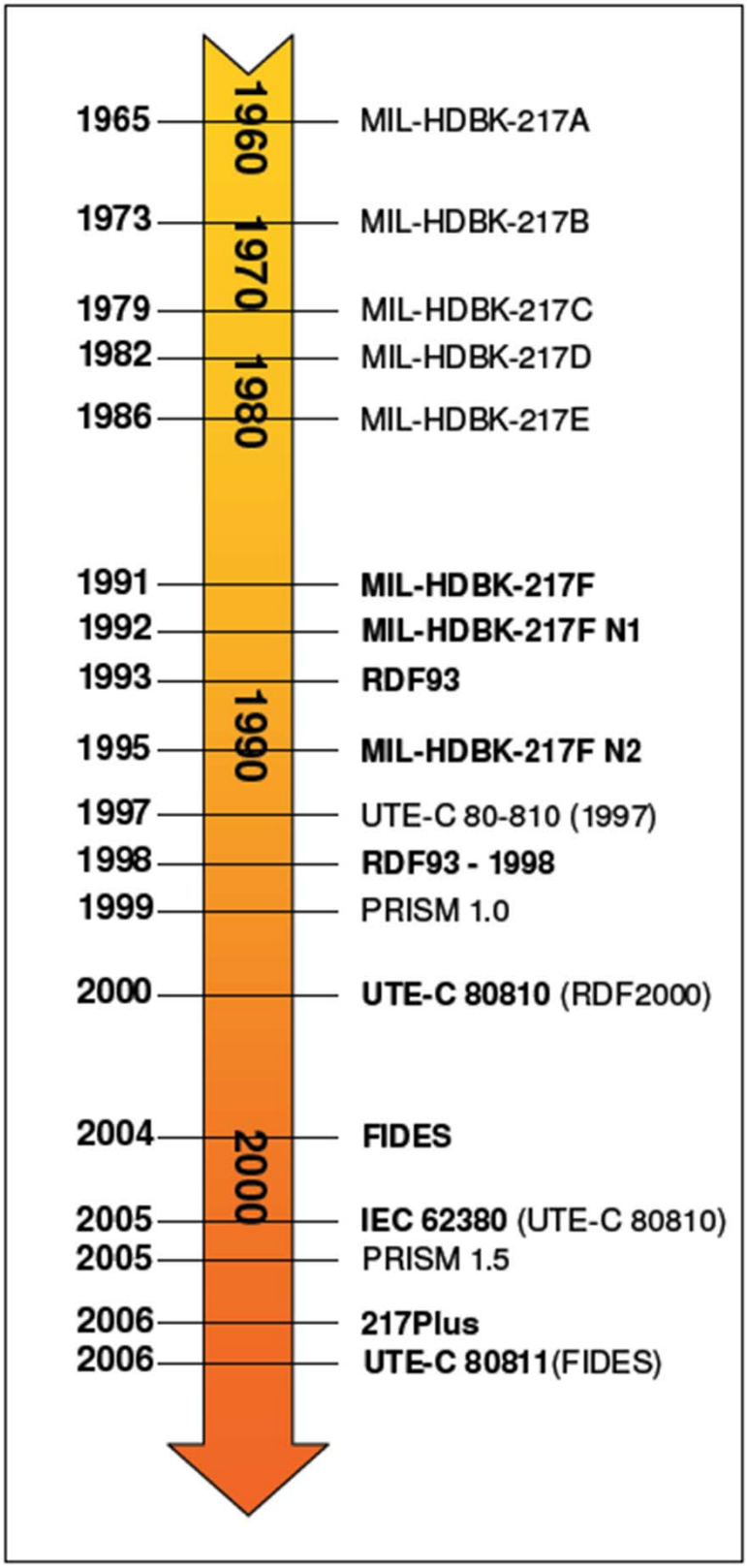
Reliability:

FIDES (theoretical procedure)

Applied already in KM3NeT Phase I

HALT (procedure)

Under application for PHASE II in combination with HASS tests -> Upgrading from ESS


1960
1970
1980
1990
2000
1965
MIL-HDBK-217A
1973
MIL-HDBK-217B
1979
MIL-HDBK-217C
1982
MIL-HDBK-217D
1986
MIL-HDBK-217E
1991
MIL-HDBK-217F
1992
MIL-HDBK-217F N1
1993
RDF93
1995
MIL-HDBK-217F N2
1997
UTE-C 80-810 (1997)
1998
RDF93 - 1998
1999
PRISM 1.0
2000
UTE-C 80810 (RDF2000)
2004
FIDES
2005
IEC 62380 (UTE-C 80810)
2005
PRISM 1.5
2006
217Plus
2006
UTE-C 80811(FIDES)

Why FIDES ?

The available Reliability Data book prediction are obsolete => because they do not cover actual component technologies and state of the art of acceleration laws (i.e. MIL-HDBK-217 is not maintained since 1995)

New economics challenges need to know realistic system reliability to engage many years lump support contracts with customers

How FIDES was created ?

Funding by DGA (French MoD) and eight international companies in 2001

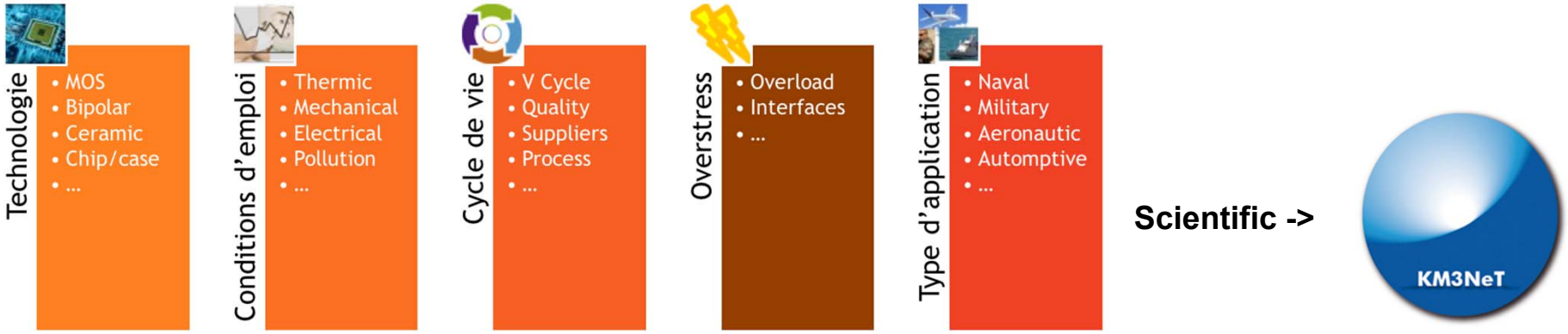
These 8 companies joined their efforts to create a new predictive reliability methodology based on Physic Of Failure

FIDES handbook (2009) developed by:

- Airbus France, Eurocopter, Nexter Electronics, MBDA missile systems (chef de projet), THALES Avionics, THALES Services SAS, THALES Systèmes Aéroportés, THALES Underwater Systems,
- And by DGA (development fund providing)
- GTR Fides open to all users Don’t hesitate to contribute

FIDES methodology:

- Include most recent technologies
- Consider all factors that could affect reliability



WR SWITCH			
Original Design		KM3NeT Upgrade	
WR SCB			
FIT	MTBF	FIT	MTBF
2937	340483	794	1259445
Chromium board (carrier)			
FIT	MTBF	FIT	MTBF
639	1564945	435	2298850
TOTAL		TOTAL	
3576	279642	1229	813669

Mainly due to decoupling capacitors. Better part choice.

290 % improvement in the reliability of the WRS

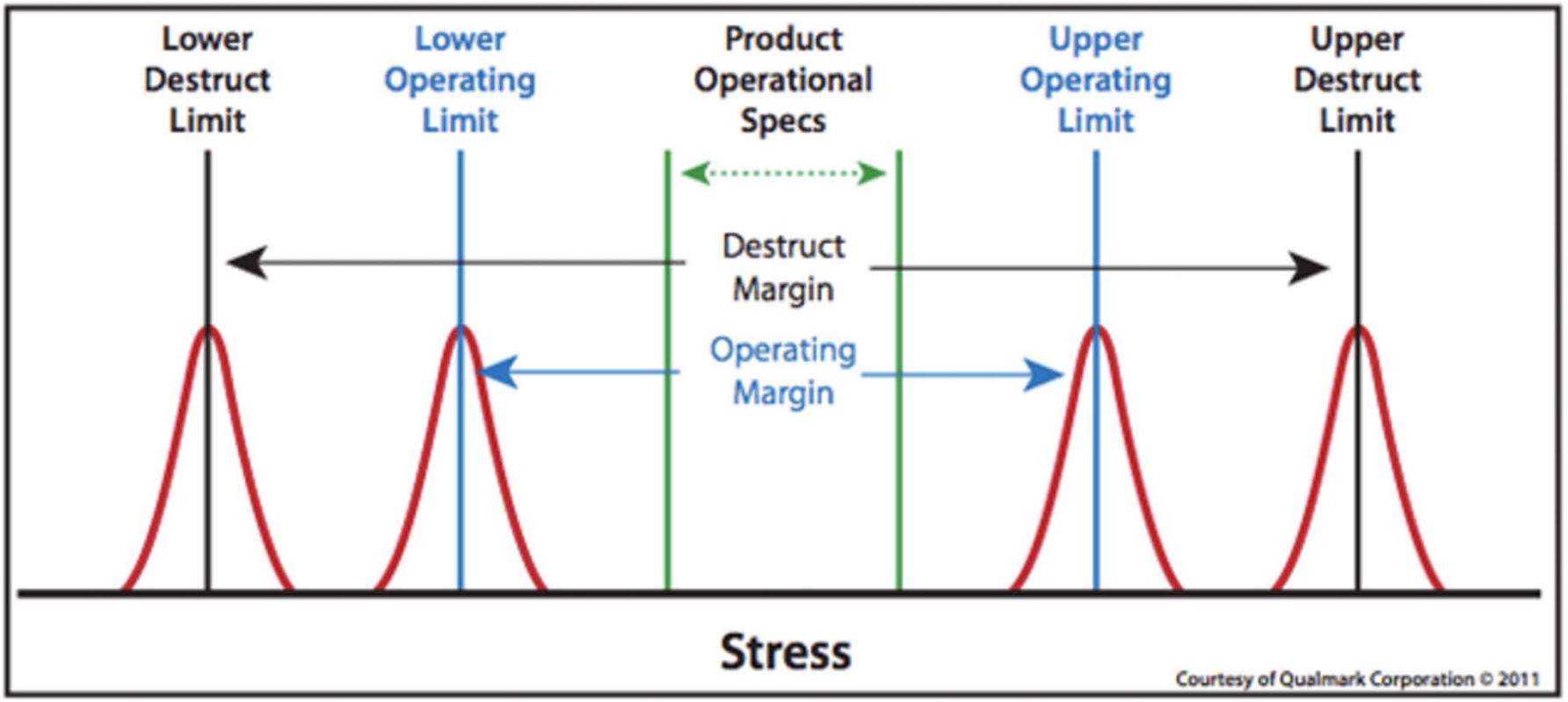
Highly Accelerated Life Test (HALT) is a design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits. The main idea is to find **weak points** in the **design** in an **early stage** in order to correct them and **improve and optimize the design in a reliable way**

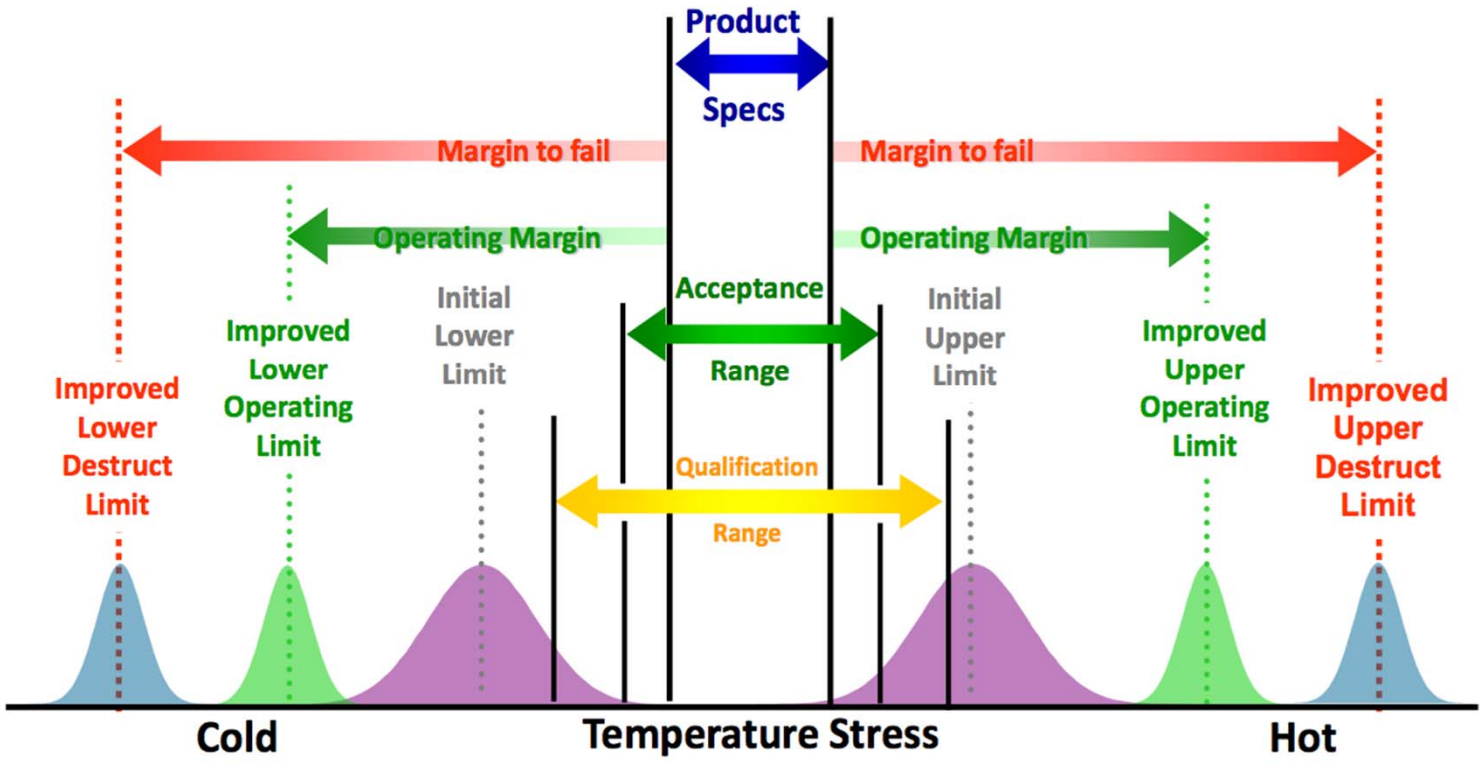
This applies only to a few boards in the design stage. Ideally to a set of 4 to 6 boards

Early Fault Detection is Key

At the 1998 Nepcon show Hiroshi Hamada, then Ricoh's chairman, estimated the cost of finding and fixing a product fault. In today's dollars, those estimates show the value in early product failure detection:

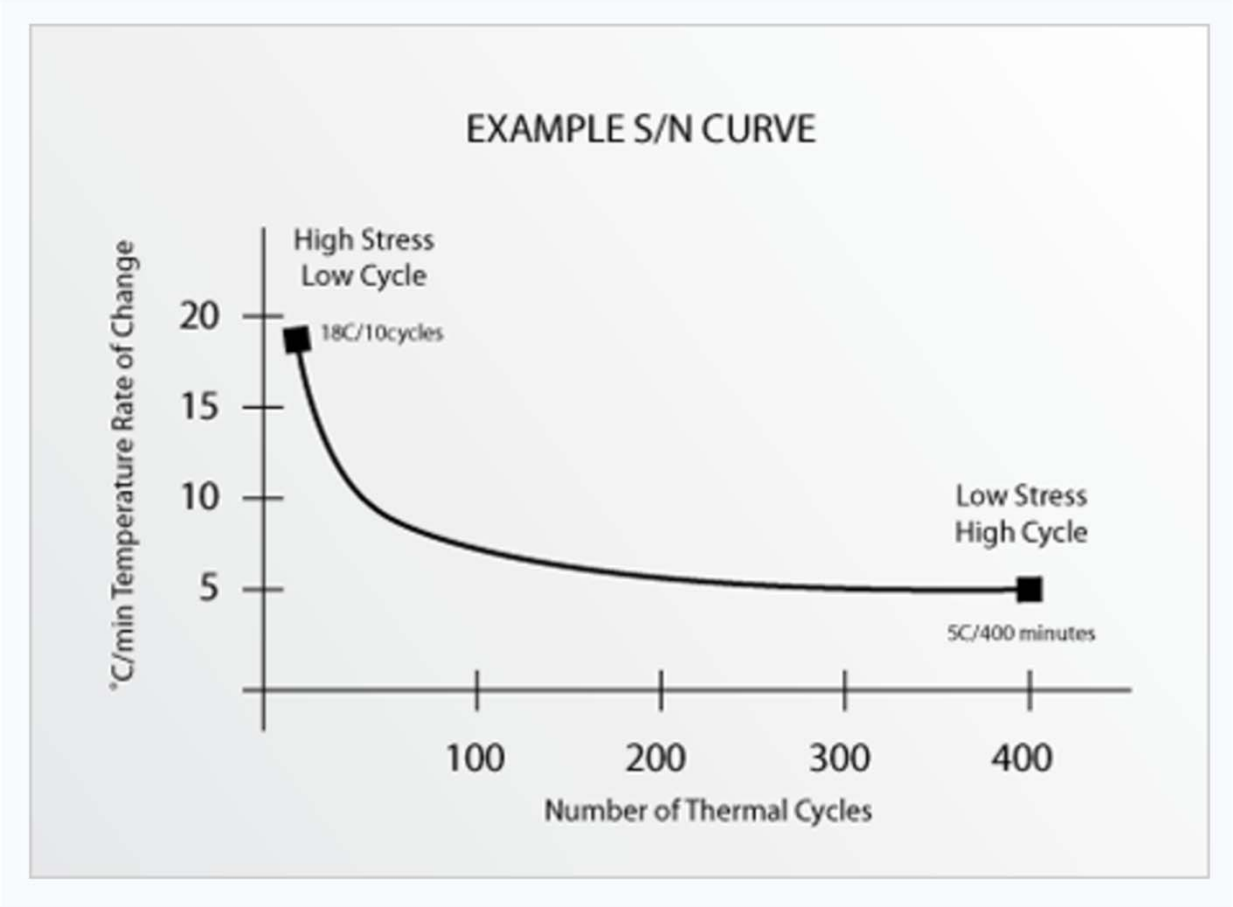
$46 - During design phase
$228 - Before procurement
$480 - Before production
$22,000 - Before shipment
$900,000 - On customer site


Lower Destruct Limit
Lower Operating Limit
Product Operational Specs
Upper Operating Limit
Upper Destruct Limit
Destruct Margin
Operating Margin
Stress
Courtesy of Qualmark Corporation © 2011


Product
Specs
Margin to fail
Margin to fail
Operating Margin
Operating Margin
Acceptance
Range
Initial
Lower
Limit
Initial
Upper
Limit
Improved
Lower
Operating
Limit
Improved
Upper
Operating
Limit
Improved
Lower
Destruct
Limit
Improved
Upper
Destruct
Limit
Qualification
Range
Cold
Temperature Stress
Hot

Usually HALT tests can be implemented using several kinds of stresses such as thermal extremes, extremes thermal rates of change, vibration and the combination of thermal and vibration. Moreover, it could be used other types of stress such as frequency margin, power supply loading, voltage margin or power cycling.

The higher the stress the lower the number of cycles



For KM3NeT will be use, thermal extremes, extremes thermal rates, and power cycling as minimum tests. Vibration, combined vibration plus extreme temperature rates of change are left as an option, recommended when possible

Constrains: time, money


Stress
(increase)
Failure
Increase stress
and start process
over
Analysis
Improve

TEST At KM3NeT Minimum tests:

1. **Thermal Extremes Stress:** Starting at the ambient temperature
2. **Thermal Extremes Stress:** Decreasing temperature at slow pace (5 degrees per step, at a rate lower than 1º/min) until the limits of the chamber(Phase I applied to CLB+PB). Allow stabilization of the temperature for 10 minutes at each step.
3. **Thermal Extremes Stress:** Increasing temperature at slow pace (5 degrees per step, at a rate lower than 1º/min) until the limits of the chamber (Phase I applied to CLB+PB). Allow stabilization of the temperature for 10 minutes at each step.
4. **Extremes Thermal Rates:** From initial temperature (ambient temperature) ramp quickly the minimum functional temperature detected in point 2 - or to the lowest temperature possible of the chamber-. The rates higher than 1 º / min.
5. **Extremes Thermal Rates:** From initial temperature (ambient temperature) ramp quickly to the maximum functional temperature detected in point 3 - or to the highest temperature possible of the chamber-. The rates higher than 1 º / min.

Optional tests:

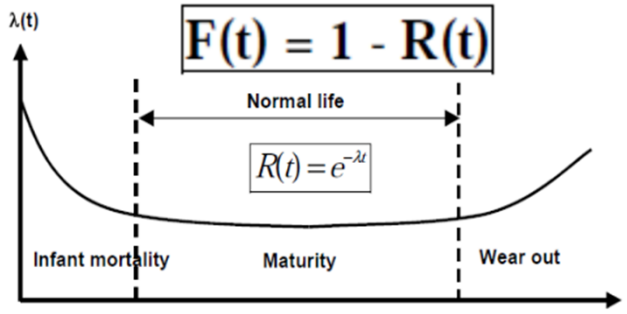
1. **Vibration Stress:** Perform vibration tests.
2. **Vibration + Temperature Stress.**

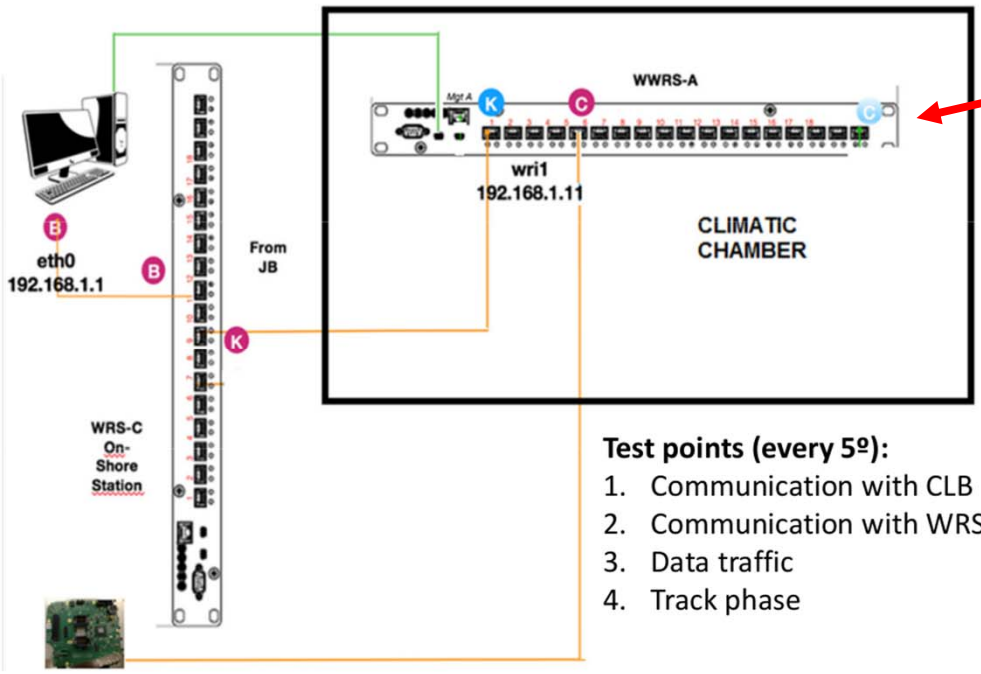
Performing HALT

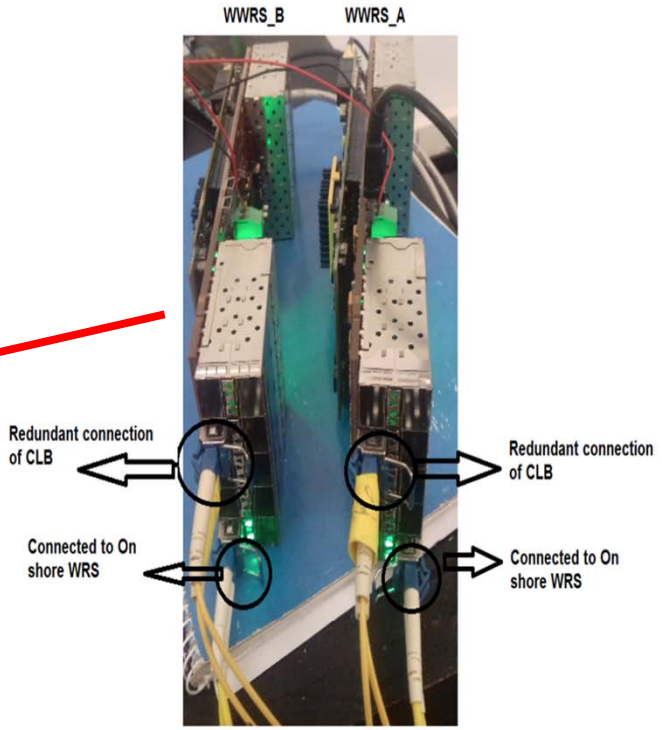
- HALT testing of WWRS is performed in a climatic chamber. It must be possible to apply incremental increases (and decreases) in temperature to levels in excess of those specified for normal product operation.
- During testing, it is essential to exercise product operation and ensure functionality. Test setups should be optimized to maximize functional test coverage.
- The test setup should also allow for remote operation of the test and product from outside of the environmental chamber.

HALT defines HASS

- HASS tests are introduced to catch in a quick way those failures added during production that are not related to a faulty design
- The limits of temperature (and vibration if chosen) are set taking into account the HALT tests and the normal operating limits. The goal is to apply partial or limited stress to the product in order to avoid early failure.
- Usually the limits are reviewed during the life of the devices to ensure that there is not under or over stress.







Test points (every 5º):

1. Communication with CLB
2. Communication with WRS in the chamber
3. Data traffic
4. Track phase

Two series of HALT performed:

a) 2 WWRS (SCB + Chromium) prototypes tested
    i) A unexpected failure found around 0 Celsius degrees
b) A design on the carrier identified and corrected. More prototypes produced.
c) 2 new WWRS (SCB + Chromium) prototypes tested
    i) Operational in a wider range (-40 to 100 Celsius degrees)
d) A third and final (?) HALT to take place in the coming weeks to end the validation of the WWRS.

1. First round of HALT: Thermal Extremes Stress

	WWRS-A (degrees)	WWRS-B (degrees)	*Mean (degrees)*	HASS (80% OL) (degrees)	ESS -Burn-in limits at KM3NeT (degrees)
UOL -Upper Operating Limit	100	95	*97.5*	**78**	65
UDL- Upper Destructive Limit	100	95	*97.5*		
LOL - Lower Operating Limit	5	-5	*0*	**5**	0
LDL - Lower Destructive Limit	-40	-5	*-22.2*		

When the transceivers failed permanently is not clear. We assume the worst case, when the fist failure appeared. On the LDL of WWRS-A we take the minimum temperature applied to the WWRS, as the boot failure did not cause a permanent failure on the board.

Boards failed at a unexpected temperature.

First round of HALT: Thermal Extremes Rates

The thermal extreme rates were also implemented. It was implemented for one surviving swicth going form LOL to UOL and viceversa, performing well

WWRS includes a CP2105 UART with floating signals when no USB is plugged. These lines are connected to the ARM processor.

Temperature influences a leakage current on the ARM processor affecting the floating voltage.

Solution: Add a pull-up resistor in the line to avoid floating voltage.

1. Second round of HALT: Thermal Extremes Stress

	WWRS-A (Celsius degrees)	WWRS-B (Celsius degrees)	*Mean (Celsius degrees)*	HASS (80% OL) (Celsius degrees)	ESS -Burn-in limits at KM3NeT (Celsius degrees)
UOL -Upper Operating Limit	95	100	*97.5*	**78**	65
UDL- Upper Destructive Limit	95	100	*97.5*		
LOL - Lower Operating Limit	-40	-40	*0*	**-32**	0
LDL - Lower Destructive Limit	-40 (chamber limit)	-40 (chamber limit)	*-40*	-32	

As in the previous case, when the transceivers failed permanently is not clear. We assume the worst case, when the first failure appeared

The boards remained functional at -40 degrees, the lower temperature provided by the chamber

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Second round of HALT: Thermal Extremes Rates

The thermal extreme rates were also implemented. It was implemented for one surviving switch going from LOL to UOL and vice versa, performing well

CONCLUSIONS:

WWRS: A White Rabbit Switch at the Bottom of KM3NeT DUs under evaluation -> High reliability needed

KM3NeT reliability tools: **FIDES and HALT**

FIDES, theoretical tool, applied to WWRS: FIDES modifications result in a three fold reliability improvement with respect original version of the WRS

HALT, practical tool, applied to WWRS (**after the implementation of FIDES modifications**): Detected a hidden problem in the design. Once corrected, HALT characterizes the operational limits of the board.

Reliability of the WWRS improved

Final HALT tests to be performed soon