A multichannel front-end readout ASIC for high flux and high time resolution applications with UFSD

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Topical Seminar on Innovative Particle and Radiation Detectors

Siena 17th October 2019

OUTLINE

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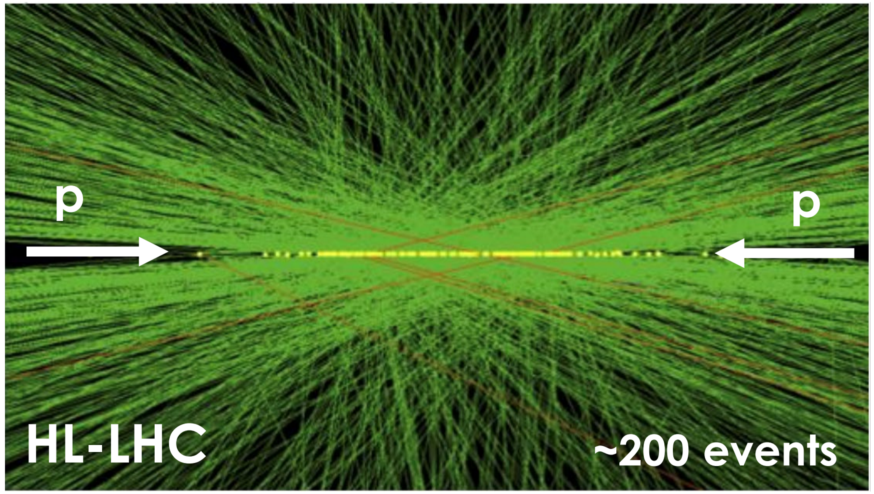
Motivation

Picosecond time resolution in High Energy Physics

Why picosecond time resolution is needed?



- At HL-LHC are expected**150-200 events per bunch crossing**
- The reconstruction of time information allows to distinguish among events overlapped in space
- Timing is included in future experiments in different ways:
  - **Timing layers**
  - **4D detectors**: timing is measured for each point along the track
- In medical applications: PET (time resolution), proton therapy (high rates)

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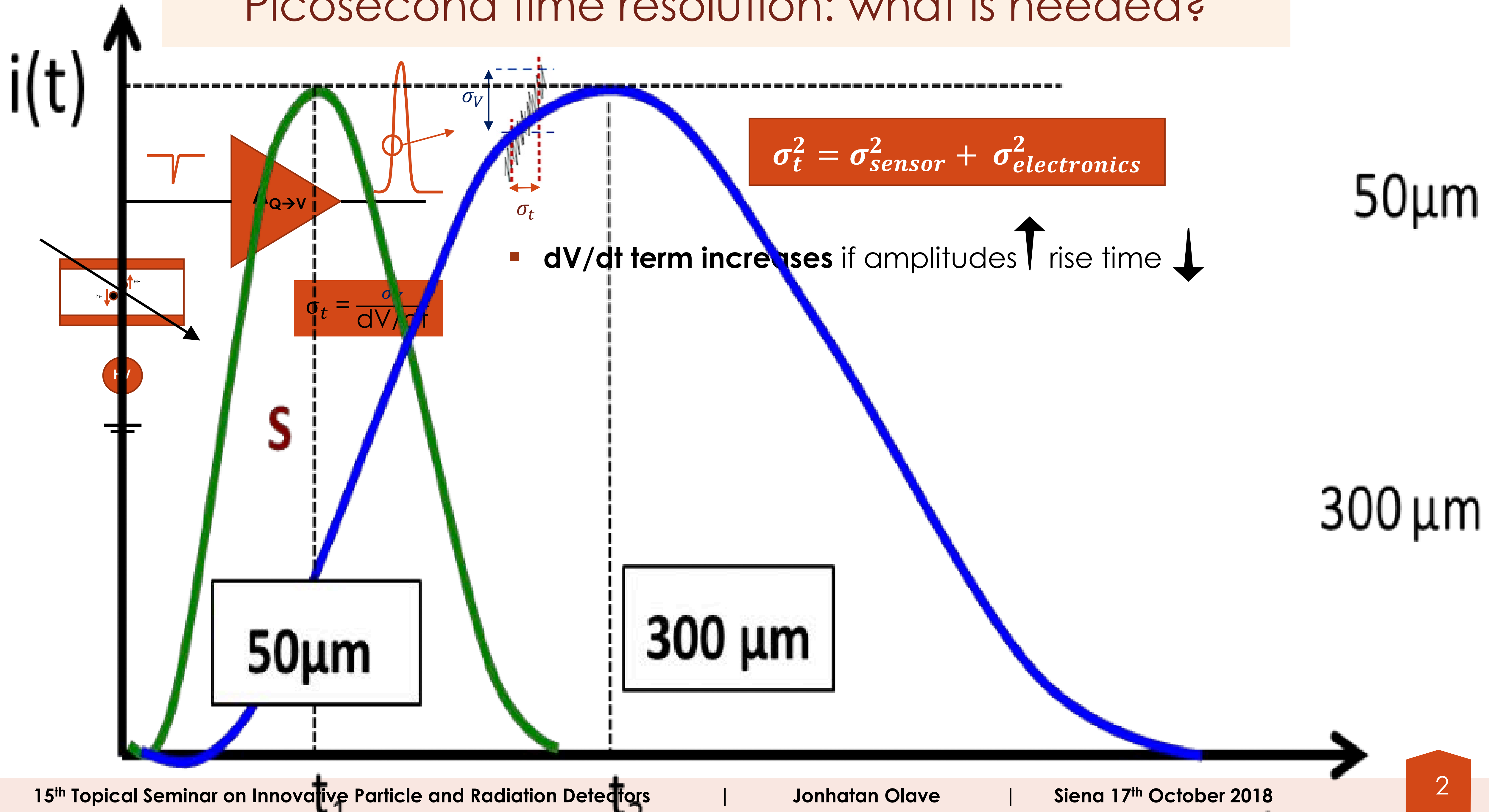
Picosecond time resolution

What is really needed?

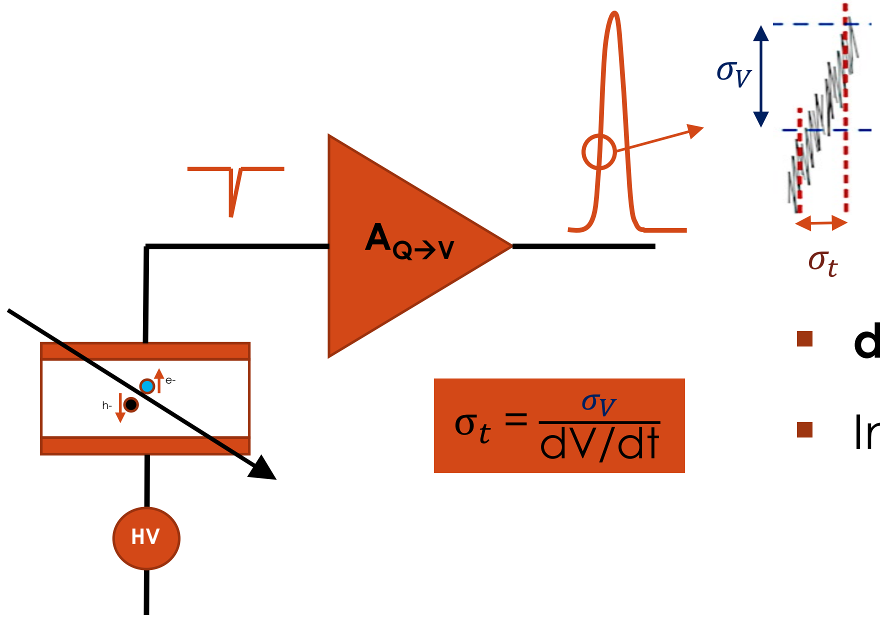
Picosecond time resolution: what is needed?



$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{electronics}^2$$

- **dV/dt term increases** if amplitudes ↑ rise time ↓

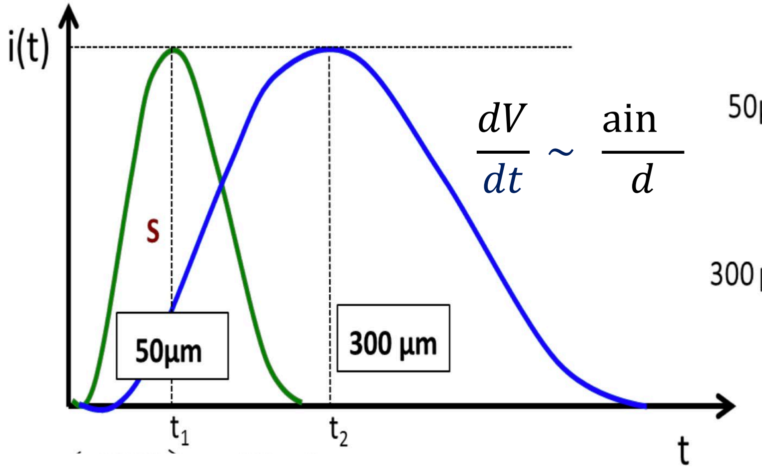
Picosecond time resolution: what is needed?

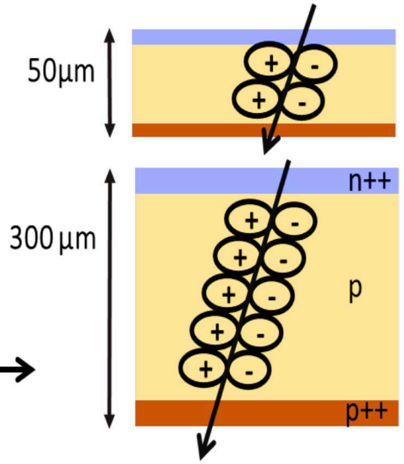


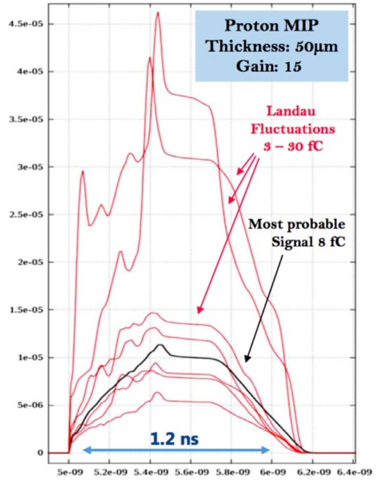
$$\sigma_t = \frac{\sigma_V}{dV/dt}$$

$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{electronics}^2$$

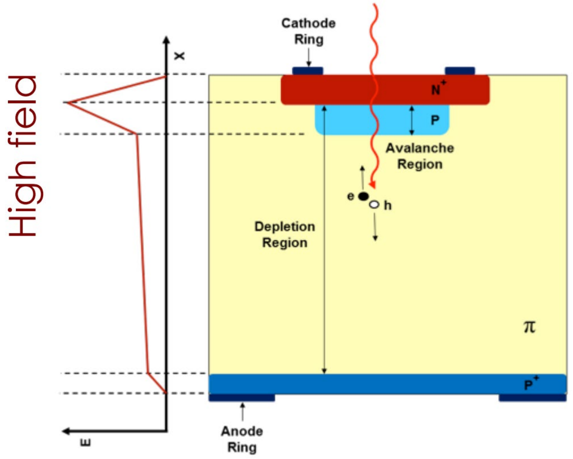
- **dV/dt term increases** if amplitudes ↑ rise time ↓
- In UFSD sensors :
  - **Large amplitudes** are obtained with the **gain**
  - **Short rise time** is obtained with **thin** sensors







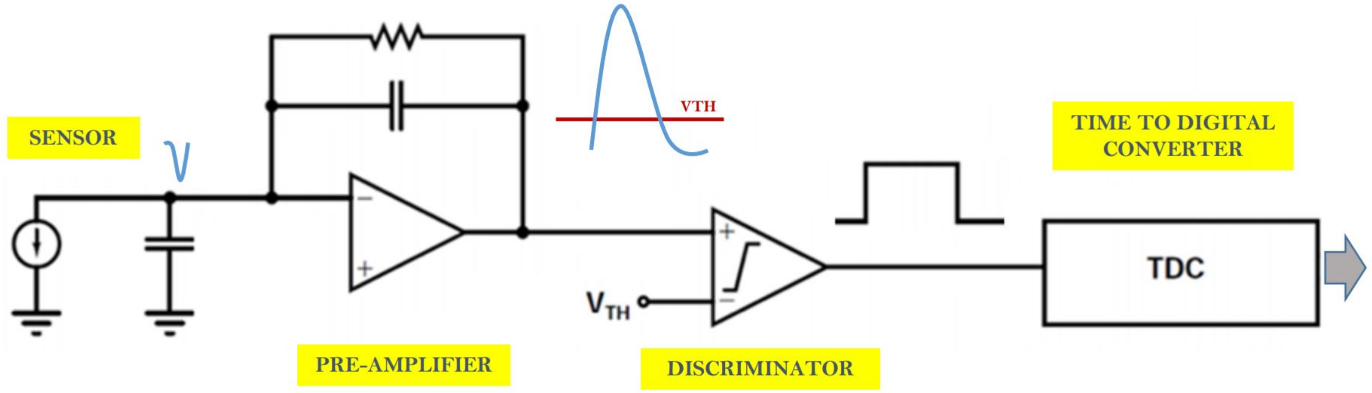
UFSD*



(*) H. Sadrozinski et al, *4D tracking with ultra-fast silicon detectors*, Reports on Progress in Physics, 2-026101-2018

Picosecond time resolution: what is needed?

Fast front-end electronics



- **Jitter** is minimized minimizing noise and increasing the dV/dt term
- Noise can be minimized in case: $\mathbf{T_{rise} \sim T_{collection}}$
- Noise depends on several factors like: **sensor cap, bandwidth, front-end topology**
- Electronics contribution: front-end, TDC and the time walk

Front end TDC Sensor

$$\sigma_t^2 = \left(\frac{N}{\frac{dV}{dt}}\right)^2 + \left(\frac{\delta_{Bin}}{\sqrt{12}}\right)^2 + \sigma_{Time\ Walk}^2$$

- The contribution from TDC is very small compared to the other terms
- **Time walk** can be reduced by using **CFD** or it can be corrected offline with particular techniques
- Going to the transistor level, time resolution is technology dependent

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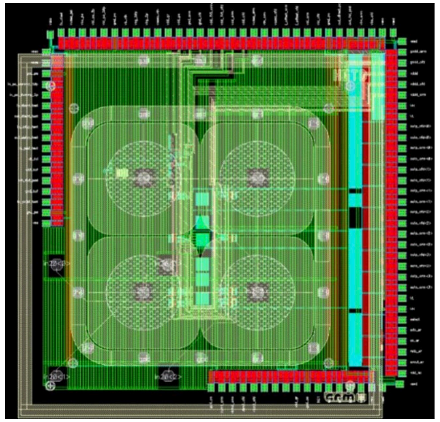
Picosecond ASICs

State of the art

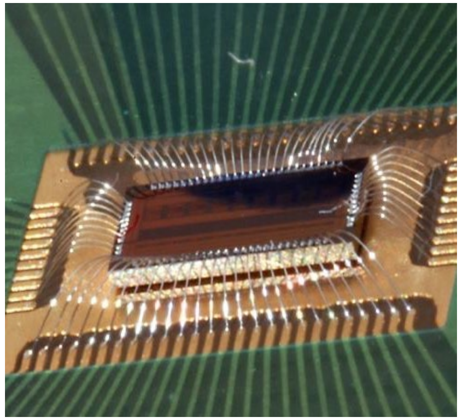
Examples of fast front end electronics

ALTIROC0 (OMEGA)



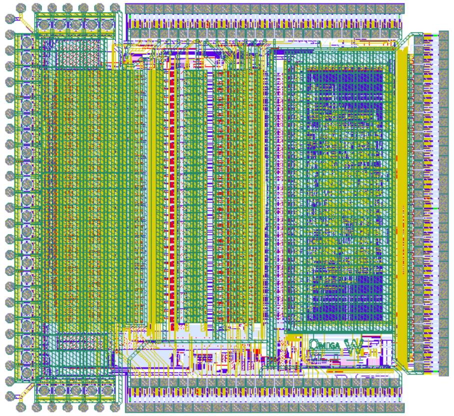
Sensor: LGAD 3.4 pF
TR = 48 ps
Power = 5 mW/ch
Qin= 3fC – 30fC
CHs: 8
Tech: CMOS 0.18um

NINO (CERN)



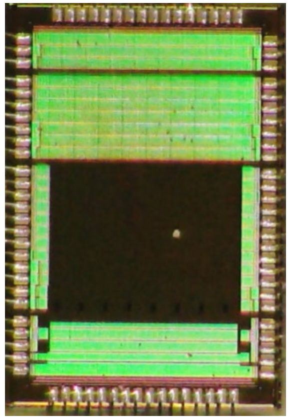
Sensor: SiPM
Jitter = 10 ps
Power = 27 mW/ch
Qin= 30 fC – 2 pC
CHs: 8
Tech: CMOS 0.25um

PETIROC2 (OMEGA)



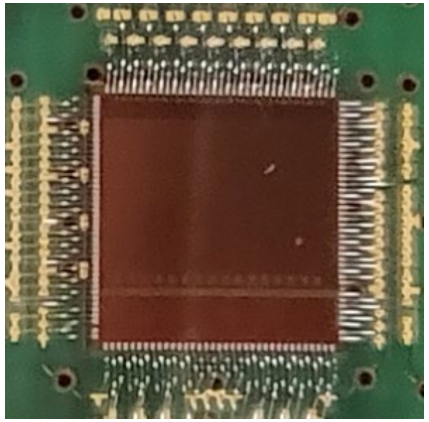
Sensor: SiPM
TR = 20–30 ps
Power= 6 mW/CH
Qin= 160 fC-400pC
CHs: 32
Tech: SiGe 0.35um

TOFFEE (TORINO)



Sensor: LGAD 3/6 pF
TR = 50 ps
Power= 12 mW/ch
Qin= 3fC-30fC
CHs: 8
Tech: CMOS 0.11um

TOFHIR (LIP)



Sensor: SiPM
TR = 30 ps
Power= 8 mW/ch
CHs: 16
Tech: CMOS 0.11um

It's quite difficult to combine the requiments of timing with sensor size and power

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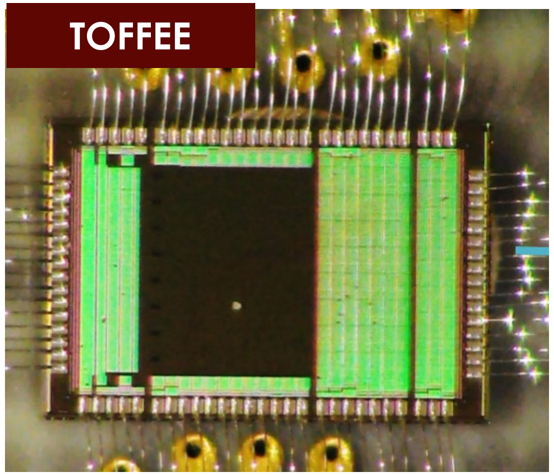
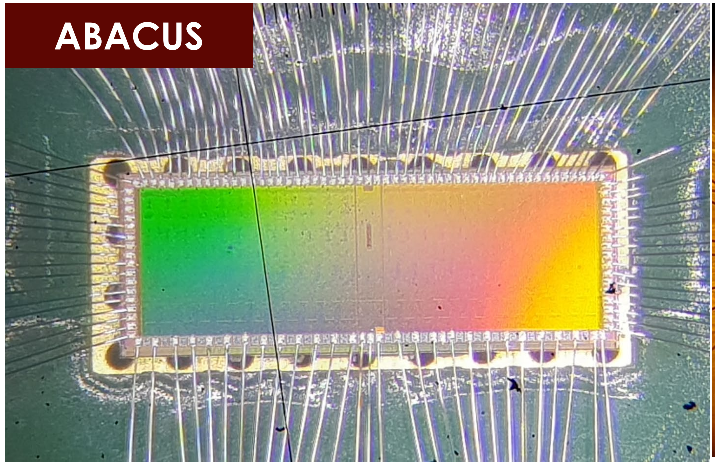
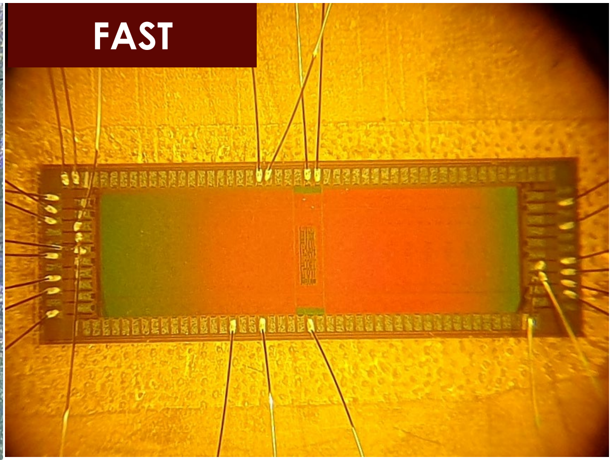
The FAST prototypes

General ASICs description

ASICs developed for applications with UFSD







Developed @ INFN-Torino

TIME

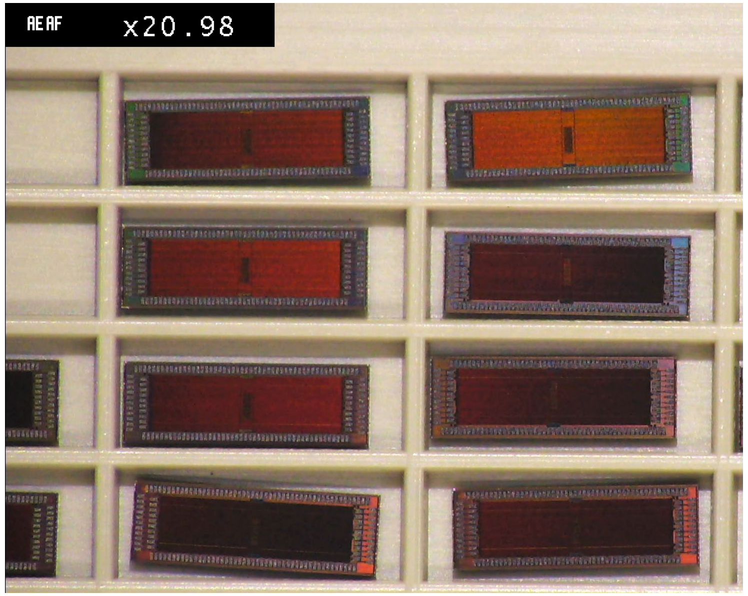
ASIC	Application	#ch	mm^2	mW/ch	technology	FoM	Production
TOFFEE	Timing	8	3.6x2.5	20	110nm	45 ps (8 fC MIP)	2016
ABACUS	Single ion counting	24	5x2	15	110nm	3-130 fC Qin @ 100 MHz	2018
FAST	Timing and counting	20	5x1.7	3	110nm	25 ps Jitter (8 fC MIP)	July 2019

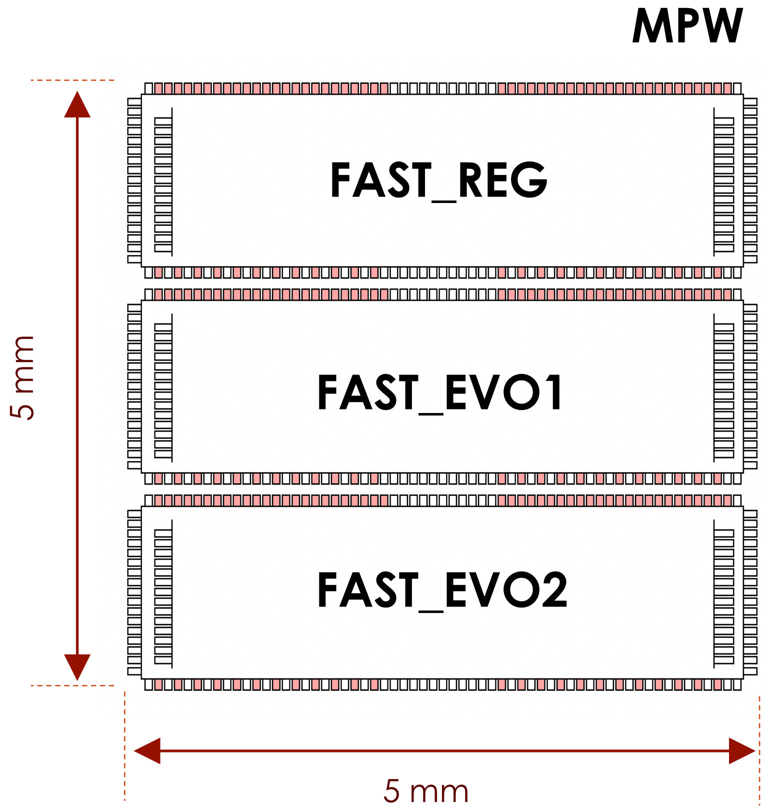
- **FoM**: picosecond time resolution and single ion detection at high rates (e.g. particle therapy applications)
- **Main challenges**: low power budget (<1.5 mW/Ch) and large sensor capacitance (6pF)

The FAST prototypes

Specifications

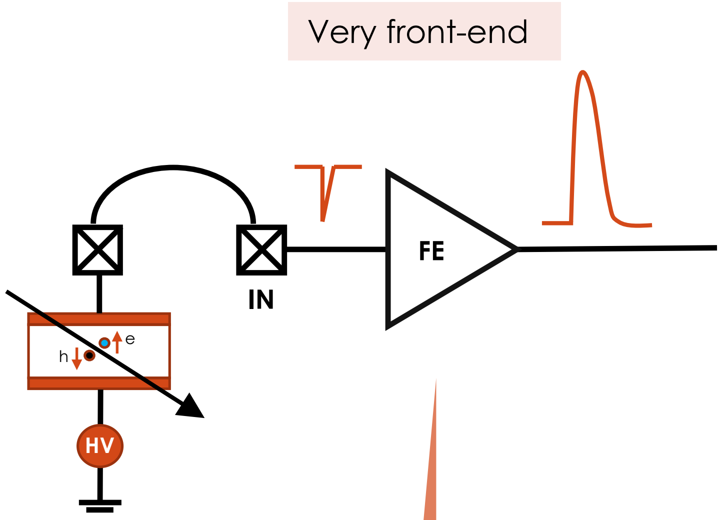
Channels number	20
FAST flavors	Regular, EVO1, EVO2
Operation Voltage	1.2 V
Size	1.6 × 5 mm^2
Sensor Cap	2-6 pF
$\overline{SNR}$	60
RMS Noise	~ 0.7 mV
Power consumption	< 2 mW/CH
Time Walk correction	ToA, Tot
MPV input signal	8fC
Nominal input dynamic range	1 fC - 60 fC





- A set of 3 ASICs has been produced in a **MPW** (07/2019)
- The flavours differ on the front-end amplifiers used
- The same IO-ring is used → the **same PCB**
- Each ASIC implements 20 channels

The channel

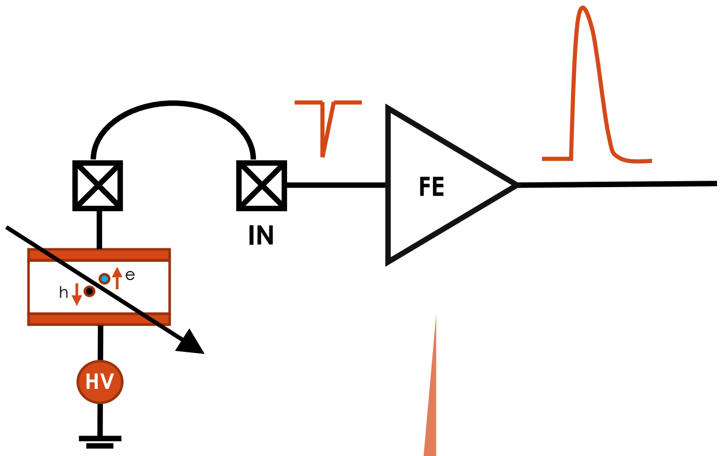


The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

The channel

Very front-end



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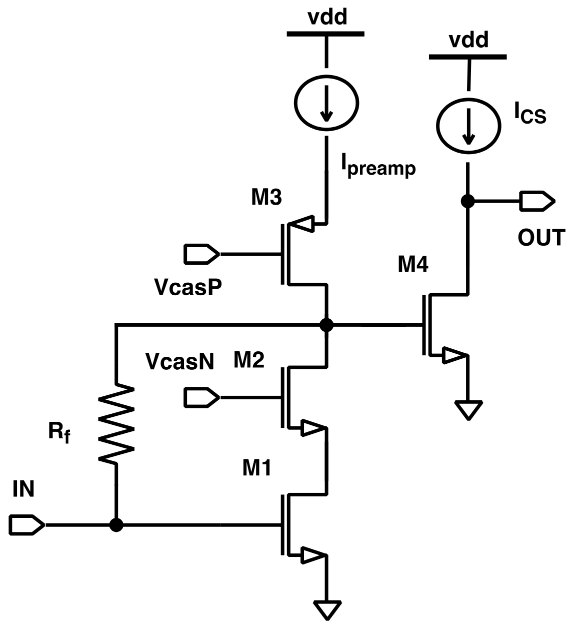
Trans-impedance - CS



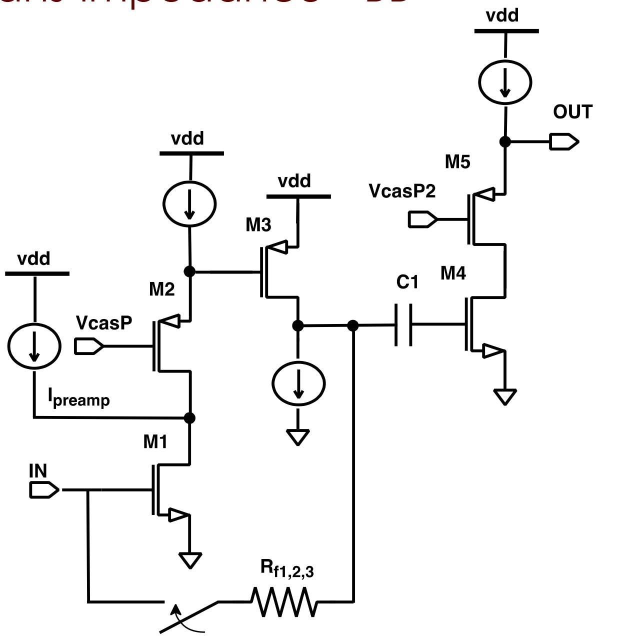
REGULAR

- Limited bandwidth to 100 MHz
- Gain: ~ 60 mV/fC
- Noise: ~310 e-
- Power consumption: ~1.2mW/CH
- SNR (MIP): ~ 160
- Max hit rate: 50 MHz

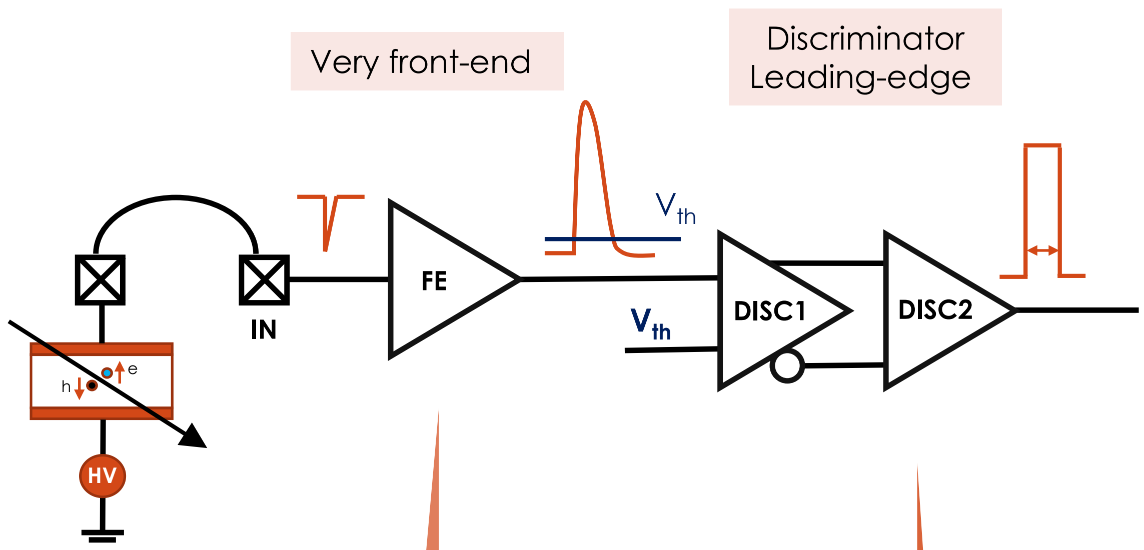
EVO

- Larger bandwidth: ~ 400 MHz
- Gain: ~ 31 mV/fC (8 regulations)
- Noise: ~640 e-
- Power consumption: ~1.2mW/CH
- SNR(MIP): ~75
- Max hit rate: 300 MHz
- AC coupling to reduce mismatch
- 2 topologies: standard CMOS & RF

Trans-impedance - BB



The channel



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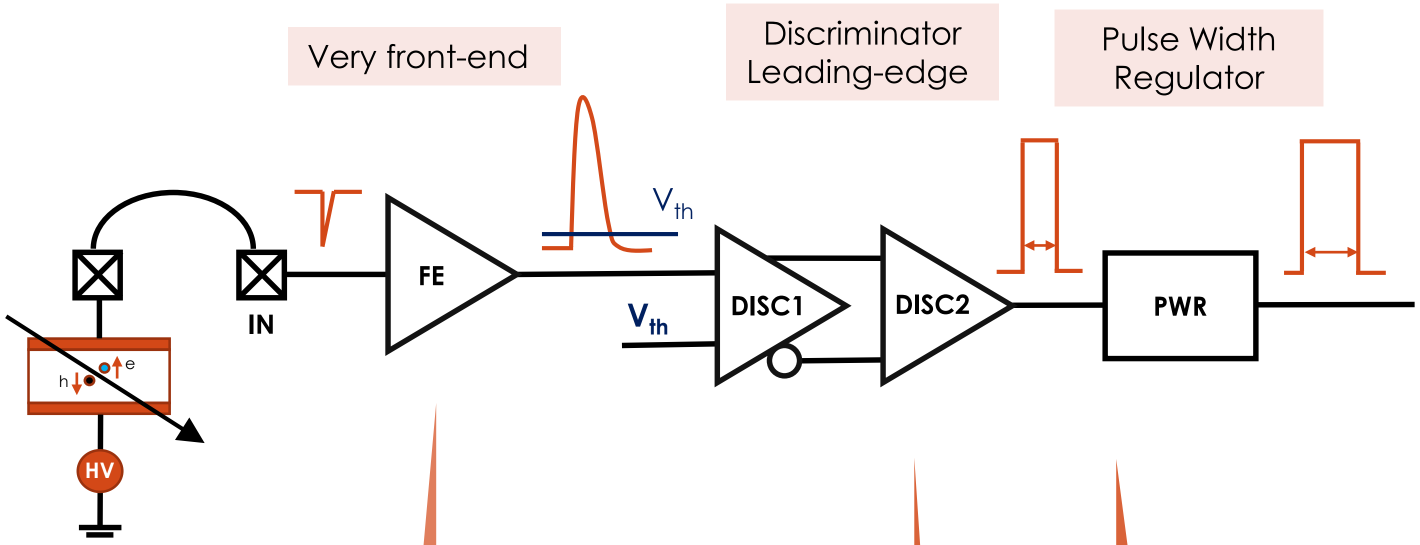
Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk**
  → offline corrected

The channel



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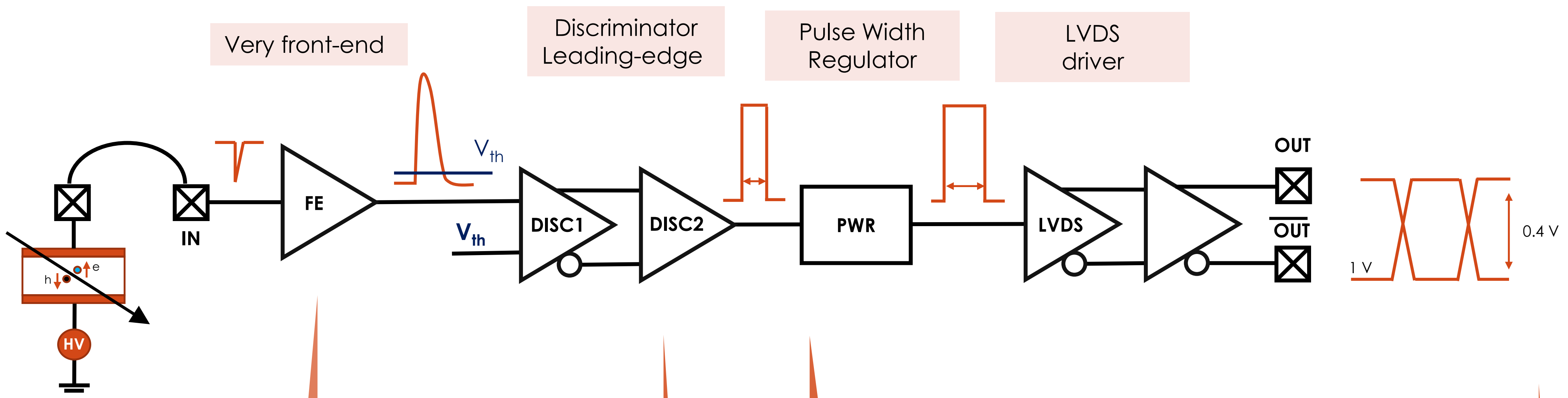
Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase a regulated Δt to this duration to make it compatible with **commercial TDCs**

The channel



The very front end

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  → offline corrected

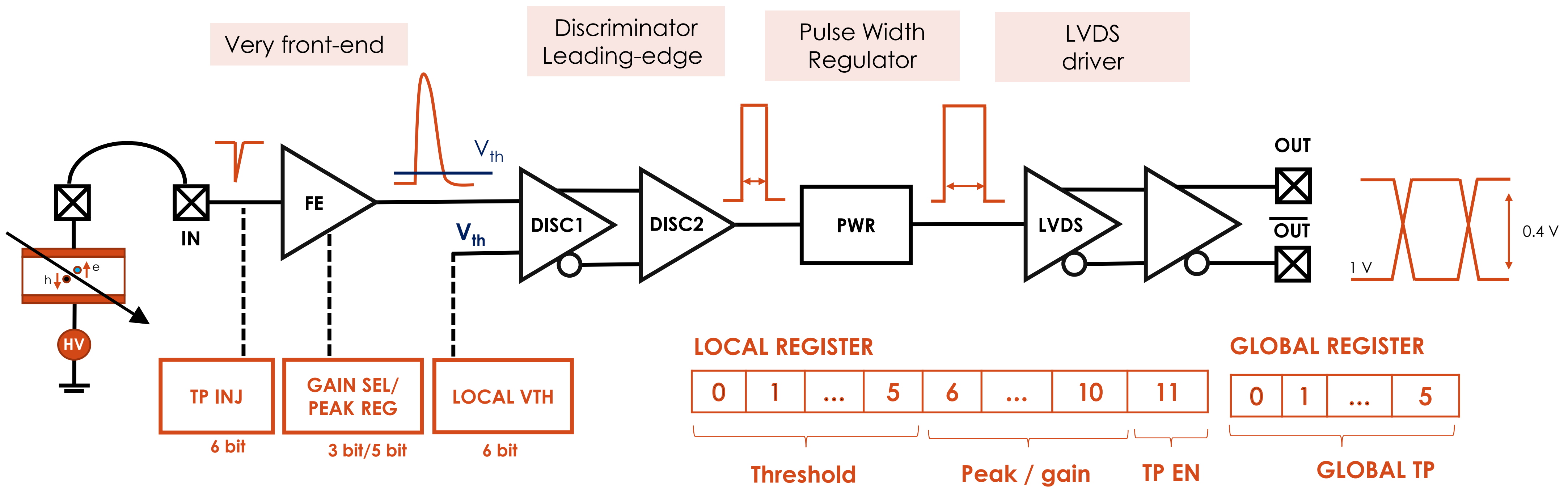
Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase a regulated Δt to this duration to make it compatible with **commercial TDCs**

LVDS drive

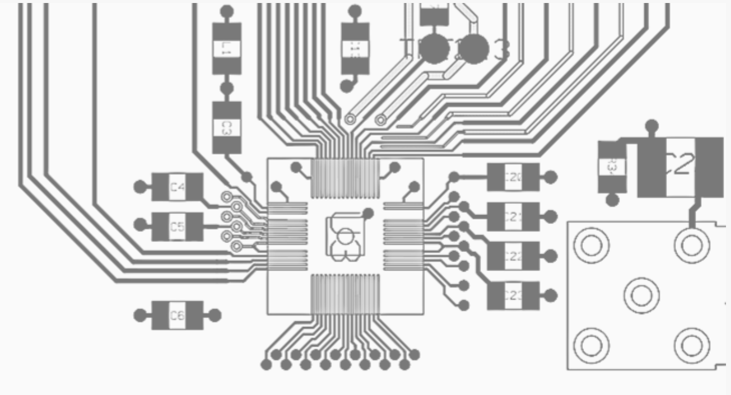
- It allows compatibility with **commercial TDCs and FPGAs**

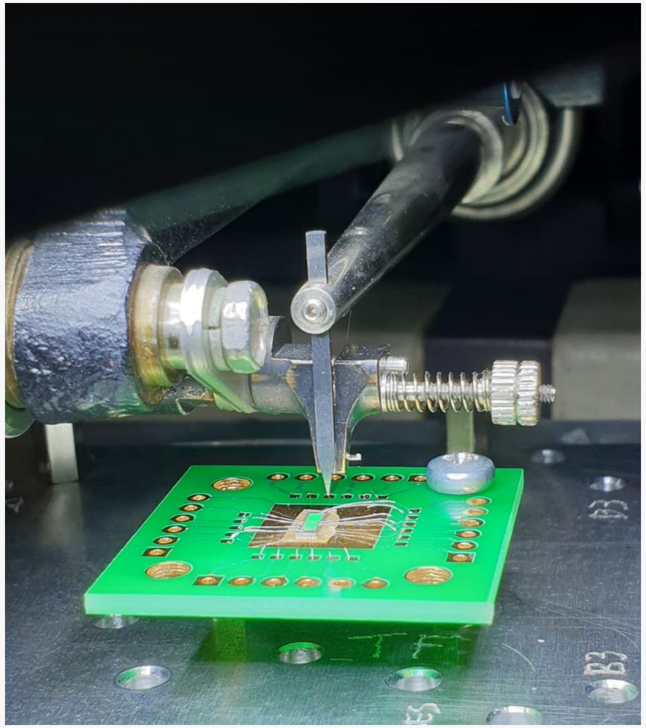
The channel



Ancillary circuitry

- **Test Pulse injection system:** a global register of 6 bits is used to inject charge from 0.3 fC to 18 fC
- **Selectable gain (EVO) or peaking time (REG):** 3 bits/5bits used to select 8 different gains in EVO or for the peaking time tuning in REG. The last regulation is meant to minimize noise
- **Local threshold regulation:** the threshold can be locally regulated up to 30 mV with 6 bits DAC
- **Pulse width regulation:** It allows to add a fixed Δt to the pulse duration.





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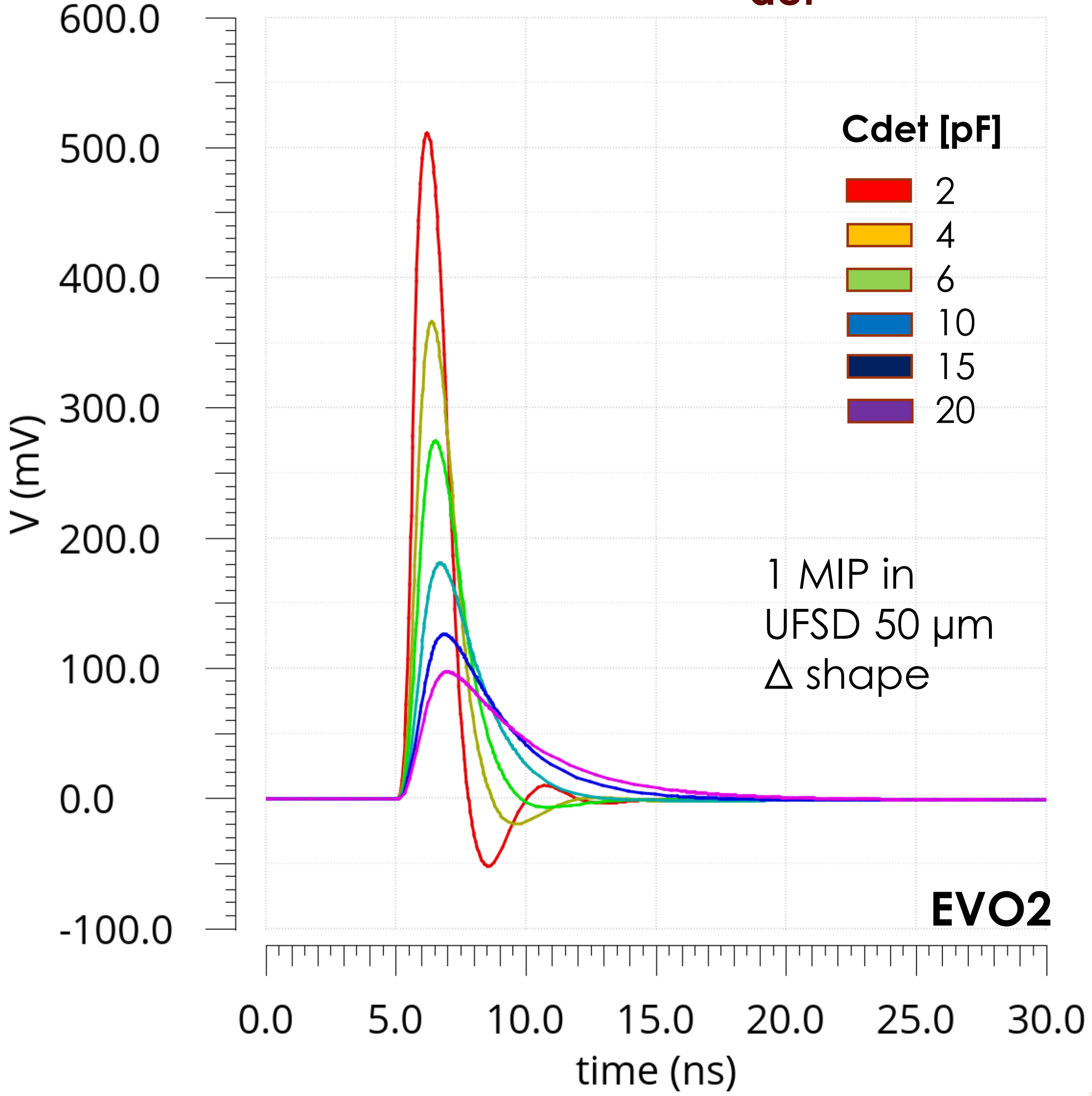
Simulations and silicon results

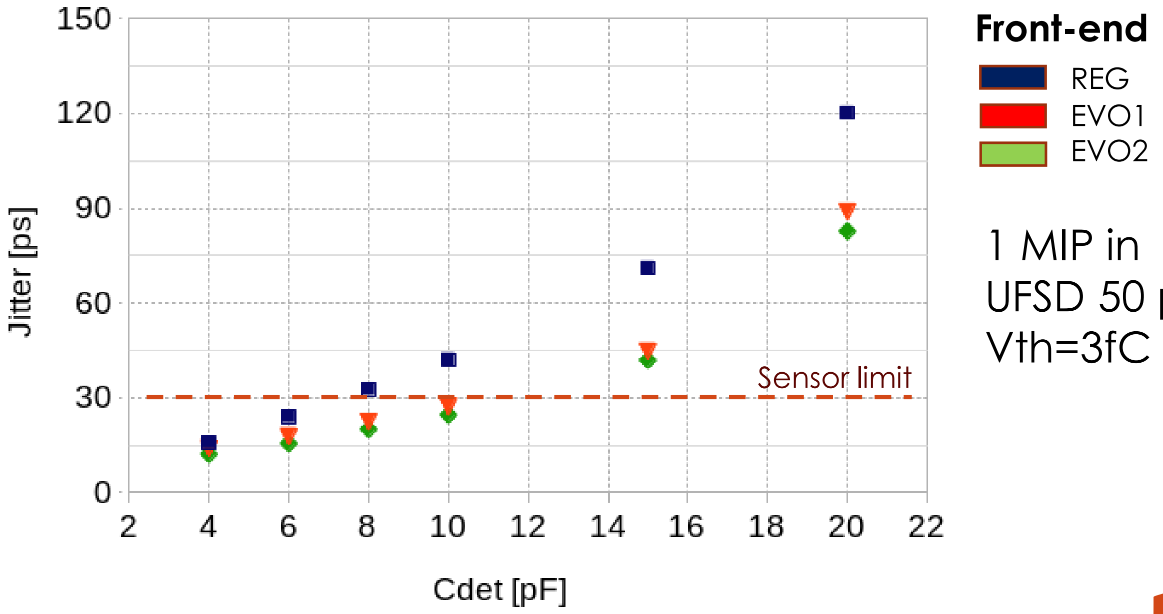
Front-end output and jitter

Vout vs C_{det}



- Analog output (amplitudes and duration) changes with the C_{det}
- Amplifiers are designed to reach 30 ps with 6 pF UFSD sensor
- Sensor cap ↓ Time resolution ↑ Max rate ↑

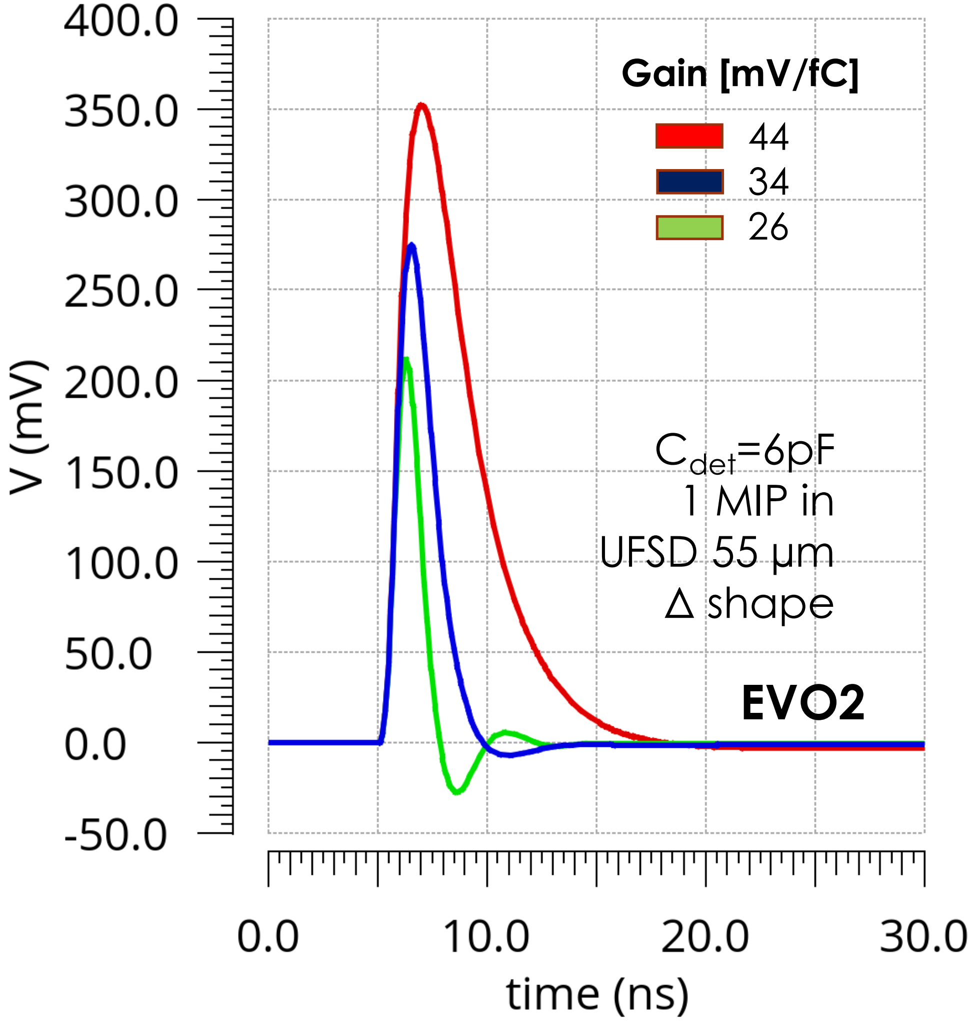
jitter vs C_{det}



1 MIP in
UFSD 50 µm
Vth=3fC

FE output (2)

Vout vs gain



jitter and rate vs gain

Gain [mV/fC]	Amplitude [mV]	Jitter [ps]	Noise [e-]	Max rate [MHz]
26	211	19.8	779	300
34	274	18.5	610	227
44	352	19.8	493	128

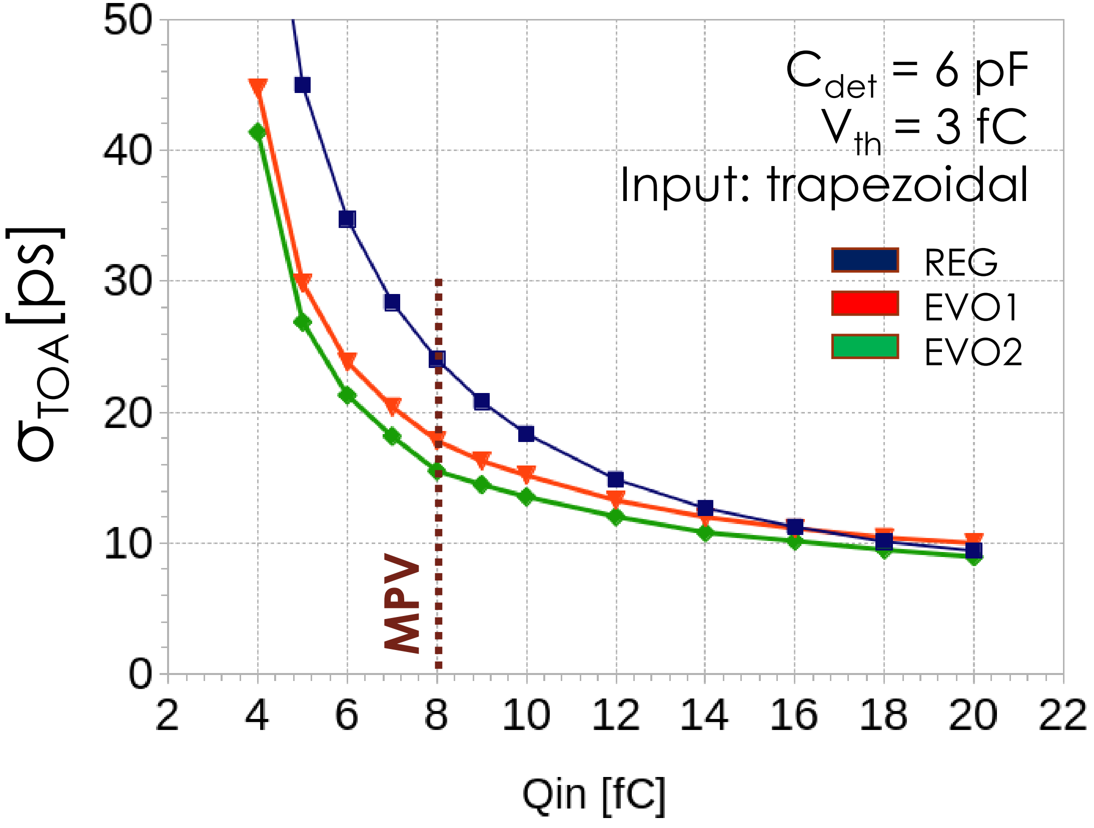
- Gain does not affect significantly the timing performances
- Generally noise decreases with gain
- Gain ↓ → max rate ↑

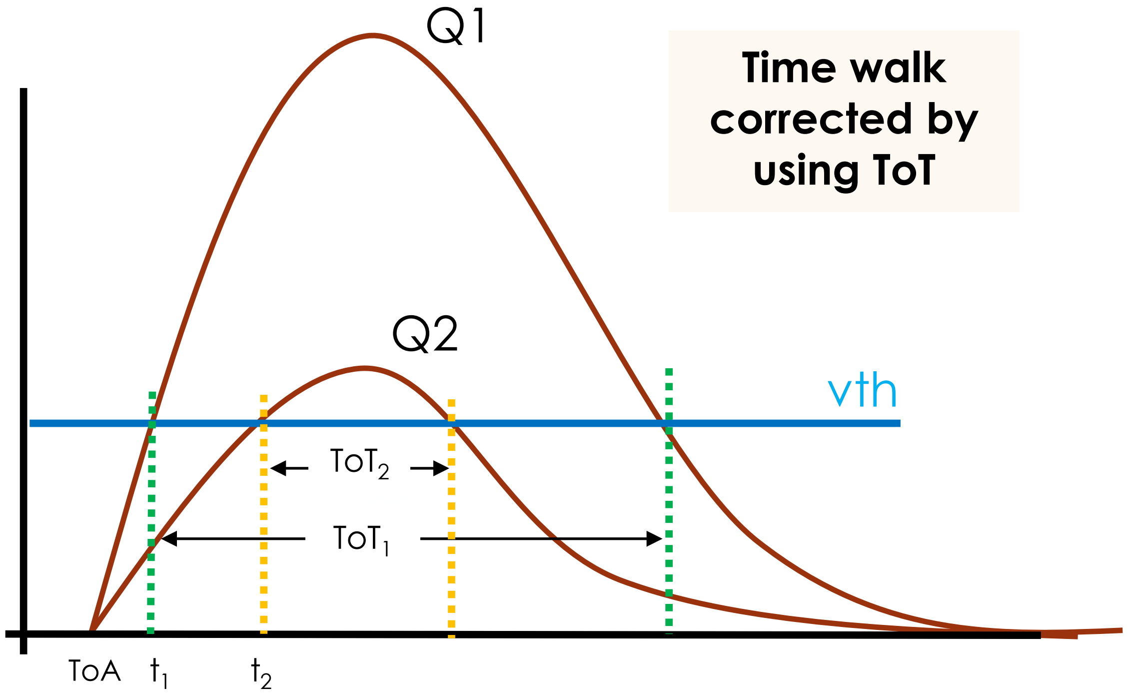
Front-end outputs comparison

Dependency from input charge

- 1 proton MIP release Q in silicon according to **the Landau distribution**
- LE-discriminator is used, ToA and then also jitter depend on Q_{in} → a corretion is needed

jitter vs Q_{in}





Time walk corrected by using ToT

ToT should be measured with good accuracy to make a precise correction → **Short tails are preferred**

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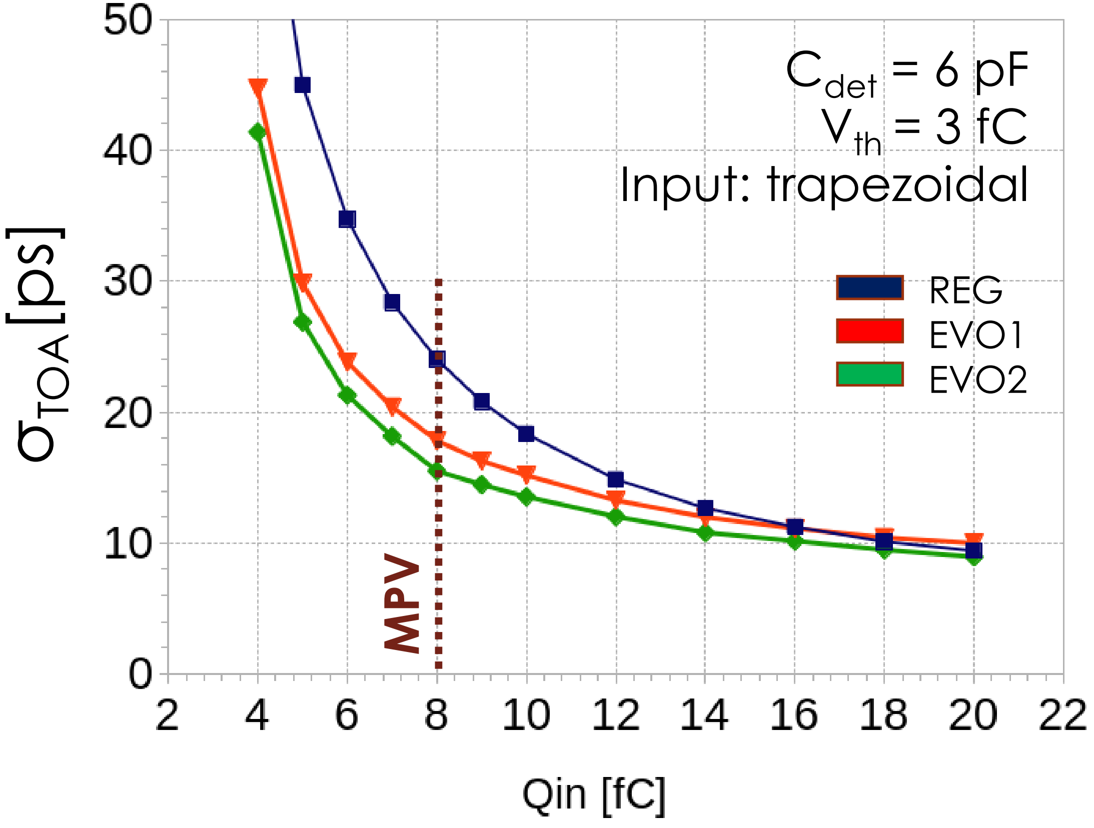
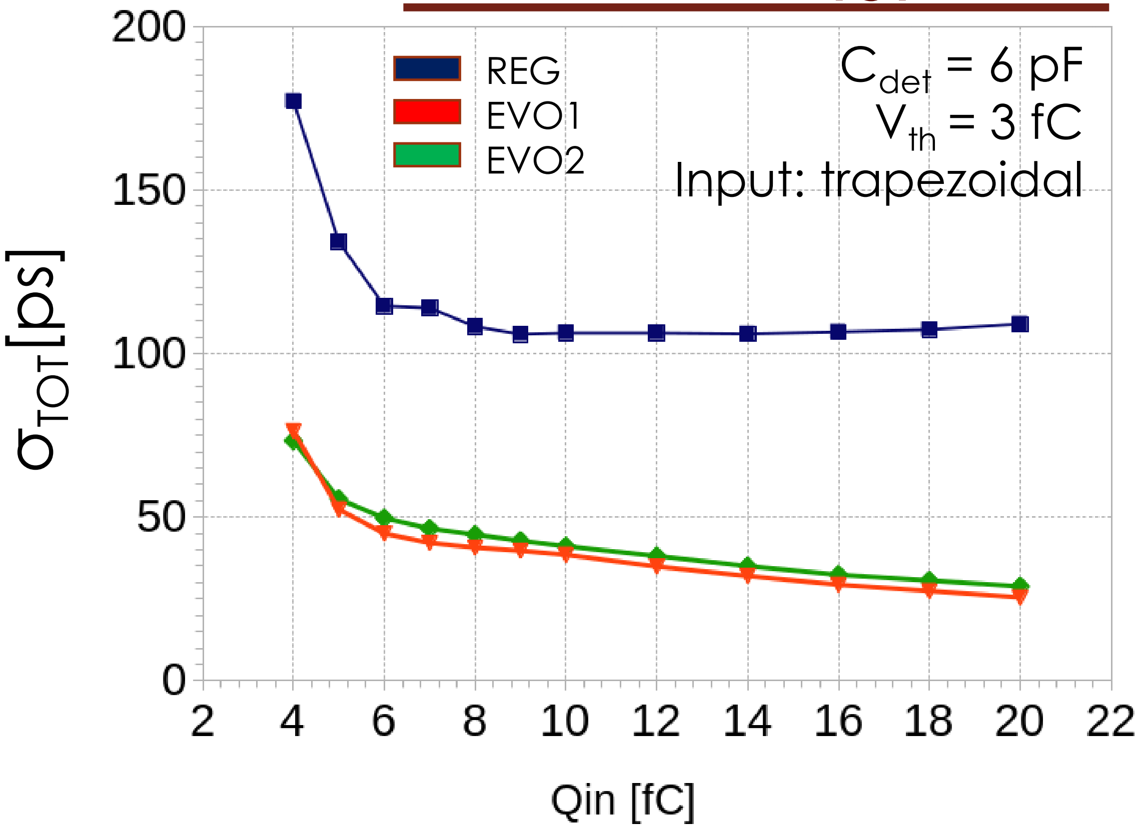
jitter vs Q_{in}



σ_{TOT} vs Q_{in}



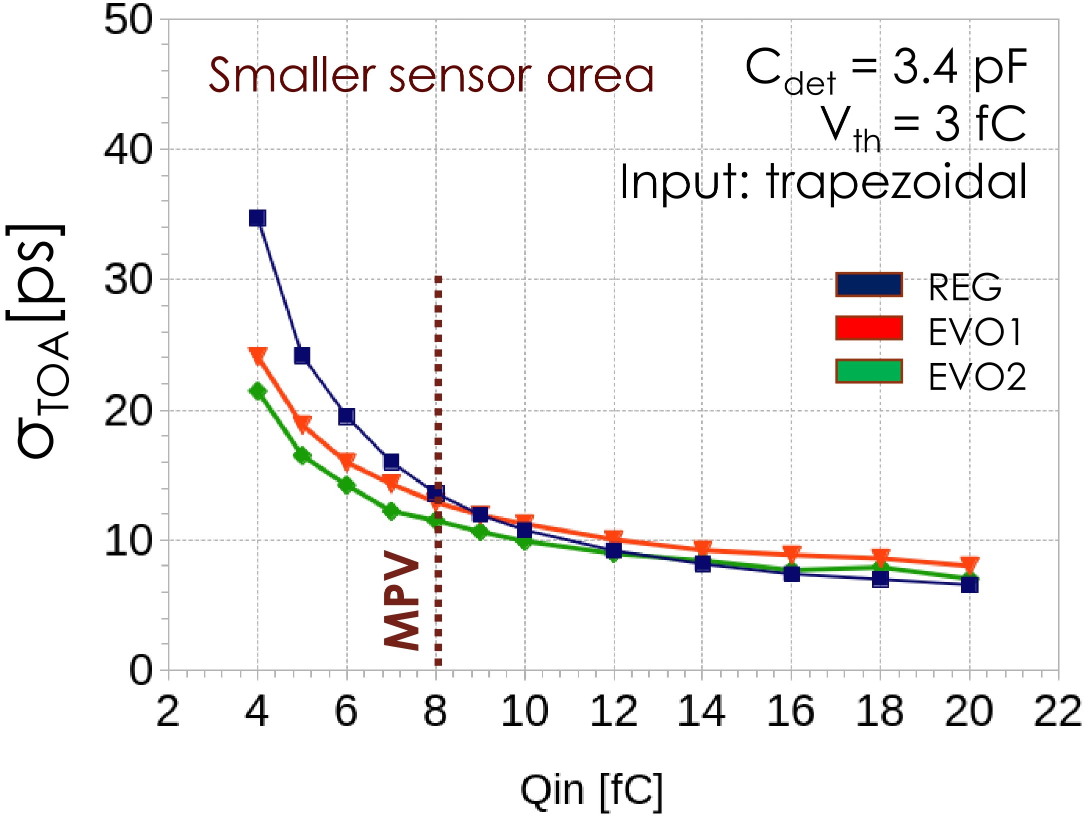
Front-end outputs comparison

Dependency from input charge

Smaller is the sensor, smaller is the jitter

- 1 proton MIP release Q in silicon according to **the Landau distribution**
- LE-discriminator is used, ToA and then also jitter depend on Q_{in} → a corretion is needed

jitter vs Q_{in}



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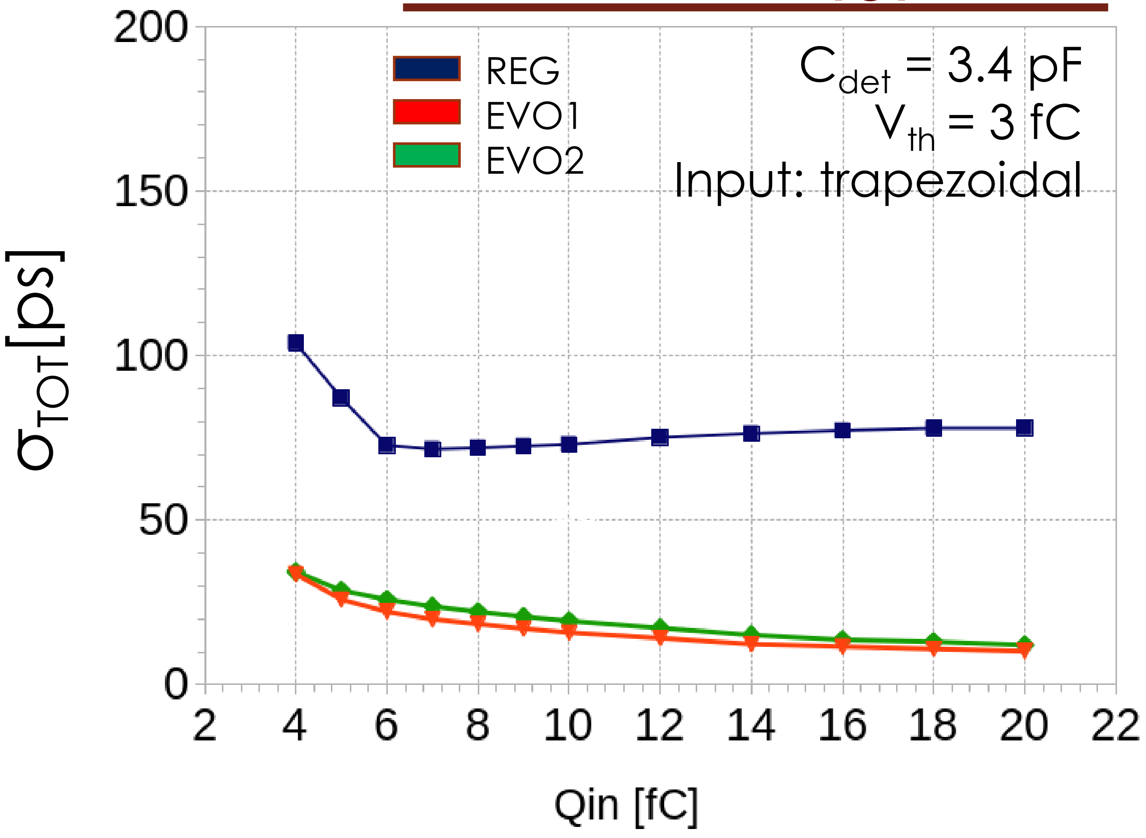


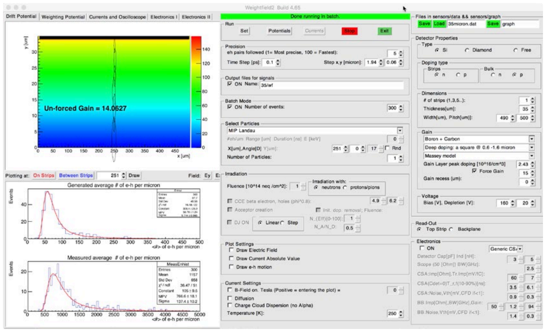
Time resolution simulations

System level simulation

$$\sigma_t^2 = \sigma_{LANDAU\ NOISE}^2 + \sigma_{DISTORTION}^2 + \sigma_{JITTER}^2 + \cancel{\sigma_{TDC}^2} + \sigma_{TIME\ WALK}^2$$

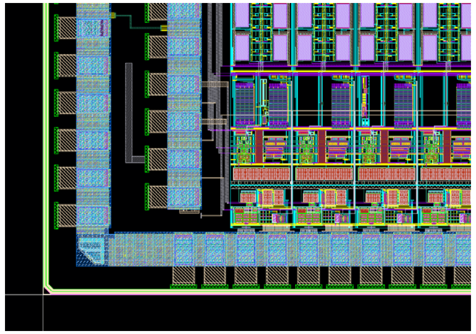
- **Simulations include effects on silicon** like Landau noise and signal distorsion (Weightfield2)
- Weightfield2 in combination with EDA tools to simulate the entire system

Weightfield



Skill language →

EDA tools



What is included in this simulations?

- Landau distributed input signal
- Transient noise simulations
- R-C-CC parasitics included
- 2 different tools used for the parasitic extraction

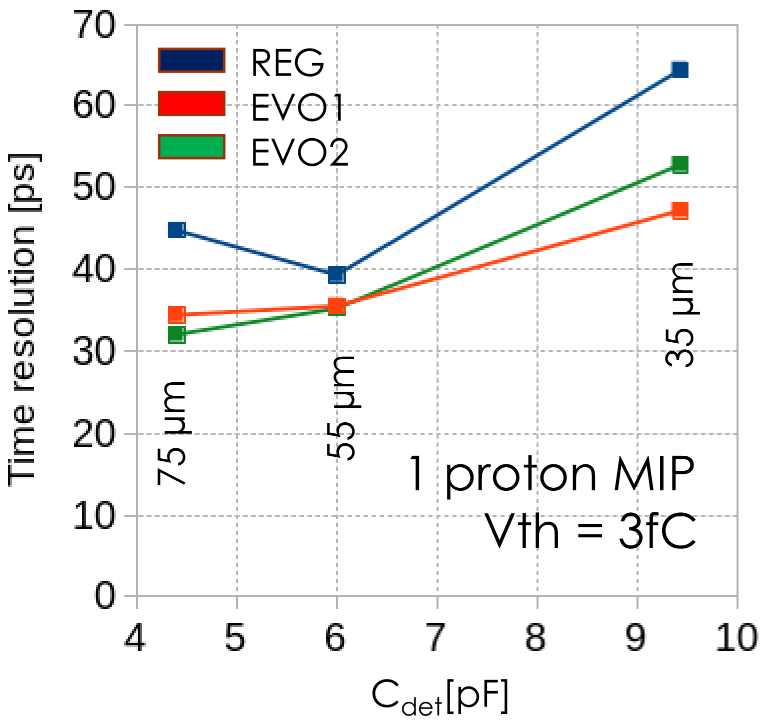
- Time walk is corrected offline
- The TDC contributes with a systematic effect

Time resolution vs sensor area and thickness

- Study done playing with three important parameters:
  - → **Sensor thickness**: 35 µm, 55 µm, 75 µm
  - → **Sensor geometry**: 1x1 mm^2, 1.3x1.3 mm^2 and 1x3 mm^2
  - → **Front-end**: REGULAR, EVO1 and EVO2

→ 3 values of C_{det}

Area = 1x3 mm^2



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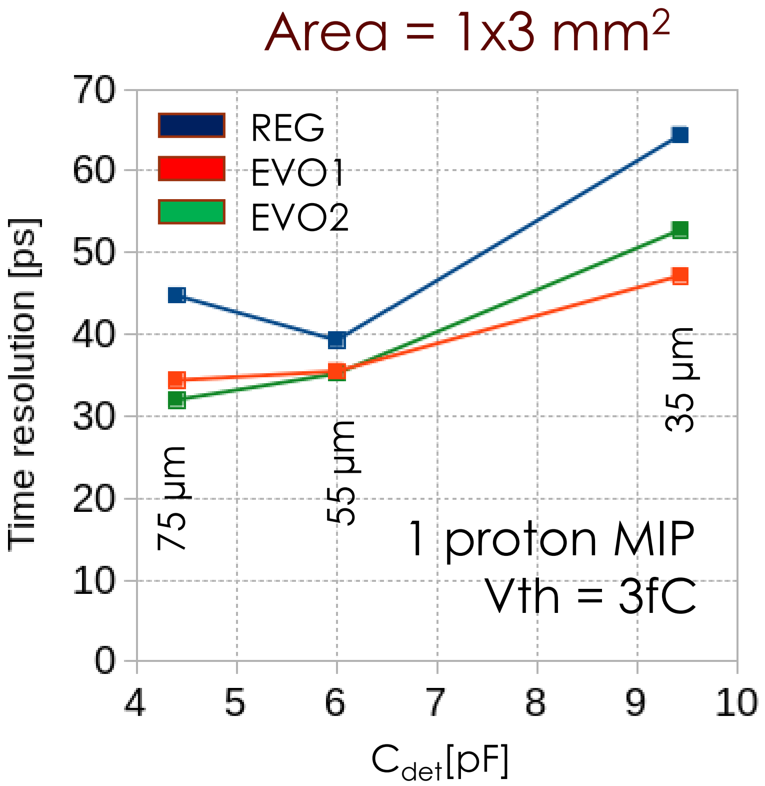
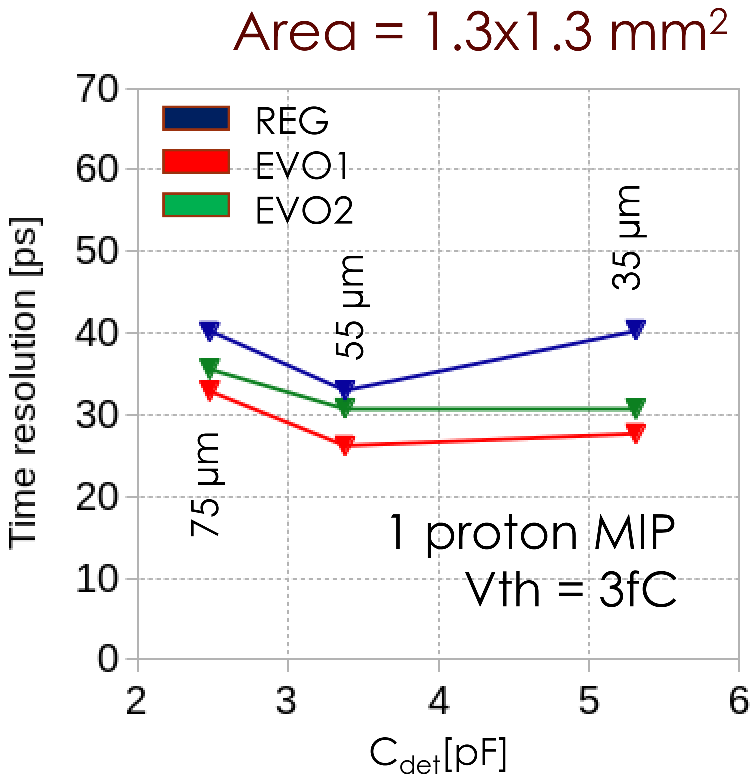
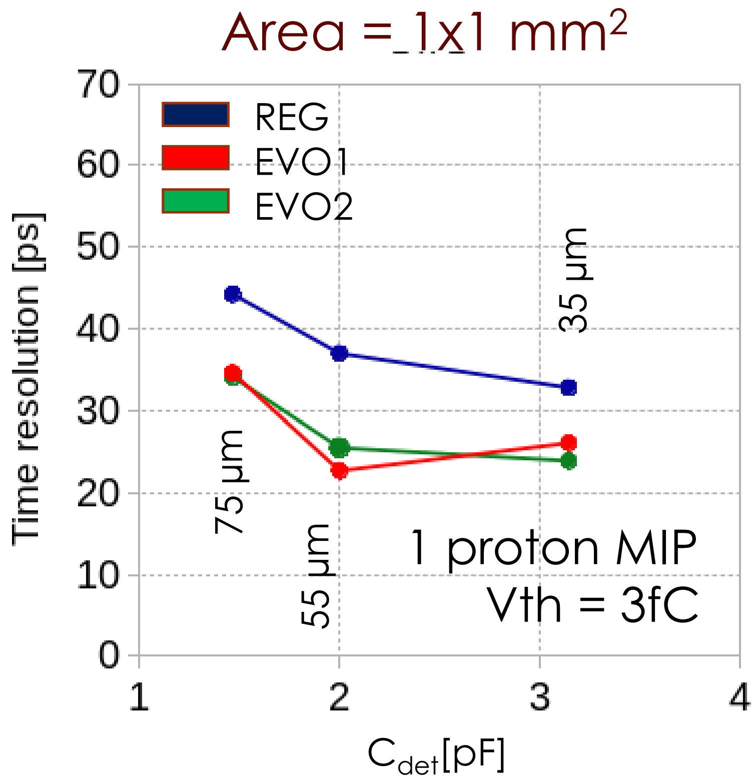
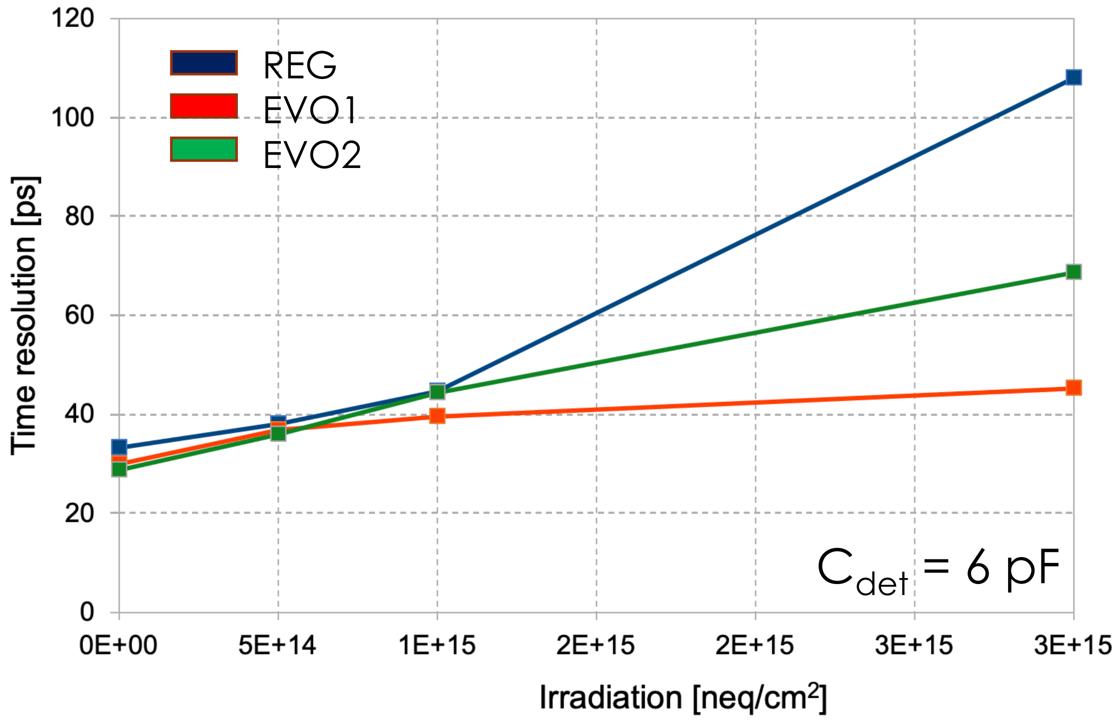






Time resolution with irradiated sensor



FBK 55 μm (Boron + Carbon)

- The effect of radiation in silicon affects the collected charge. This effect is taken into account
- **Time resolution for non-irradiated sensors** is around **30 ps**
- EVOs measure always time more precicely than REG
- FAST + FBK allows to maintain a time resolution below 50 ps up to $1x10^{15}$ n_{eq}/cm^2
- Leakage current is not included in this simulations

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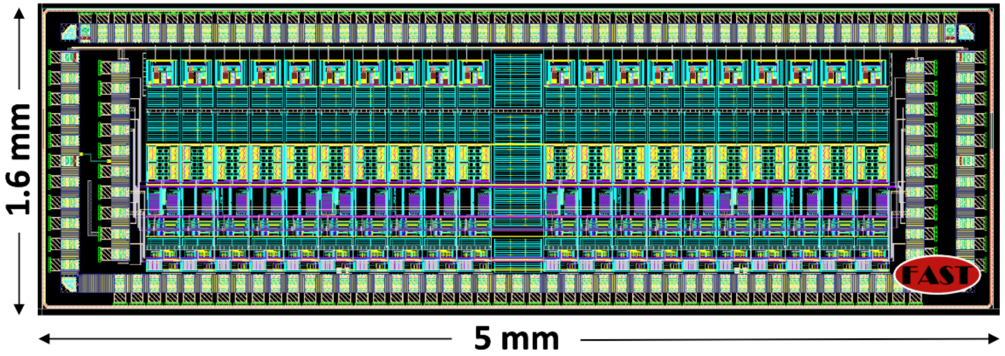
First silicon results

Preliminary results

Custom board for FAST



- Number of PADs: 140 (46 for the POWER)
- **Particular attention during the design** to reduce parasitics:
  - → wire bonding lenght <0.5 cm
  - → wire diameter of 25 μm
  - → 2 bondings/PAD can be done

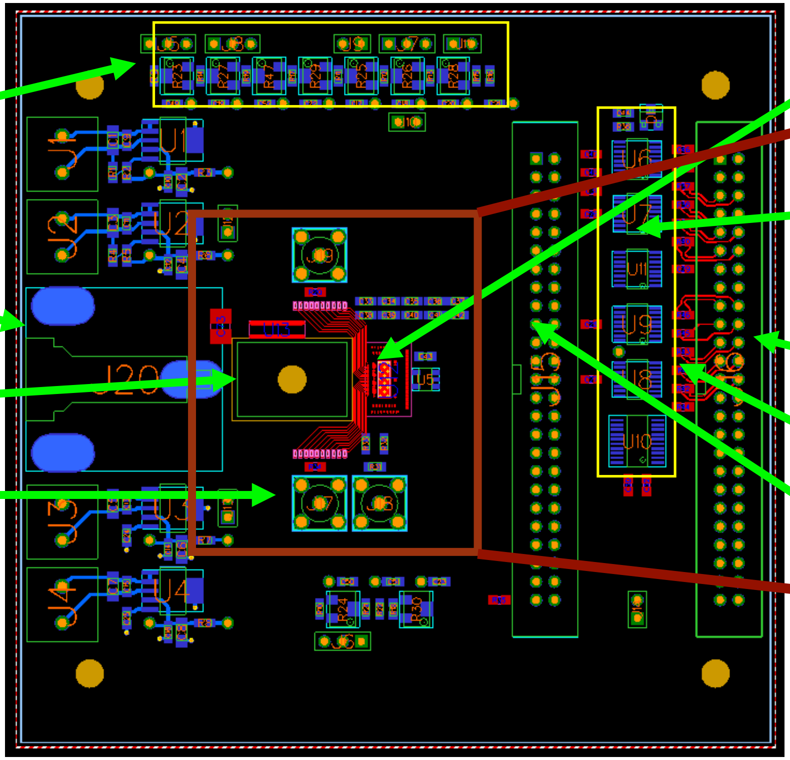
Trimmers

Voltage regulators (3.3, 1.2, 2.5)

SHV connector

HV area

SMA for TP



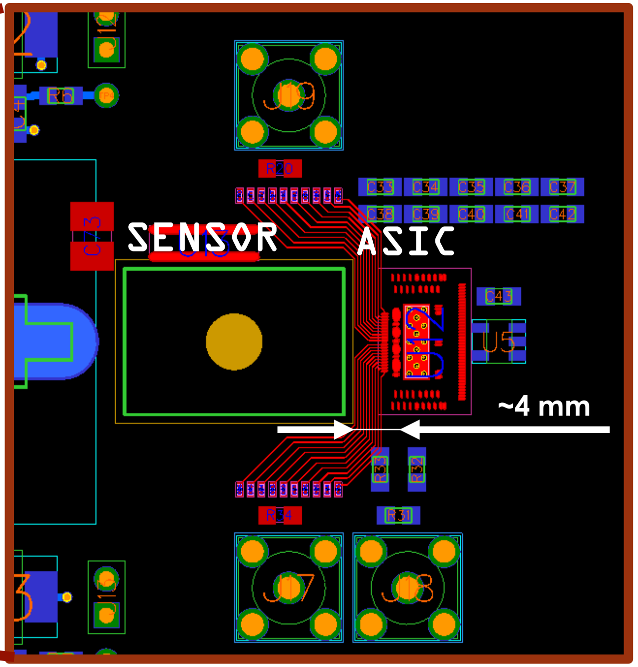
Chip Footprint

LVDS outputs

Digital inputs (FPGA)

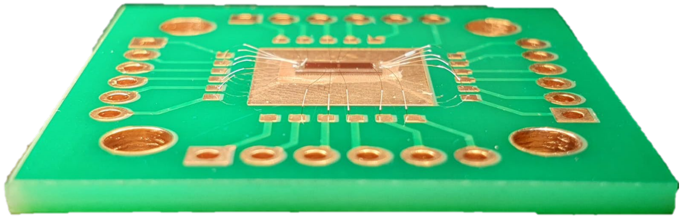
Converters (diff to SE)

Temperature sensor



The custom board will be delivered in few weeks

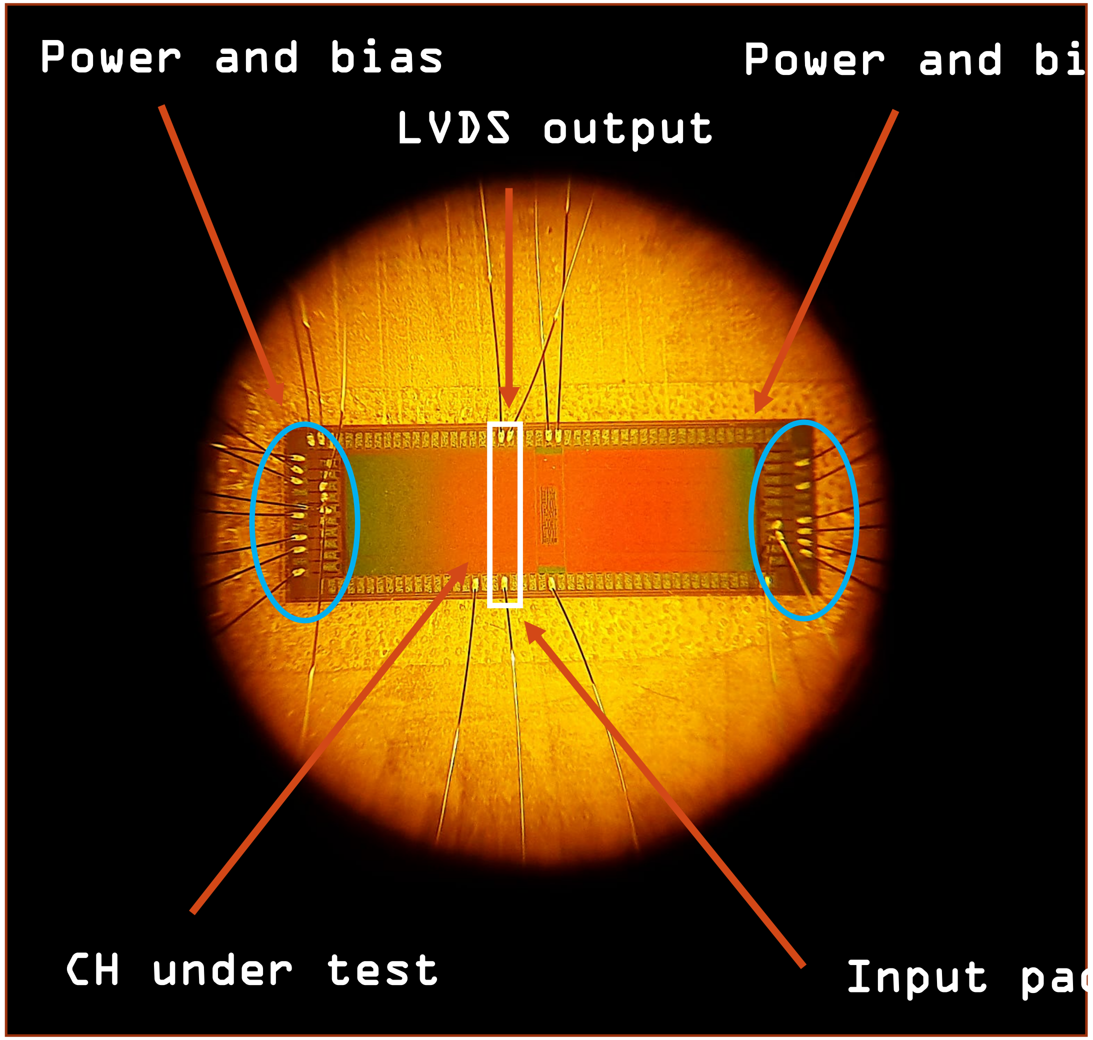
First basic setup with FAST



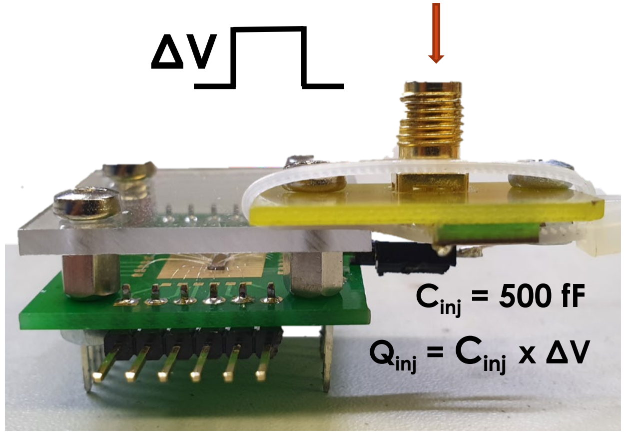
- FAST prototypes delivered on October 2019
- A general purpose board has been used for the first basic tests
- Connection for basic tests:
  - Power lines: 1.2 V (ANA and DIG) and 2.5 V (IO)
  - Biases: I & V
  - IN/OUT of a channel

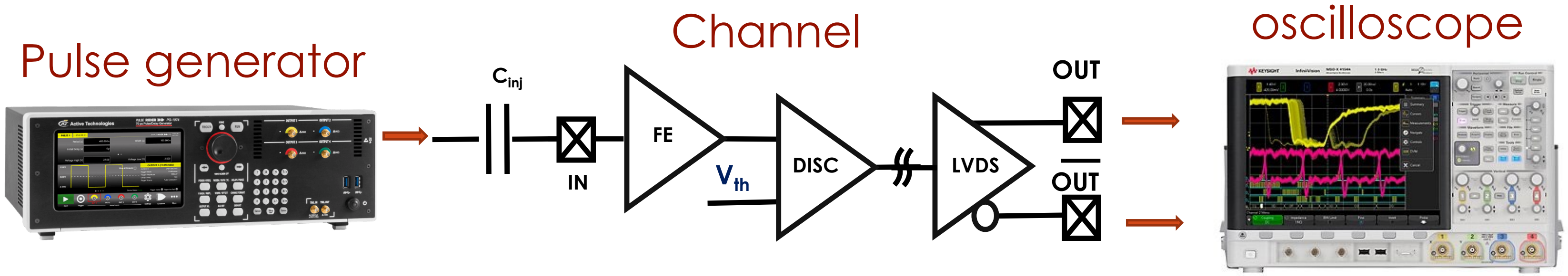
Power consumption

Domain	Expected	Measured
Anag & Dig 1.2V	62 mA	60 mA
IO 2.5 V	18 mA	20 mA



Test with charge injection





- A small carrier board is used to mount C_{inj} and a SMA connector
- Vth is provided by one pin on the PCB

Voltage response to a injected pulse

- First threshold scan shows a **peak-to-peak noise of 10 mV** in good agreement with simulations
- The first test allows to see that the entire chain is propertly working
- The system has a lot of **antennas** (to be optimized), so interference should be reduced
- The setup is enough to test some block of FAST but not to measure time resolution

Conclusions and future steps

6/6

- FAST prototypes have been designed in CMOS 110 nm technology exploring **three front-end amplifiers** and they have been received on **October 2019**
- Several **simulations** of the readout electronics coupled with the sensor have been carried out **including the most important contribution in time resolution**. Results are very promising and fit the **30 ps time resolution also with 6 pF sensor**
- A **custom PCB has been designed** taking into account important design choices for high precision time measurements. It will be available in few weeks
- A very basic setup has been used to power on the ASICs and this has been used to measure **power consumption** as expected by simulation and **noise.** The setup has been used to test all the bocks of one channel by means the injection of a signal
- For the future:

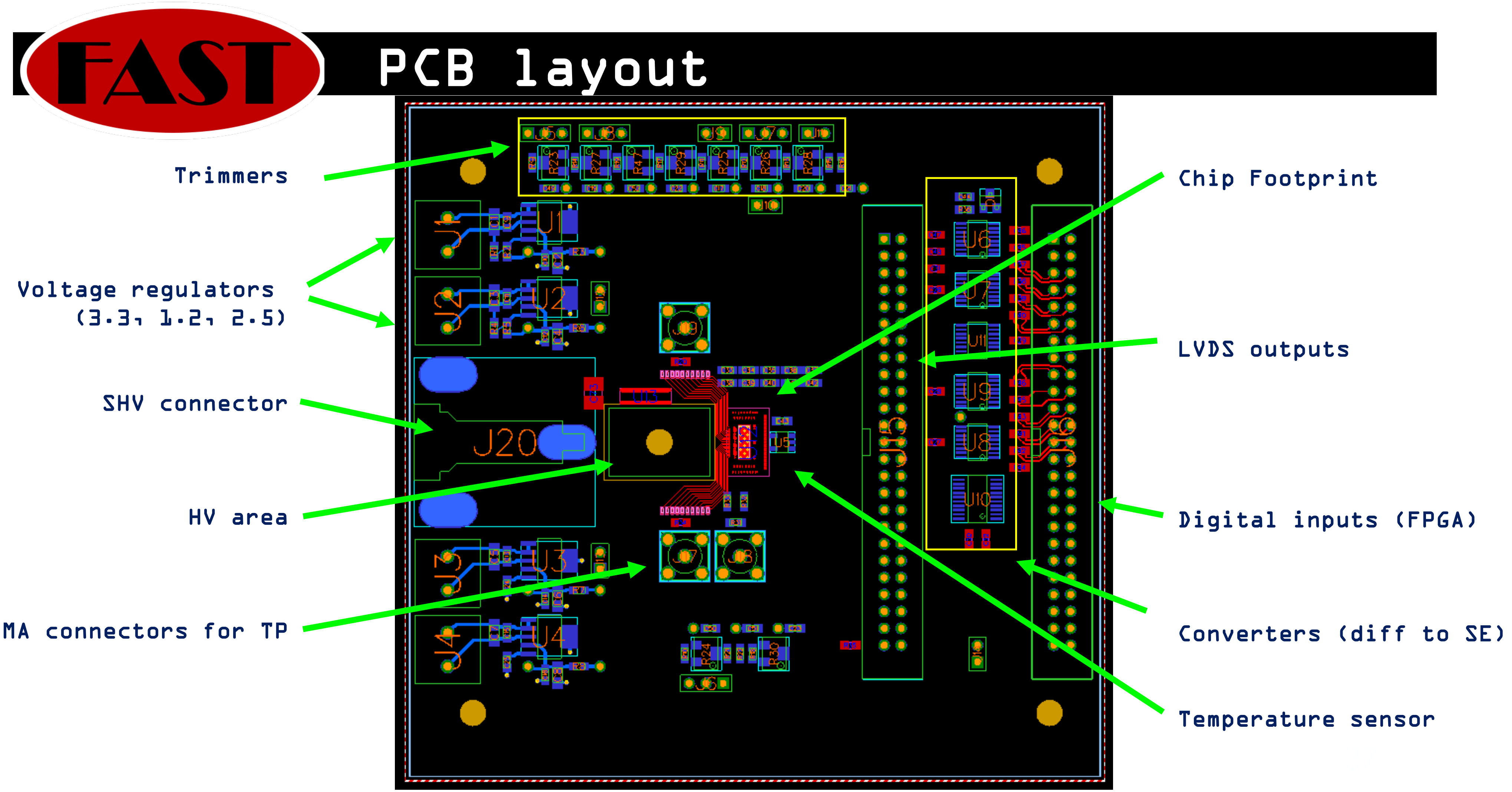
  - **Improve the system** to test other blocks like the digital logic
  - **DAQ** is based in LabView and an Xilinx FPGA
  - **FAST characterizaion** with UFSD sensors by using laser sources, active sources
  - A test beam is planned on 2020

We kindly acknowledge the UFSD group for the support and the following funding agency: Horizon 2020 Grant URC 669529 Ministero degli Affari Esteri, Italy, MAE

Thank you for your attention

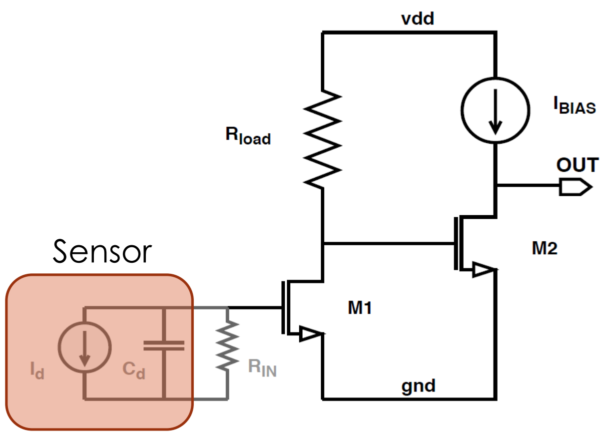
Backup slides

Custom PCB for FAST

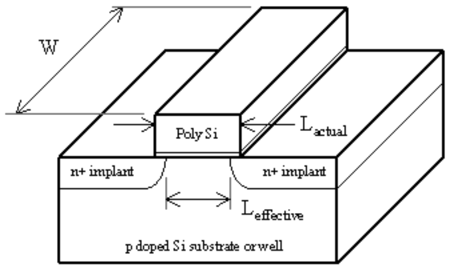


The technology choice in timing applications

Broad-band amplifier

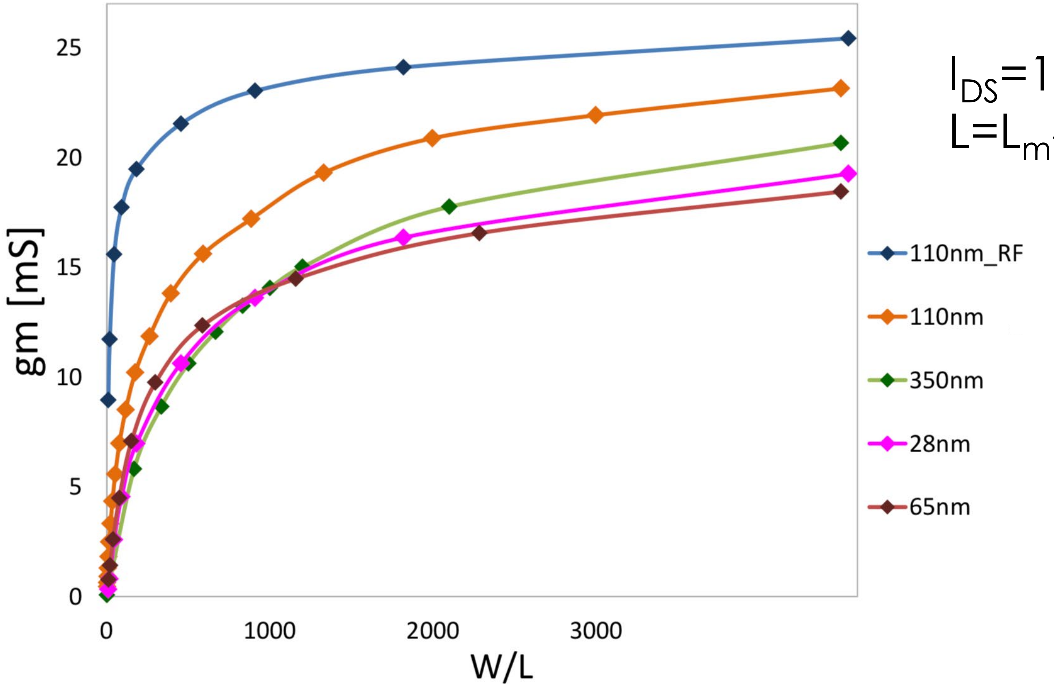


$$\sigma^J_t = \frac{C_d}{Q_{in}} \sqrt{\frac{2KT}{g_{m1}} t_d}$$



- Jitter depends on the **trasconductance g_m**
- g_m in general is not a technological parameter, but it can be consider a good parameter to compare different tecnologies fixing some parameters like power consumption
- The comparison shows that fixing the power consumption to 1 mW, the gm is higher in 110 nm CMOS technology

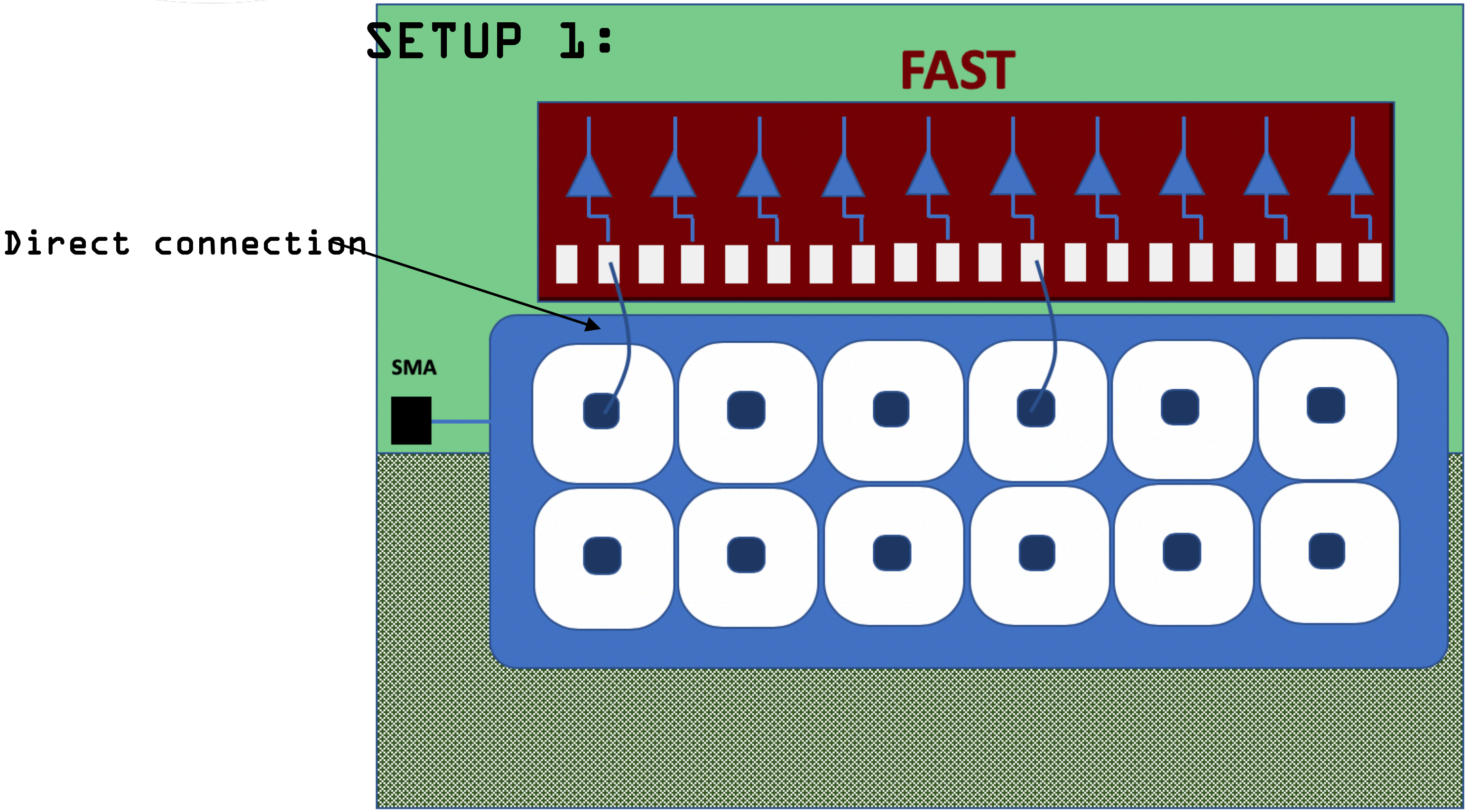
Comparison between CMOS tecnologies



I_{DS}=1 mA
L=L_{min}

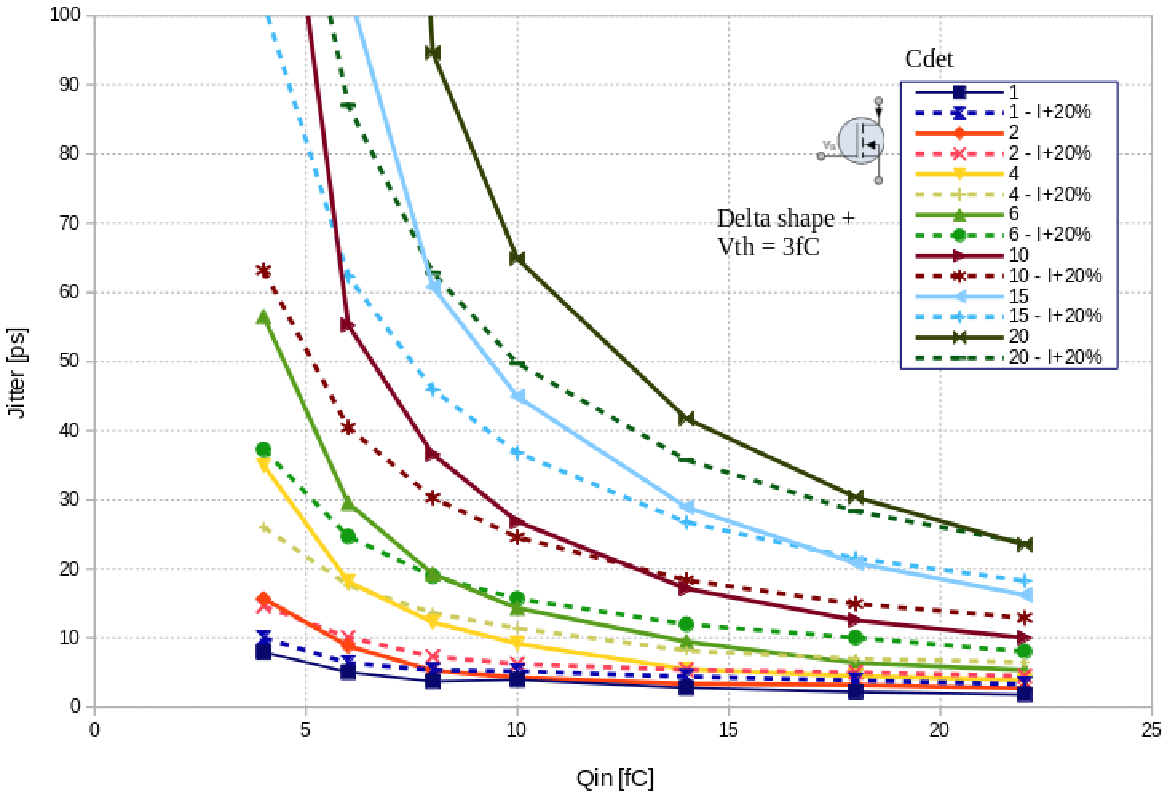
Scheme for wire bonding

PCB for FAST: INPUT PADs

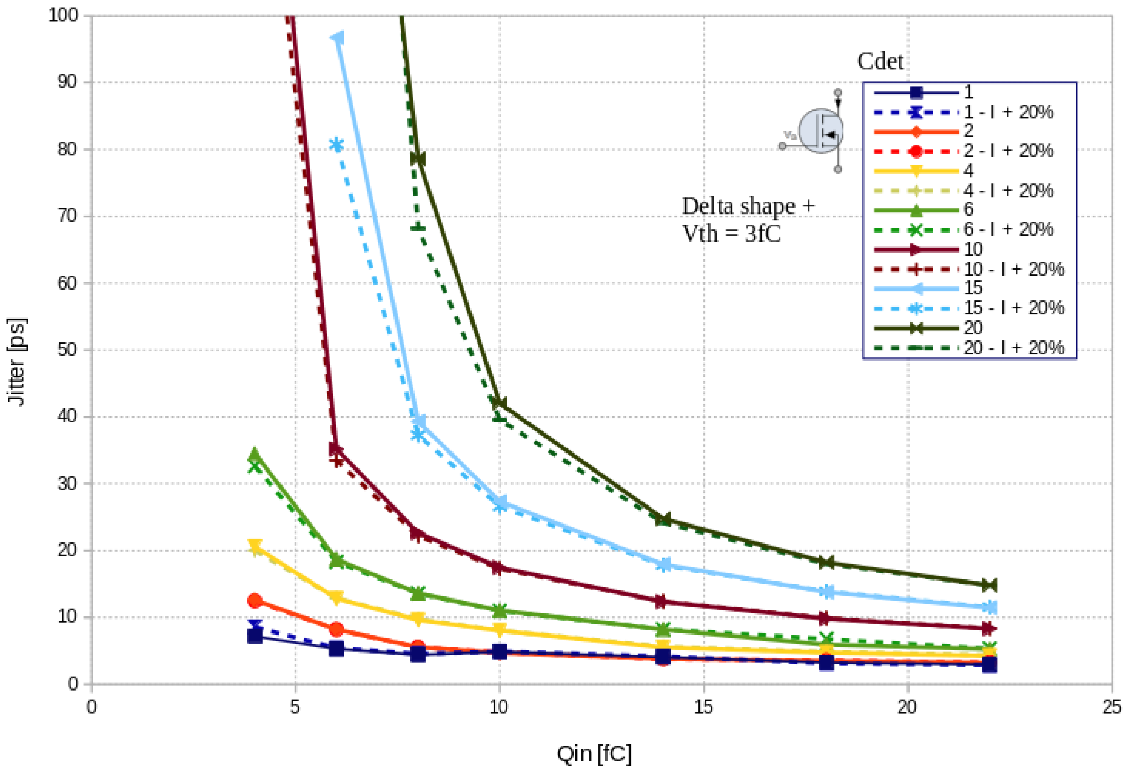


Jitter vs input charge in case of extra power

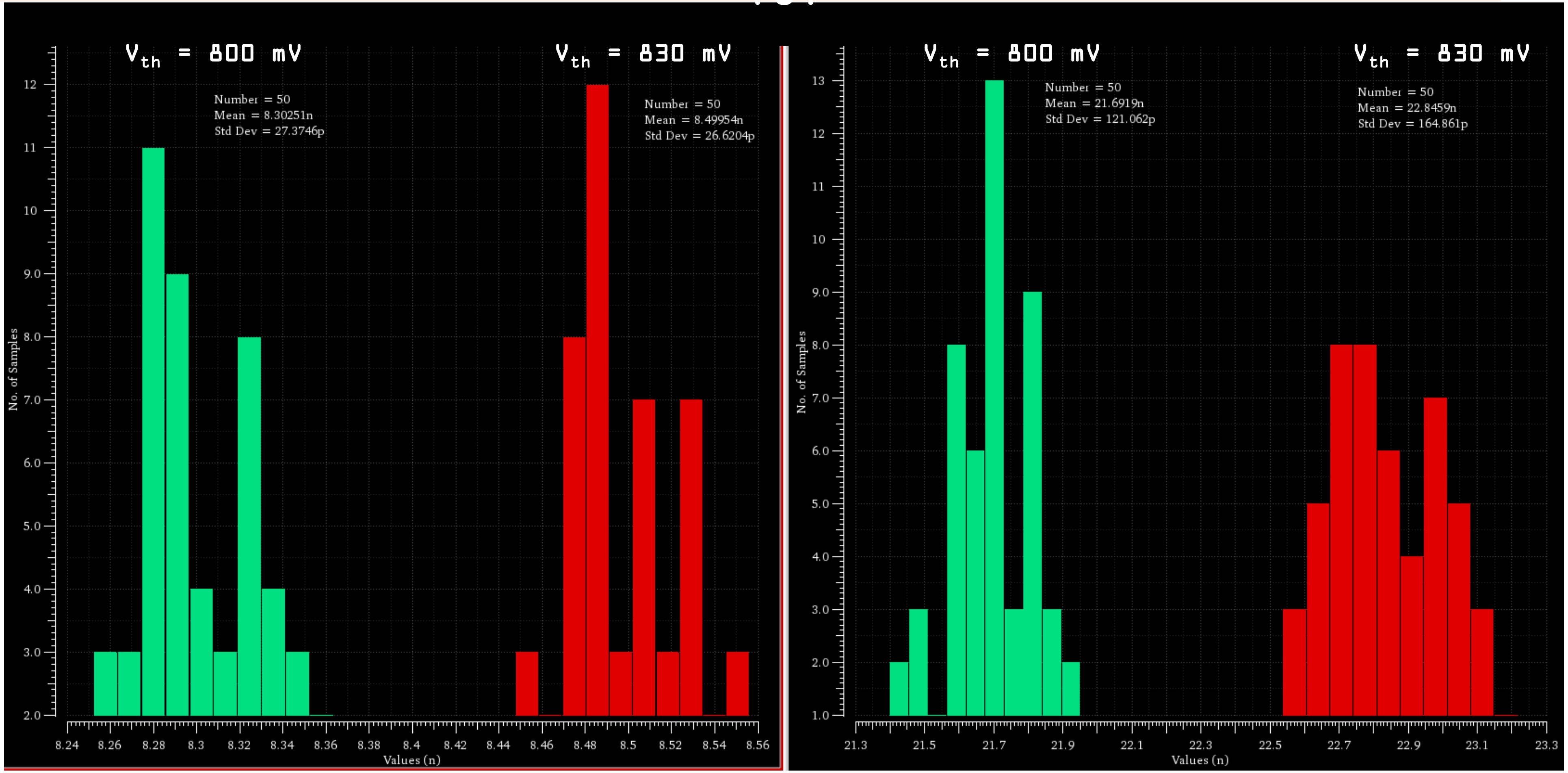
FAST REG



FAST EVO1

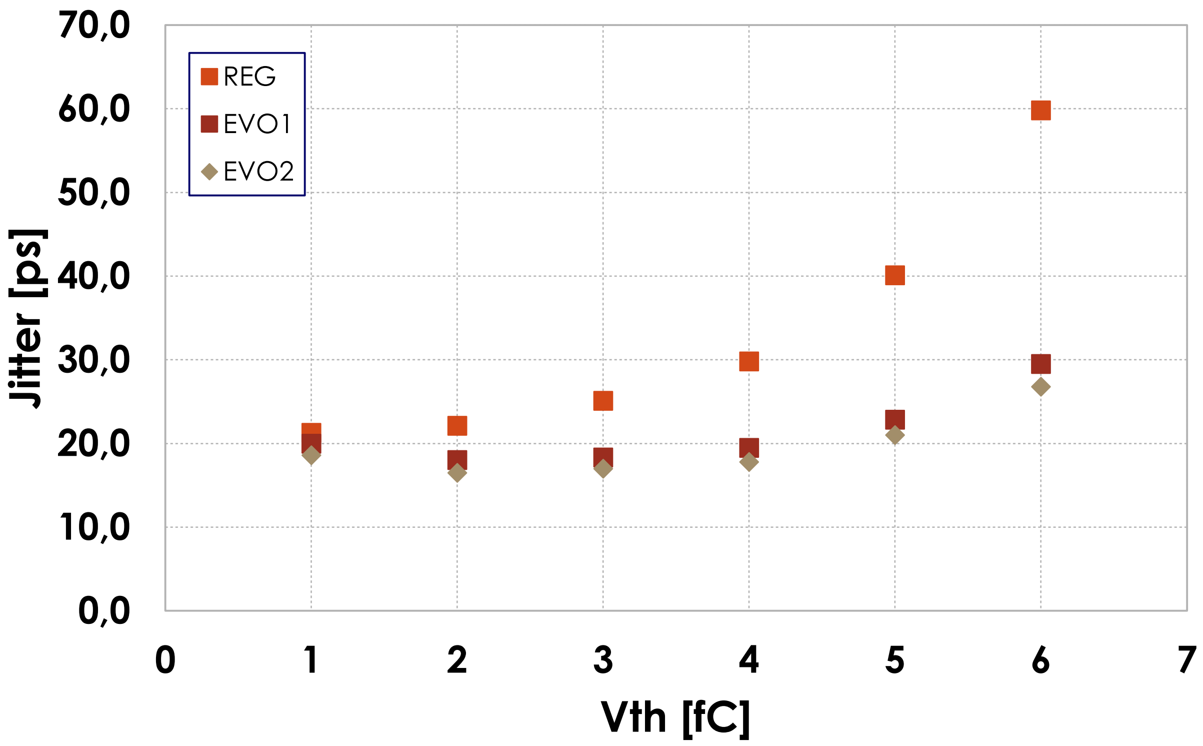


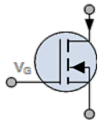
ToA



- The time resolution in this condition is 26 - 27 ps. The optimum for the
- More than 50 runs are required to estimate the resolution with good accu
- Wire bonding is modeled by means of an inductance of 2 nH (worse case)

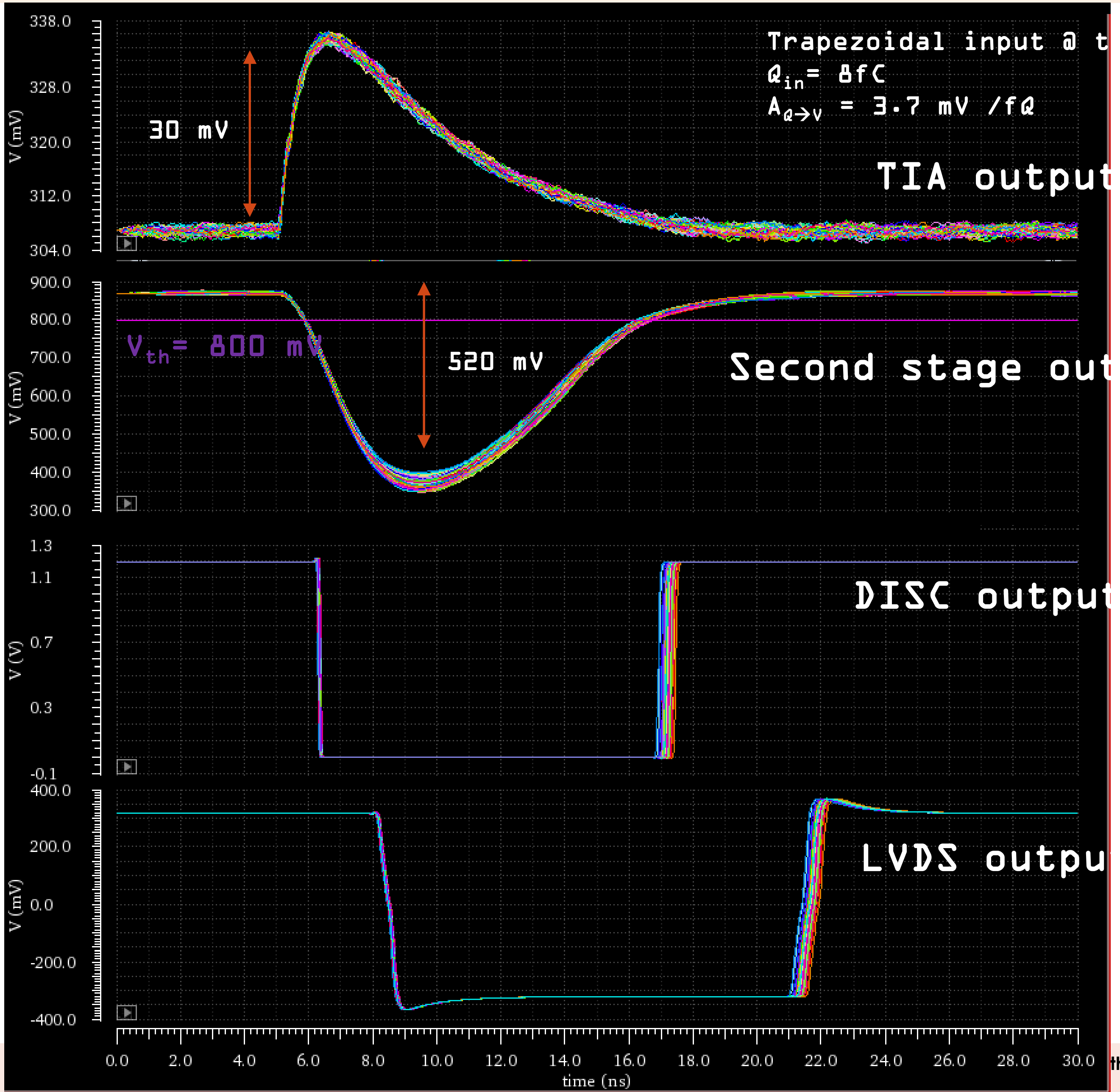
Jitter vs threshold



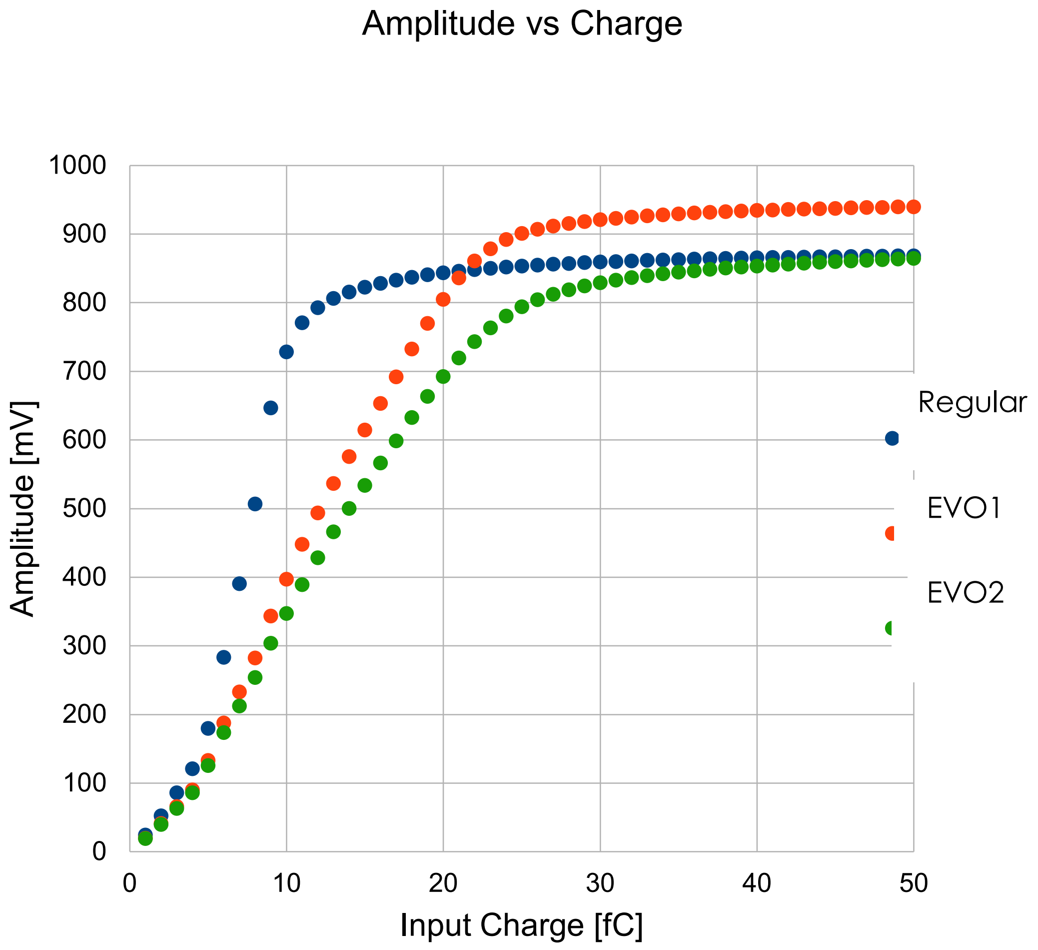


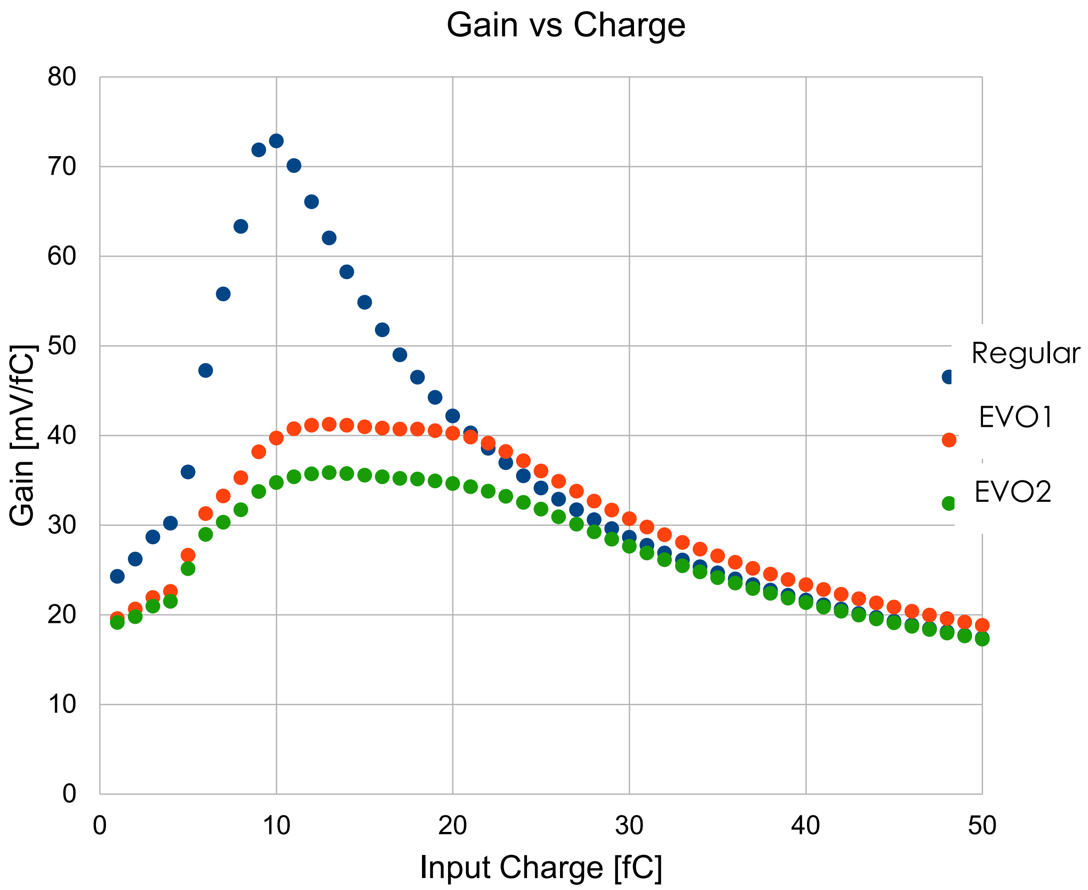
Cdet = 6 pF
Qin = 8 fC (trapezoidal)
Ibias = 1mA
T = 27 °C
Regular Rf = 20 K
EVO Rf = 11.6 K

Transient noise with R-C-CC-L parasitics

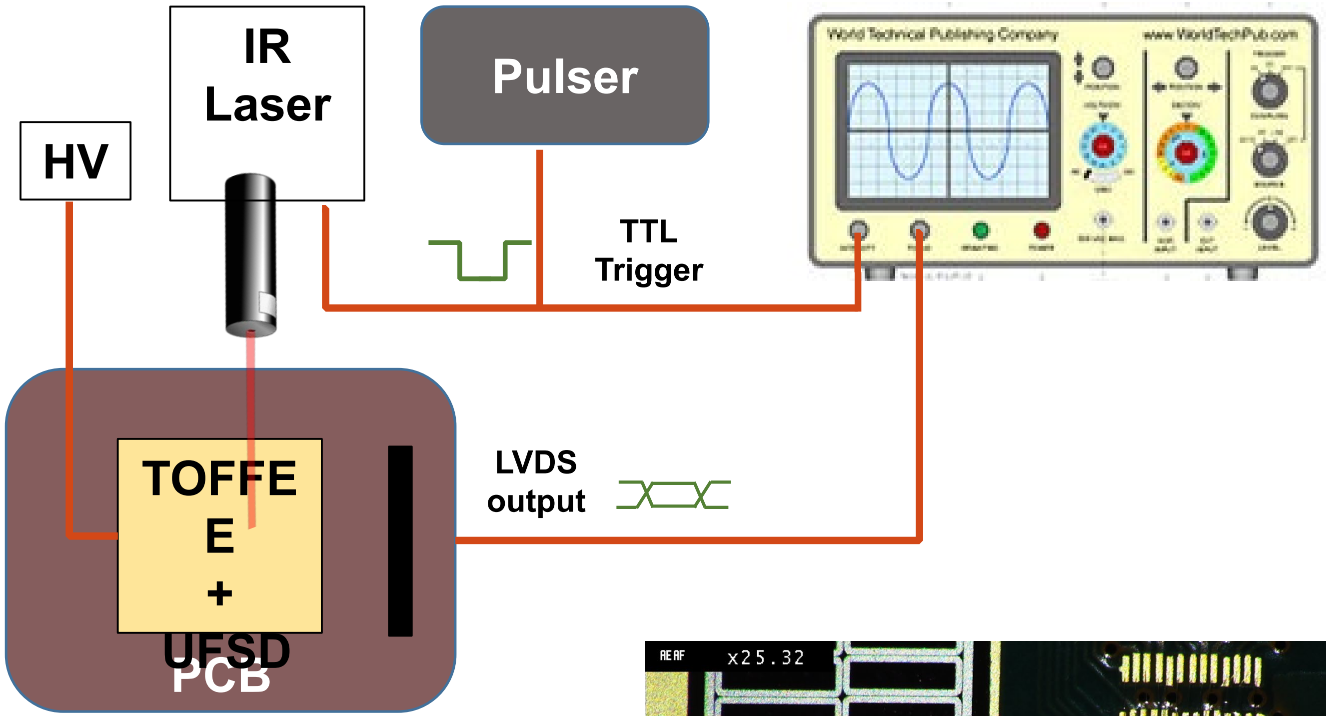


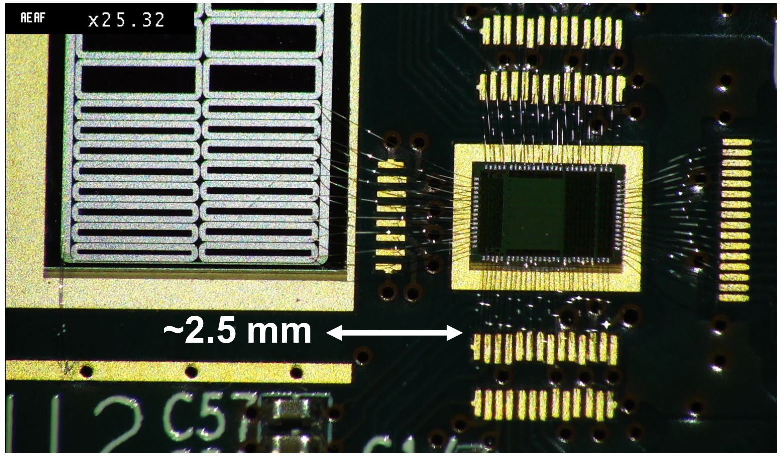
Front-end gain comparison

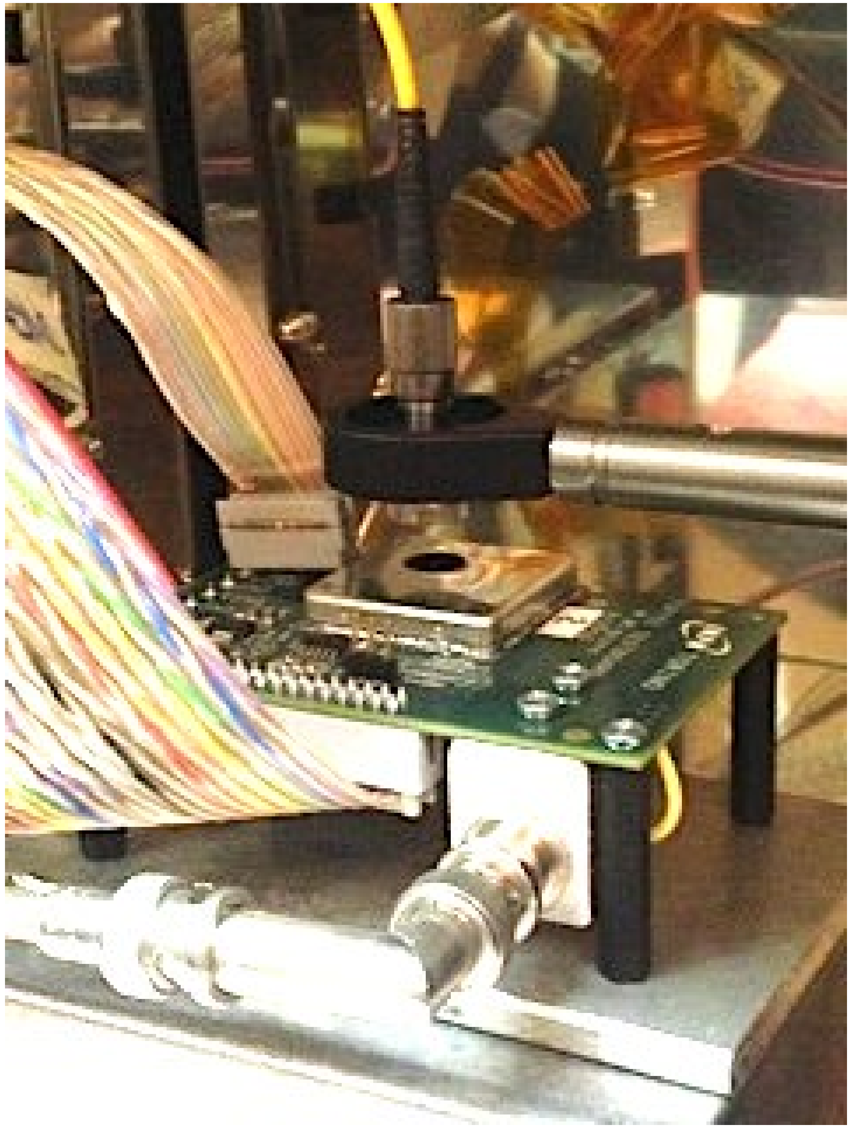




ASIC for UFSD sensors: TOFFEE



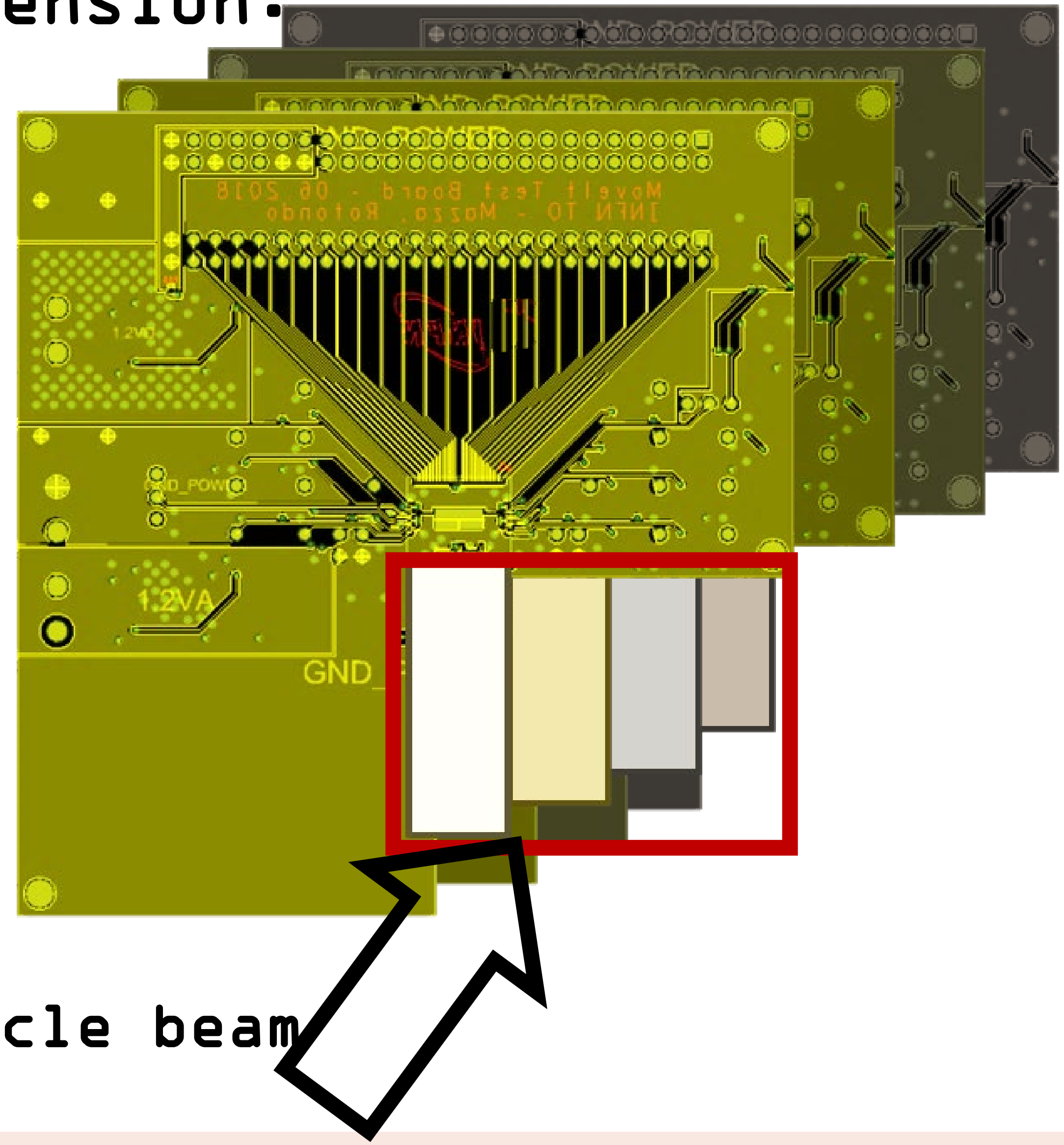




- Direct connection between CT-PPS module and the ASIC
- Climatic charmber used to reduce external interference
- Sensors depleted with ~200 V

ASIC for UFSD sensors: ABACUS

Active area extension:



Particle beam

Some examples from test beams

- **CMS HGCAL:**

  PIN diode thickness 300 μm A=25 mm2

  Cd = 8 pF en = 1 nV/√Hz td = 3 ns σ = 420 ps/Q(fC)

  1 MIP = 3.8 fC => σ = 110 ps/#MIP

  ~200 ps measured

- **ATLAS HGTD:**

  LGAD diode thickness 50 μm A= 2 mm2 G = 10

  Cd = 2 pF en = 2 nV/√Hz td = 0.5 ns σ = 50 ps/Q(fC)

  1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP

  ~40 ps measured

- **NA62 tracker:**

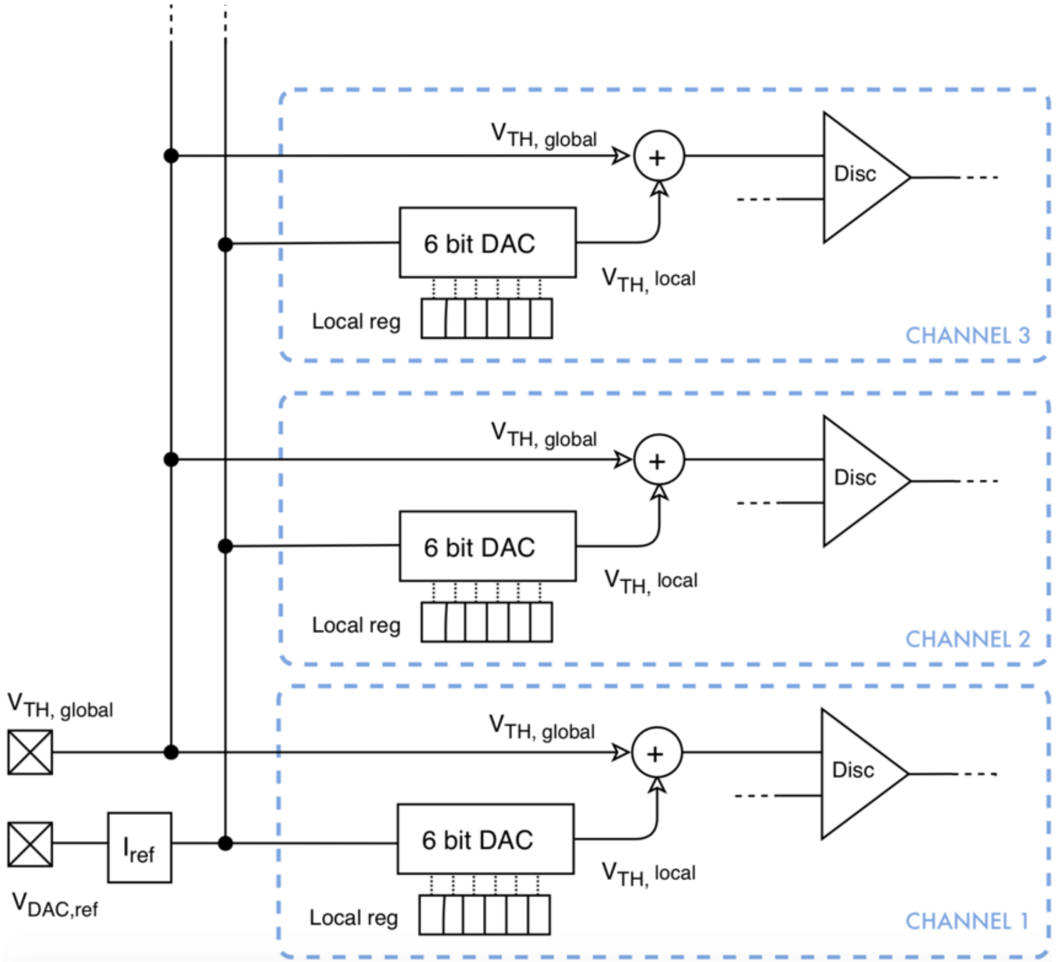
  PIN diode thickness 300 μm, A=0.09 mm2

  Cd = 0.1 pF en = 11 nV/√Hz td = 3 ns σ = 60 ps/Q(fC)

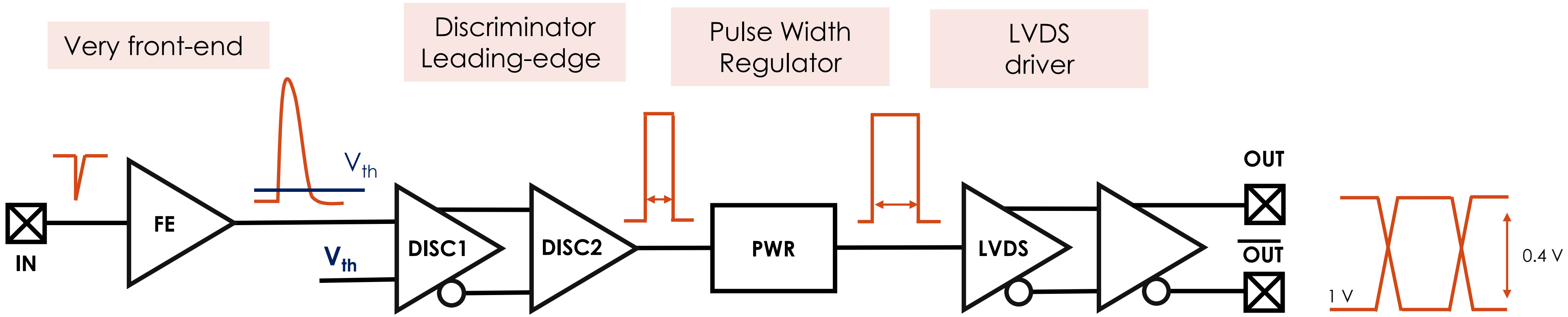
  1 MIP = 3 fC => σ = 20 ps/#MIP

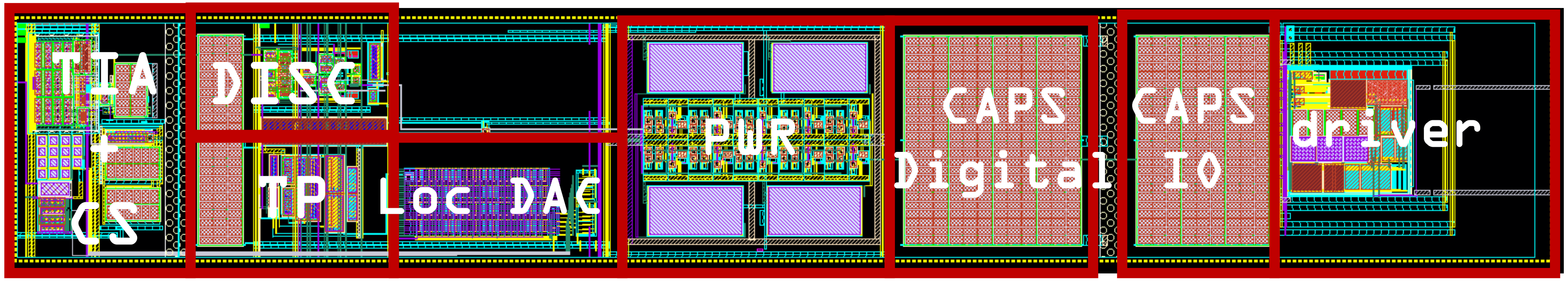
  ~60 ps measured

Threshold voltage generation

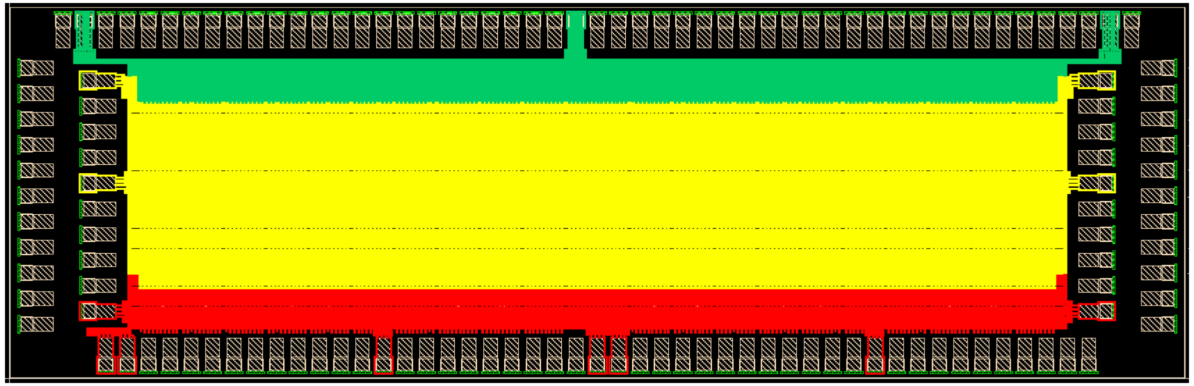


The channel of FAST



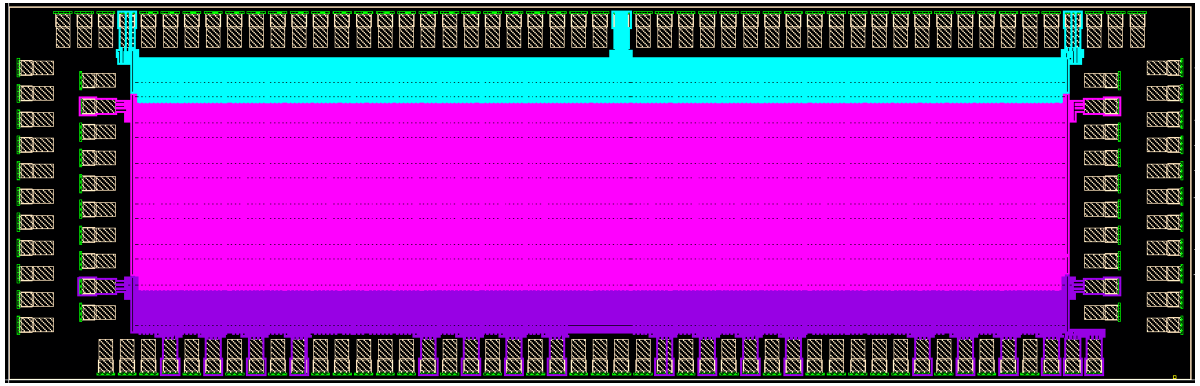


Power distribution: vdd, gnd, sub



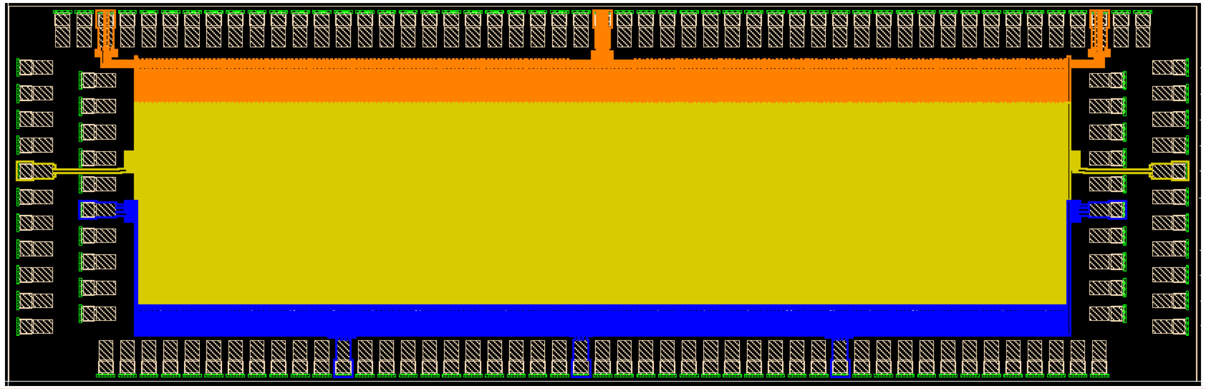
VDD

2 (+6) + 4 + 3



GND

2 (+ 18) + 2 + 3



SUB

2 (+3) + 2 + 3