The ATLAS Hardware Track Trigger
Design towards first prototypes

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The LHC will be upgraded to its final **high luminosity** form (the HL-LHC) from 2026 onwards

- It will deliver to both ATLAS & CMS around $3ab^{-1}$ of data at 14TeV!
- The instantaneous luminosity will have to be **upgraded** to $7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
- This equates to $< \mu >= 200$, i.e. on average **two-hundred** $p - p$ collisions per bunch-crossing!

To **thrive** in these conditions ATLAS will need to be **extensively upgraded**
What does $<\mu> = 200$ look like?

Currently ATLAS deals with around 40 collisions per bunch crossing, 200 is a large increase.

Will result in $\mathcal{O}(10,000)$ particles per bunch crossing.

Need to pick out the high-$p_T$ tracks of interesting objects from a swamp of low-$p_T$ particles.
The core of the ATLAS trigger strategy is centred around simple single and multi-object triggers, facilitating a broad range of analyses at the EW scale.

The rates of these triggers increase with instantaneous luminosity, some non-linearly!

In Run 4 the Level-1 trigger system will be upgraded to allow output at a higher rate,
- Level-1 rate: $0.1 \rightarrow 1 \text{ MHz}$
- DAQ throughput: $1 \rightarrow 50 \text{ TB/s}$

This higher rate is then passed to the Event Filter (EF), a CPU farm connected by a high-speed commodity network.
Information provided from tracking in the upgraded inner-tracker (ITk) will allow improved trigger rejection at the EF:

- Better track $p_T$ resolution, to reject low-$p_T$ leptons
- Early identification of the primary vertex to allow origin requirements to be made for objects (esp. jets/$E_T^{miss}$)

Track reconstruction is a CPU intensive process, and scales non-linearly with pile-up.

Without upgrades the $p_T$ thresholds of triggers will have to be increased.

The Hardware Track Trigger (HTT) will solve this by rapidly providing hardware-based-tracks to the EF system, reducing the CPU load.
**Baseline**: Regional (rHTT) and global (gHTT) tracking @ 1/0.1MHz input

**Evolved**: rHTT moves to L1Track at 30μs latency @ 4MHz input

- Track $p_T$ thresholds: regional (global) 2GeV (1GeV) and L1track 4GeV
The (baseline) HTT will act as a **co-processor** for the EF CPU farm, **reducing** the CPU requirements for tracking.

Will allow trigger thresholds in Run 4 to be maintained **despite** the extremely **challenging** conditions.

- $\mathcal{O}(500)$ boards grouped into **HTT-units**, housed in **ATCA shelves**
  - Units interfaced to the EF via dedicated servers, **HTTIF**
- Each unit will cover **one region** $\eta/\phi$ of the ITk
- All boards based on the same **Tracking Processor** (TP) motherboard
- Mount different **mezzanines** on the TP to change the boards role in the system
- Two **types** of TP
  - **AMTP**: Associative Memory TP, 12/unit
  - **SSTP**: Second Stage TP, 2/unit
- The **same units** will handle both rHTT and gHTT requirements
Tracking steps

**Pattern recognition** in AM ASICs (rHTT)
- Pre-computed 8-layer track patterns stored in associative memory, are compared to incoming clusters
- Reduced cluster resolution, uses **Super-Strips** (SS)

1st stage track fit in **FPGAs** (rHTT)
- 8-layer tracks with full cluster resolution
- Properties limited by short lever arm & distance to IP

2nd stage track fit in **FPGAs** (gHTT)
- Full 13-layer tracks, close to offline resolution provided
- ITk inputs split into overlapping $\eta/\phi$ segments, passed to dedicated HTT-units to run required steps
TP Board Layout

- **High-bandwidth** motherboard with:
  - 1 large or 2 small **mezzanines**
  - **10Gb/s** links
  - Large FPGA on board
  - **System-on-chip** for data control system (DCS) and monitoring
  - **ATCA** support and connectors

- Demonstrator boards **ready** this month, aim to **validate** design choices and modelling of:
  - Thermal and mechanical **modelling**
  - Low profile **Z-ray** connectors for mezzanines
  - **High-speed** links
  - Readiness for **integration** and cooling tests @ CERN in 2020 and onwards
TP board will be **responsible** for the following functions:

- Data **sharing** and **switching** to/from the HTTIF and mezzanine cards
- Pixel hit **clustering** to reduce data size
- Track duplicate **removal**
- Event **synchronisation**
- Running the control system and allow **monitoring** of the system
AM09: Associative Memory ASIC

- The **AM09** chips form the **central** component of the HTT **pattern recognition** system.

- A **low-power** CMOS device for parallel **bit-wise** comparison of incoming clustered hits with **pre-stored** patterns.
  - About **30 peta-comparisons** per second per chip!
  - **Low** power and size allow many chips per board.

- The **future** AM09 chip will be used for HTT, an **evolved** version of the successful AM06 used in FTK.
  - Will take 8 layers of ITk inputs at **1Gbps**
  - Power consumption **driven** by bit-comparison rate
    \[ P = 1W + \text{<Rate>} \times 0.05W/MHz \]
  - \(16b\times50\%\) bit-flip @ 50MHz, on 8 buses \(\rightarrow 2.5W\)

### Prototype AM07 ASIC

<table>
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<th>ASIC</th>
<th>year</th>
<th>technology</th>
<th>patterns</th>
<th>clock [k] [MHz]</th>
<th>power [fJ/comp/bit]</th>
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<td>AM09</td>
<td>2021</td>
<td>28</td>
<td>(3\times128)</td>
<td>250</td>
<td>0.42</td>
<td>KOXORAM+</td>
</tr>
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</table>
The PRMs are **single** board mezzanines on an AMTP board containing:

- **One large FPGA**: Current candidate an Intel® Stratix® 10
  - Performs linearised $\chi^2$ fit for 1st stage tracks
  - 1GHz fits/board
  - High-bandwidth-memory (HBM), removes need for external RAM to access fit constants
  - Handles data sharing

- **Four blocks** of 5 AM09 ASICs per PRM:
  - **Storage** for $\approx 7.5$M patterns/PRM
  - **Peak** cluster rate/layer: 250 MHz

- Reduced the AM/PRM from 6 $\rightarrow$ 5 to meet power constraints
- Demonstrators **ready** in early 2020 ready for integration tests
Track Fitting Mezzanine (TFM)

- **Two** TFM s are connected to each SSTP board
  - Performs the **second stage** tracking (gHTT)
  - **Extrapolates** the 1\(^{st}\) stage (PRM) 8-layer tracks to the full 13 ITk tracks
  - **Fits** (a further \(\chi^2\) fit) the full track parameters

- One large FPGA: **Current** candidate a Intel\(^{\text{\textregistered}}\) Stratix\(^{\text{\textregistered}}\) 10 MX
  - **High-speed** links to the TP
  - **HBM** for the fit constants

- **Same** connectors and similar heat-sinks as the PRM

- Demonstrator board **expected** in December 2019
  - Firmware **under development**, partially based on FTK experience
  - Prepare for **integration** tests in 2020
System Summary

System Size

- **576** AMTP boards in **48** ATCA shelves
- Containing **11520** AM09 ASICs
- **192** TFMs on **96** SSTP boards
- **1440** FPGAs (TP+PRM+TFM)
- **Additional** PCs for HTTIF, DCS and monitoring
- A highly **modular** and **flexible** system!

Power/Data-flow Estimates

- Total HTT power and data rates under study (final numbers still under internal review)
- Currently **within** the capabilities of the **available** cooling and limits of the DAQ system
The **Hardware Track Trigger** system is a crucial component of the ATLAS trigger upgrades for the HL-LHC.

- System described in the 2018 TDR

**Baseline**: Run as both a regional and global tracking co-processor to the Event Filter @ 1 MHz and 100 kHz respectively.

**Evolved**: Regional tracking to L1Track, running at 4 MHz on Level-0 inputs.

**Modular** design: Track processor + Mezzanines
- Pattern Recognition Mezzanine (1\(^{st}\) stage fit)
- Track Fitting Mezzanine (2\(^{nd}\) stage fit)
- **Flexible** and modular system allows the same boards to be used in both scenarios.

#### Status

1. **Base** design, power and data flow estimates made ✓
2. System specification review concluding
3. Demonstrator boards for all components being produced to begin integration tests in 2020
References

- Bulk of information found in the Phase-II Trigger Upgrade TDR

1. Phase-II Trigger Upgrade TDR

2. ITk TDR

3. FTK TDR
   https://cds.cern.ch/record/1552953


5. https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults

6. https://twiki.cern.ch/twiki/bin/view/AtlasPublic/PhysicsAndPerformancePhaseIIUpgradePublicResults