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RADSAGA System Level Test Review November 12th, 2019





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Some definitions

In the context of radiation hardness assurance a system shall be considered as any assembly of two or more devices:

- which concur to deliver a functionality that none of them can deliver by itself;
- for which at least one of the devices is sensitive to radiation effects which can impact the functioning of at least one other device or the assembly as a whole.

Custom-built system based on COTS parts

- Designed by the end user with direct control on features such as part selection and traceability
- Radiation-based design

Fully commercial (COTS) System

- System bought off-the-shelf with no control on part selection and traceability
- No architecture/schematics available
- Not radiation-based design
- E.g. SoC



Application areas

• People in the community are using system level testing

Space

- Limited in-situ testing
- Dedicated to commercial boards/subsystems

Accelerator

- Implemented in the RHA process for accelerator equipment at CERN
- Guidelines

Ground and avionics

- Test of specific applications
- Dedicated to high reliability electronics









System Level Testing as a Tool

Increasing Cost





System Level Test Types

Global on the system

- Irradiation of full system
 - Synergistic effects
 - Radiation source provides TID, DD and SEE
 - CHARM
 - High energy protons
 - Isolate TID from SEE (or DD)
 - Individual radiation sources
 - Co-60 + Spallation neutrons
 - Co-60 + Very high energy heavy ions (usually rather low LET)

Targeted on components

- Focus on only one component to check effects on system functionality
 - Fault injection schemes
 - Only effects (and user-biased), no rate for application
 - Laser testing
 - Only effects, no rate for application
 - Heavy ion testing
 - Effects and rate as a function of LET



System Level Test Types

Global on the system

- Only high penetration beams
- Beam field homogeneity needed
- Reduced beam time cost
- Reduced sample preparation cost
- Global functionality monitoring and rates

Targeted on components

- Multiple ion strikes are rare in application
- May not be cheaper than individual component testing
- Still needs sample decapping
- Test planning may be very elaborate
- No global functionality rates

- Verification of mitigations
- Get information on failure modes features
- Assess need for additional mitigations



Promising radiation testing methodologies

Survey from the RADECS Emerging Assurance Qualification Methods for Commercial Systems Modeling and Experiments, Pasadena, CA, October 28-29, 2019





Existing Guidelines

Board level proton testing book of knowledge for NASA electronics parts and packages program (Guertin, 2017)

- Example application: non-critical electronic equipment for the ISS
- Test with higher energy to limit TID (200 MeV)
- Good estimator for soft errors, but very poor for destructive events
- It provides only a quite large upper bound to failure rate prediction
 - Untested board upper bound 0.1 failure/board-day
 - Fluence of 10¹⁰ p/cm² 0.01 failure/board-day
 - Fluence of 10¹¹ p/cm² 0.003 failure/board-day
- Estimated to cost 10 times less than individual device testing



Energy deposition and SEU rates for ISS orbit and proton testing. Good agreement for energy depositions in the 1-10 MeV range. The region above the proton testing cutoff brings a marginal contribution.



Existing Guidelines

Guideline for ground radiation testing of microprocessors in the space radiation environment (Irom, 2008)

- First good example of testing complex devices whose findings can be extended to digital systems
- Provides different test schemes
- Provide a list of sub-components that have to be tested
 - Registers
 - Cache memory
 - Operational SW
 - Program hangs
- Reports on orders of magnitude variations in the functional SEFI cross section as a function of firmware and software

Test Methods	Self Testing Single Computer	Controller Assisted		Controller Dominated	
Trade Off Criteria	r	Single Computer	"Golden Chip"	Single Computer	"Golden Chip"
Effective Clock Frequency	High	Medium	Medium	Low (< 10 KHz)	Low (< 10 KHz)
Individual Element Test Ability	Low	High	High	High	High
Error Table Structure/Data Display	Simple	Complex	Complex	Complex	Complex
Test Preparation Lead Time	Short	Medium	Medium	Medium	Long

Other works:

- FPGA Single Event Effect Radiation Testing (Berg, 2012)
- SoC Single Event Effect Testing Guideline development (Guertin, 2013)



Existing Guidelines

Qualification of Electronics Components for a Radiation environment when standards do not exist (Uznanski, 2017)

• **Design and validation process** applied to the FGCLite and extended to other accelerator equipment

Class	Radiation response	Sourcing	Components
Class-0 (potentially sensitive)	Quite resistant or moderate sensitivity to radiation	Easily replacement Different manufacturers and types on the market	Diodes, Transistors
Class-1 (potentially critical)	Potentially susceptible to radiation, not on system's critical path	Substitution possible (list of preferable replacements is defined)	Voltage regulators/ references, DACs, memory
Class-2 (highly critical)	Potentially susceptible to radiation, on system's critical path	Difficult to replace as no equivalents on the market	ADCs, FPGA mixed circuits for field bus

Add whether I have radiation data for these parts from someone else at component level or that was recovered through system level







Existing Guidelines

Guidelines for the Radiation Hardness Assurance for CERN accelerators equipment (Danzeca, CERN internal)

- Very first inclusion of system level testing within the design process and validation of a system to replace system modelling
- First classification of failure modes at system level
- Procedure to identify failure modes based on SEE or TID/TNID
- Defines the required protocol to be followed for radiation testing at CHARM.





Within the community

- Radiation effects engineers have been doing board/module/sub-system/system level testing over the last 20 years
- There's currently no session in conferences for radiation effects at system level and some publications may fall out of scope within TNS
- There's very poor documentation in literature of such tests
 - Tested applications may be IPs
 - **Confidentiality** needed for parts used within the system
 - Lack of standardization on how system level data shall be reported
 - e.g will the test report of a commercial PCB contain all the information that are needed if someone wants to buy and use the same PCB?



Within the community

Double-sided board testing of a data acquisition unit at NSRL (De Bibikoff, 2019)

- Presented at RADECS 2019
- Board modelling with TRIM
- Required beam energies
- Selection of ions for targeted LETs
- Perform **SEL measurements** with new techniques





- Higher energies can reduce energy gaps due to the Bragg peak among consecutive components
- Ion beam fragmentation increases with energy



Within the community

GEFE – Gigabit Transceiver based Expandable Front-End (CERN BE-BI)

- FPGA-based rad-tol card for multi-purpose applications:
 - Fast data acquisition
 - Slow control installed in the beamline
 - Used in other systems according to user's needs
- Card qualification at CHARM
 - Based on simplest functionality
 - Use of **architecture** structure that will likely be replicated by users
- Will be tested at CHARM in the various systems that will make use of it





Within the community

CELESTA (Secondo, 2018)

- First example of **full satellite** tested at CHARM
- Payload is a space version of the CERN Radiation Monitor (self-monitoring of the beam flux)
- Test at different fluxes and dose rates
- Observed same degradation of SEL cross section measurements as it was observed during component level testing
- The first test outcome was actually 'fail':
 - Communication to the payload was lost at 140 Gy(Si)
 - Root cause was identified
 - Mitigation was applied





Objections to system level testing

With respect to no testing

- It is expensive
- I don't know how to do it
- It's not recognized by certification institutes as a way to perform RHA
- It is done only for in-house developments

With respect to replacing component level testing

- It is a **pass/fail** test
 - Not clear what to do if the outcome is 'fail'
- Lack of observability
 - I may not understand what went wrong
- Worst Case Analysis for TID
 - Cannot be performed without individual component level testing
- Data portability
 - I have to start over even if I use same components
- Limited level of confidence



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