ESR 13 FPGA modules for avionic and new space applications

RADSAGA System Level Test Review– November 12

Israel Lopes

Supervisor: Vincent Pouget

Co-supervisor: Ketil Røed

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie-Sklodowska-Curie grant agreement number 721624.

Outline

- Context
- State-of-the-art
- Methodology
- Case study
- Radiation experiments
- Results and Discussion
- Conclusion

Context

- Digital system under study:
  - Commercial Industrial Digital System-on-Modules (SoMs)
    - Including state-of-the-art System-on-Chips (SoCs)
  - Application: Control loop

- COTS components
- Space and atmospheric environments
- Cost-effective qualification approach
- Small-sats and non critical missions
- Short and long duration missions

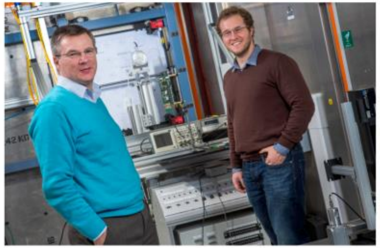
Partners

- RADSAGA network

- University of Montpellier
  - Institute of Electronic and Systems (IES)

- Facilities
  - ISIS ChipIR atmospheric neutron facility
  - KVI-CART high-energy proton facility

Science & Technology Facilities Council
ISIS Neutron and Muon Source



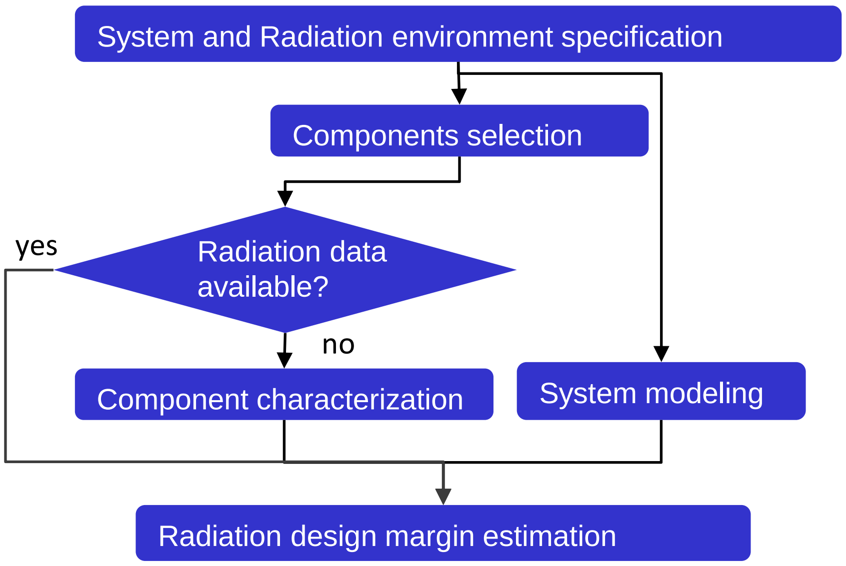
The ChipIr team Dr Chris Frost and Dr Carlo Cazzaniga

RADSAGA

Conventional Radiation Qualification Methodology

Component Level approach

- Bottom-up approach
- Used for hardened and COTS components
- Benchmark application used
- System-level reliability is estimated with significant margins
- Sensitive components can be replaced or protected by system-level solutions
- Particle beams: Low and High energy protons and heavy-ions, and high energy neutrons
- Gamma ray source: 60Co
- Reference standards:
  - TID: ESCC 22900, MIL-STD 883 Method 1019, MIL-STD 750 Method 1019
  - SEE: ESCC 25100, MIL-STD 750 Method 1017, JEDEC 89A

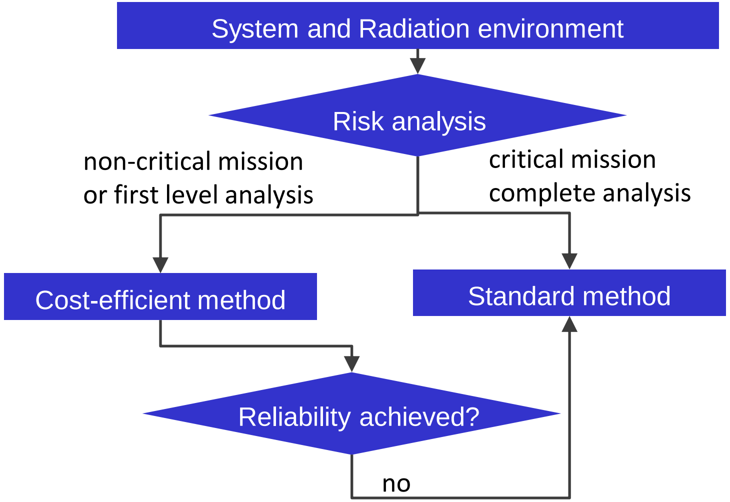


[AIRBUS, RADECS 2017- Short course]

Emerging Radiation Qualification Methodology

System Level approach

- Top-down approach [3]
- Best-suited for COTS systems [1][2][3]
- Mostly used for non-critical missions [3] or small[4] and cube sats[5]
- “Test as you fly” [1]
- Direct system-level reliability estimation
- High penetration beam with large spot size required
  - 200MeV proton test commonly used [1]
  - Atmospheric neutrons (< 800MeV)
  - CHARM AND NSRL alternatives
- Low fluences
  - Screen most sensitive components
- Higher fluences [2]
  - Better coverage of fault modes
- No test standard available



[Rousselet, RADECS, 2016]

[1] Guertin, Board level proton test book, 2017
[2] Ladbury, NSREC 2017 Shortcourse
[3] Uznanski, RADECS 2017 Shortcourse
[4] Julien, AeroConf, 2017
[5] Secondo, TNS, 2018

RADSAGA

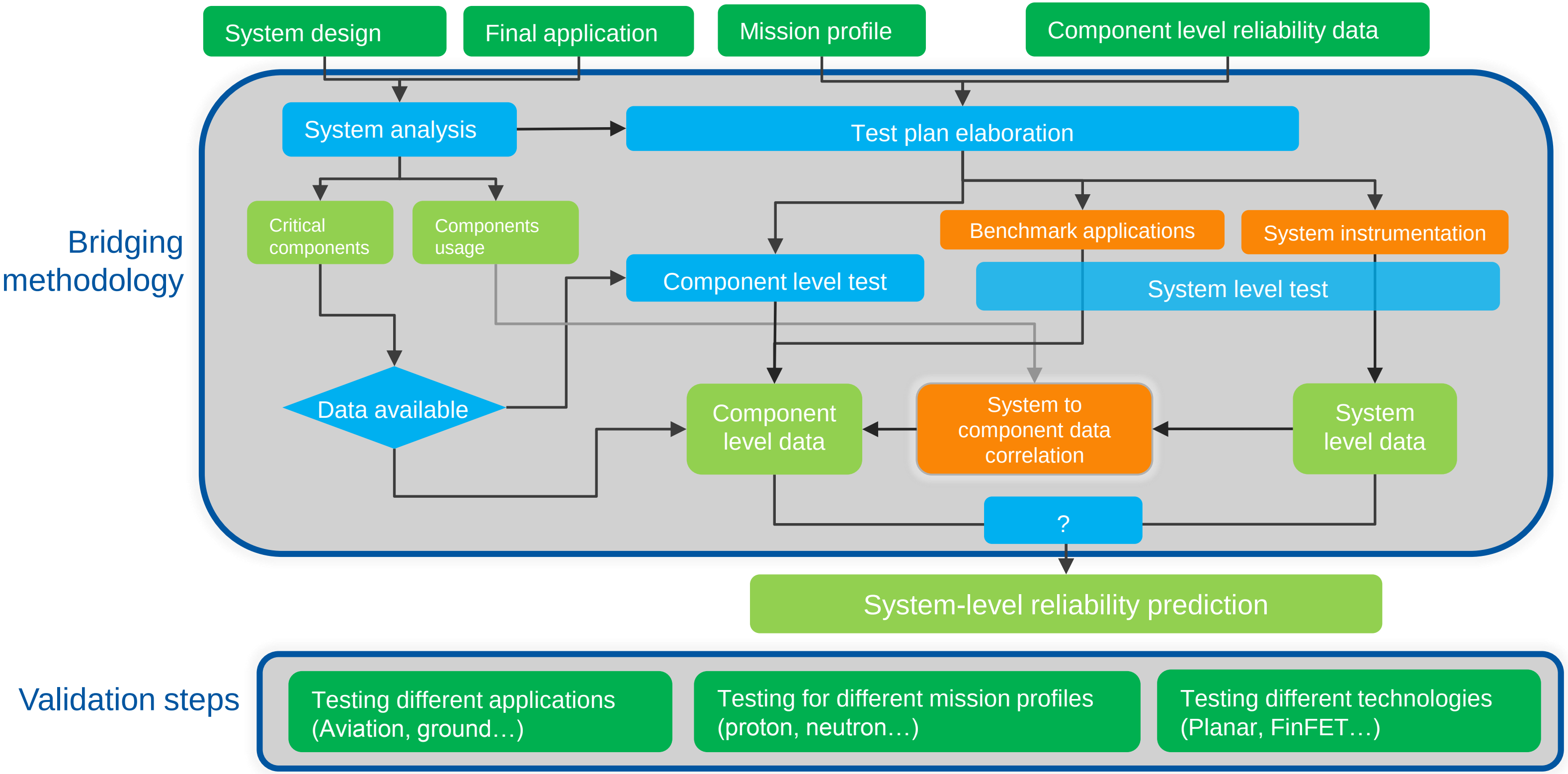
Component vs System level approach

	Component	System
Cost	☹	🙂
Reusability	😐	☹
Component observability	🙂	☹
System observability	☹	😐
Evaluation of complex Components	☹	🙂

- Component observability enables data reuse
- System-level observability enables more direct system failure analysis
- Component data usually not reusable for complex components (SoC, FPGA etc)
- A combination of both methodologies is required

RADSAGA

Bridging methodology development



RADSAGA

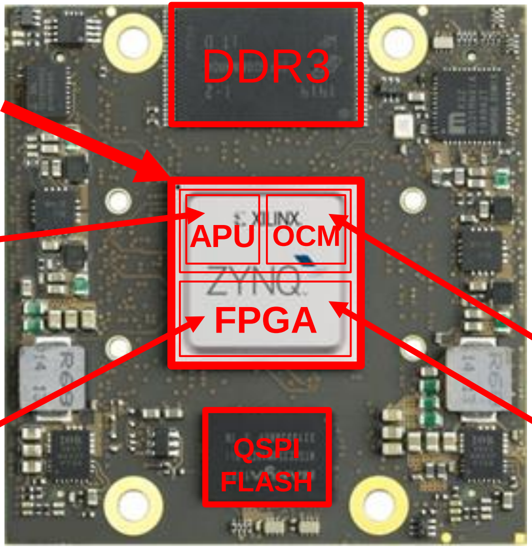
System-on-modules

Zynq7000 System-on Module

28nm CMOS Zynq7000 System-on-chip

Dual-core Application Processing Unit

Programmable Logic (PL)



On-Chip Memory SRAM

Block-SRAM (BRAM) embedded

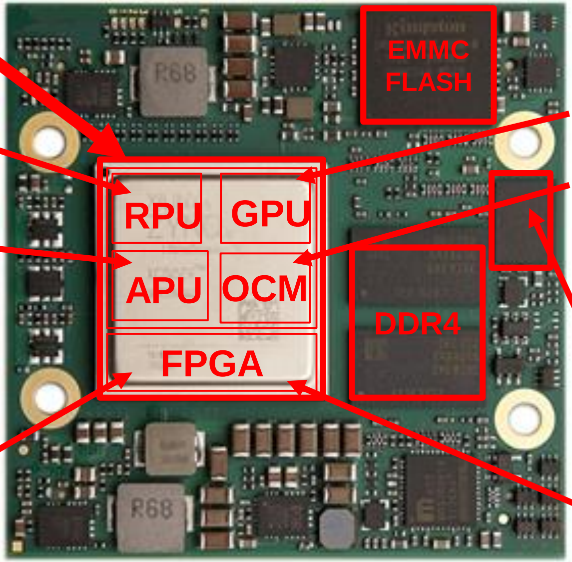
Zynq Ultrascale+ System-on Module

16nm FinFET ZynqUltrascale+ System-on-Chip

Dual core Real-time Processing-Unit

Quad core Application Processing-Unit

Programmable Logic (PL)



Dual core Graphics Processing-Unit

On-Chip Memory SRAM

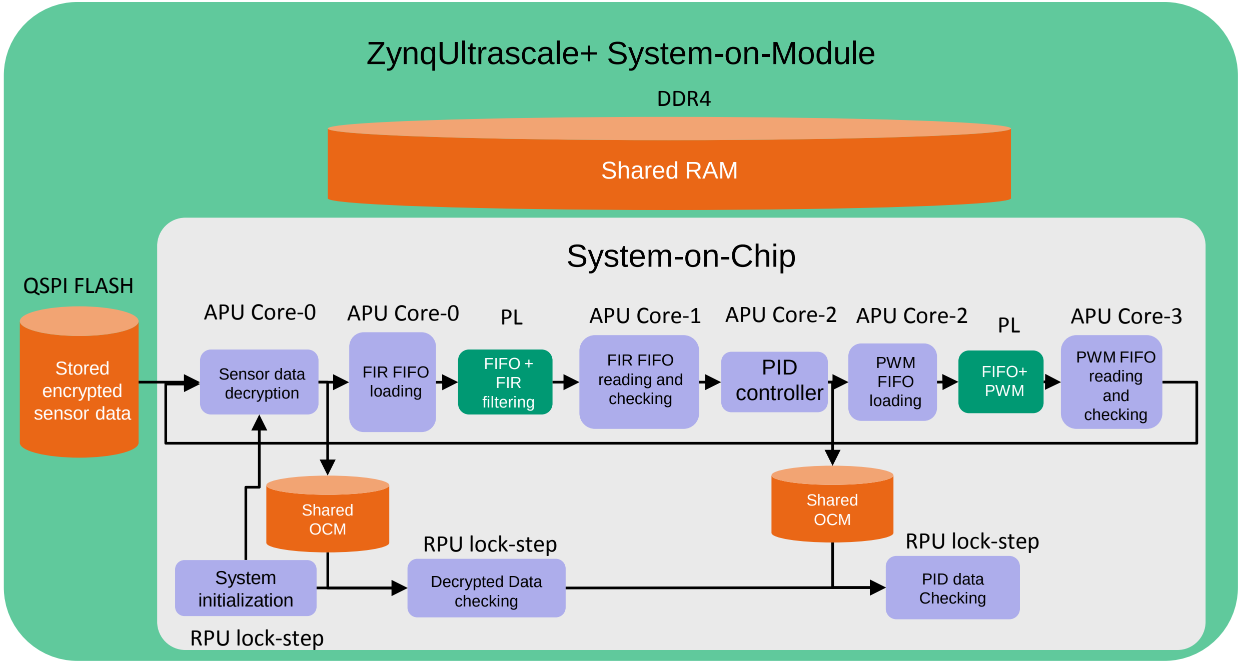
QSPI FLASH

Block-SRAM (BRAM) embedded

RADSAGA

Application: Control loop

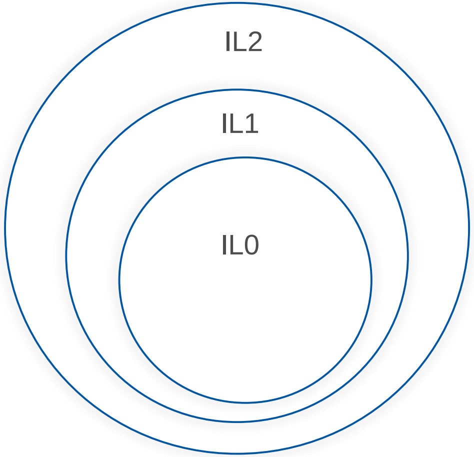
- Representative application of a space or avionic embedded digital system
- **Data processing loop**
  - AES decryption
  - FIR filtering
  - PID controlling
  - PWM actuation
- **Resources under test:**
  - DDR, QSPI FLASH, OCM, APU and PL (FPGA)
- **Self-test controller** implemented with RPU



Software/Firmware **instrumentation**

- **Instrumentation =** adding IP or code elements to the application to improve system's observability and failure diagnosis

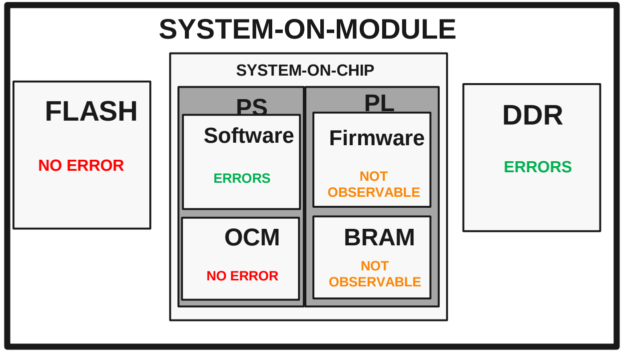
- Different levels of instrumentation are implemented and can be activated dynamically during the campaign:
  - **Instrumentation level 0 (IL0) – Application control**
    - Counter-based watchdogs
    - Status checking: FLASH, PL FIFO
    - Application output checksum
  - **Instrumentation level 1 (IL1) – mostly external resources checking**
    - FLASH and DDR ECC checking
    - Intermediate applications checksums
  - **Instrumentation level 2 (IL2) – Internal resources checking**
    - BRAM and OCM ECC checking
    - SoC registers checking

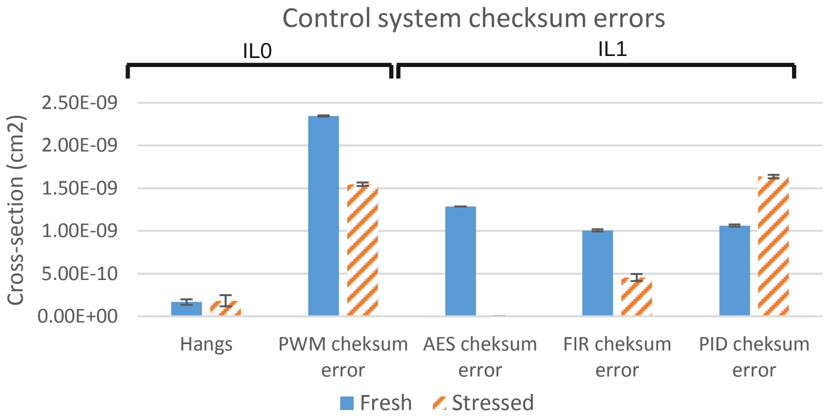


Component/System neutron experiment

- **Facility:** ChipIR atmospheric-like neutrons (<800MeV)
- **Systems under test:**
  - Run 0: ZYNQ7000 SoM + benchmarks (DDR3, QSPI)
  - Run 1: ZU+ SoM + benchmarks (DDR4, QSPI, OCM)
  - Run 2: ZU+ SoM + application (IL1)
- Fresh and temperature-stressed components tested
- Runs 0 & 1:
  - No error in QSPI FLASH, no error observed in ZU+ OCM
  - DDR3 and DDR4 SEUs, MCUs, and probably SEFIs
- Run 2:
  - IL1-related errors observed
  - Soft and Hard SEFIs observed (low statistics)
- Simple test-bench with only software instrumentation
  - Provides first set of useful results at system and component level

Results summary

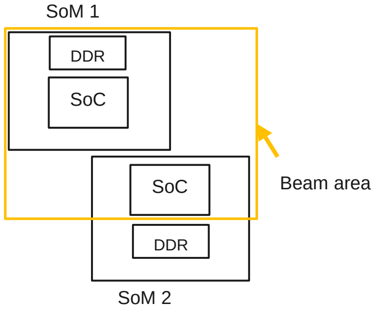




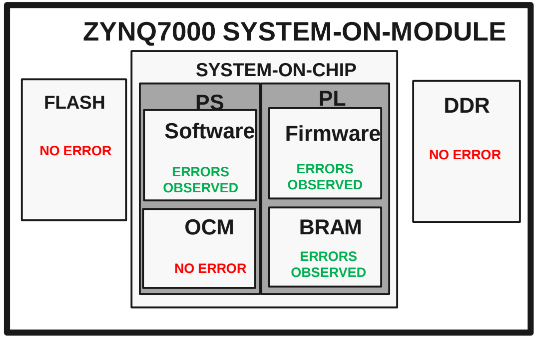
Component/System proton experiment

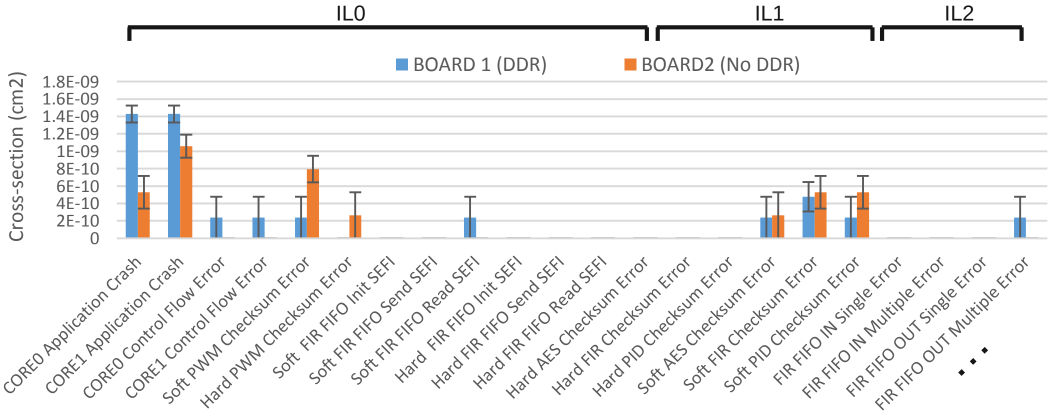
- **Facility:** KVI-CART, protons at 184MeV
- **Systems under test:**
  - Run 0: ZYNQ7000 SoM + benchmarks (DDR3, OCM)
  - Run 1: ZYNQ7000 SoM + application (IL0-2)
  - Two boards in parallel: 1 with full SoM exposed, 1 with DDR out of the beam
- Run0 (low fluence ~1E8, facility issue) :
  - No OCM and DDR errors
- Run 1(low fluence ~1E8-9, facility issue) :
  - Influence of DDR on application crashes could be extracted
  - Different types of errors could be observed using IL0 and IL1

Experiment layout



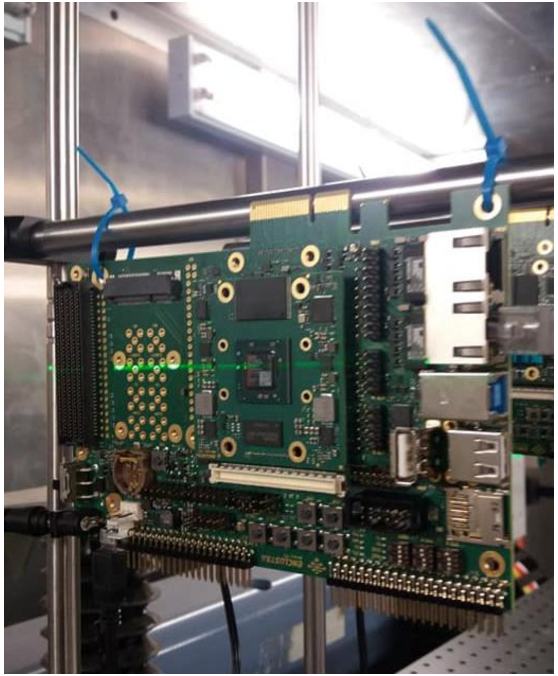
Results summary



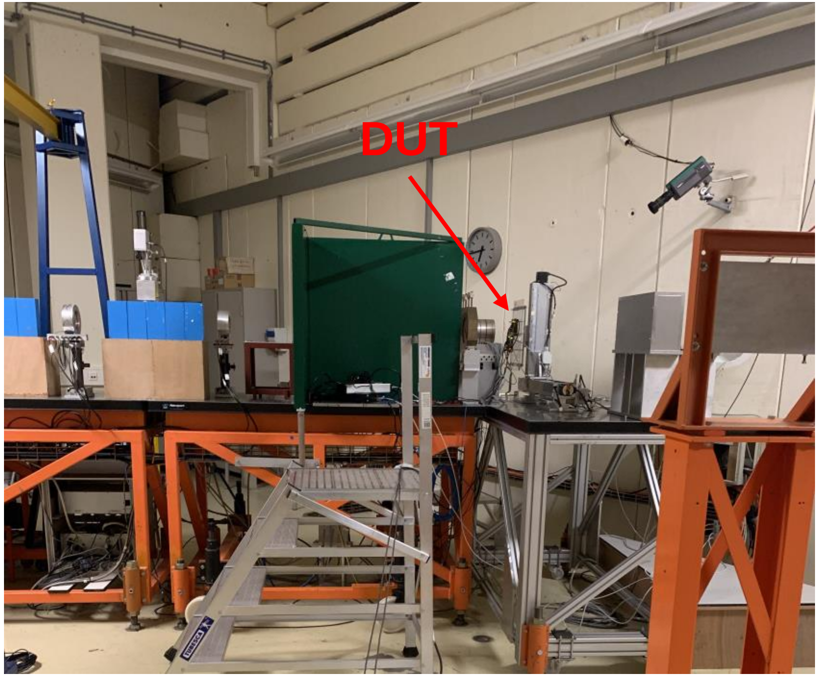


Component/System experiments

ChipIR experiment



KVI-CART experiment



Results summary

- **System-level testing of 2 commercial digital SoMs**
  - Pros
    - Direct obtention of a system's fault signatures catalogue (with their relative rates)
    - Good observability of soft failures in digital parts could be achieved using software instrumentation
      - Instrumentation requires source code access
      - Many different kind of events with low statistics
    - Besides the final SW application, benchmarks can help in improving the test coverage
    - Excluding a component from the beam (or masking it) can help in isolating a sensitive component
  - Cons
    - Lack of observability of SEL and analog parts (power regulators)
      - Could probably be achieved by minor hardware modifications (full schematic required, test complexity ↑)
      - No destructive event observed during the campaigns

First set of guidelines and recommendations

for system-level testing of a digital System-on-Module

- Increasing the observability is a key
  - Gives more value to the collected data
  - Facilitates the implementation of fault-tolerance solutions at system-level
  - Solution: implementation of flexible Software/Firmware instrumentation
    - Can be automated at compiler level
    - Could include benchmarks as parasitic workload
    - Optimal use of embedded resources required to limit the overhead

- Fault injection techniques can be used
  - Laser testing, SW or HW-based techniques
  - Before testing: to tailor the instrumentation design
  - After testing: for root cause analysis of critical events

- Make a good use of the beam geometry or component masking possibilities

Conclusions and future prospective

- Bridging methodology from component to system-level
  - Finding an intermediate path to make an optimal use of both levels, and to facilitate the transition to system-level testing
  - Opening the use of state-of-the-art technologies and devices
  - Reducing margins
  - Reducing costs
- First sets of experimental results and guidelines
- Future works
  - New proton campaign (KVI-CART) in <2 weeks for testing the ZU+ SoM
  - X-ray TID campaigns in progress (IES)
  - Laser tests of ZU+ SoM (IES)
  - Still being considered for early 2020:
    - feasibility of an heavy-ion campaign (RADEF)
    - ageing campaign (IES)

Conclusions and future prospective

- Applicability to a future qualification methodology
  - The proposed methodology relies on well-established practices:
    - Testing with ~200MeV proton or atmospheric-like neutron spectrum
    - “Test as you fly” (i.e. using the final SW application)
  - An originality of our approach:
    - Different levels of software instrumentation to improve system’s observability (first results to be published)
    - The approach needs to be generalized and tested on other architectures
    - Could be standardized through the development of a standard library compatible with various architectures

  - The question of optimal use of system-level test data to estimate system failure rates still requires new modular SW tools for rate prediction (for instance: starting from the basis of SEAM [1] capabilities)

[1] https://modelbasedassurance.org/