CADENCE simulation of Micromegas NSW LM1 resistive layer

Layout :

- The ATLAS – NSW upgrade
- MM for the ATLAS – NSW upgrade
- The resistive layer (brief) description
- Previous calculations
- Some of our (preliminary) results
- Conclusion

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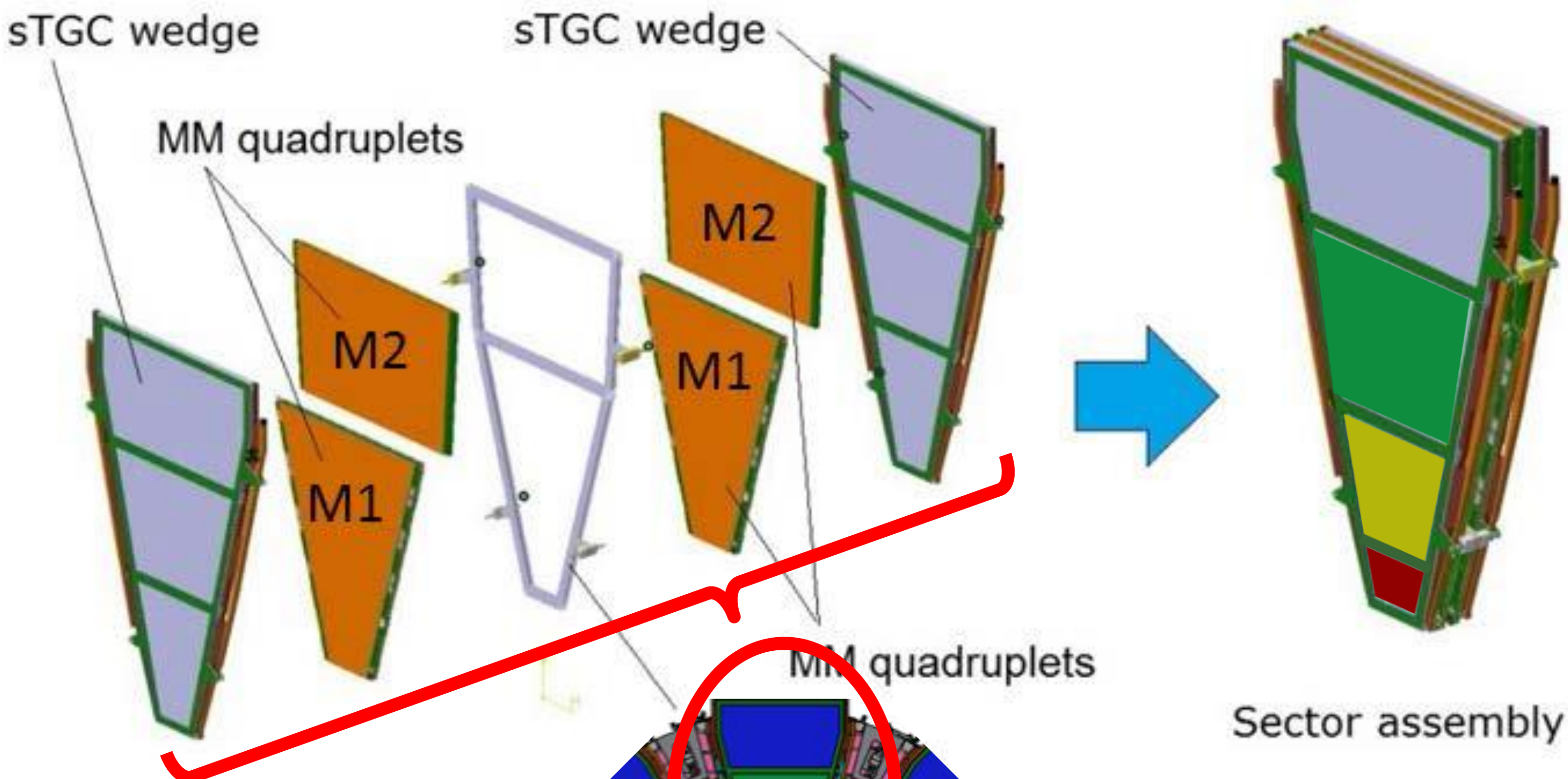
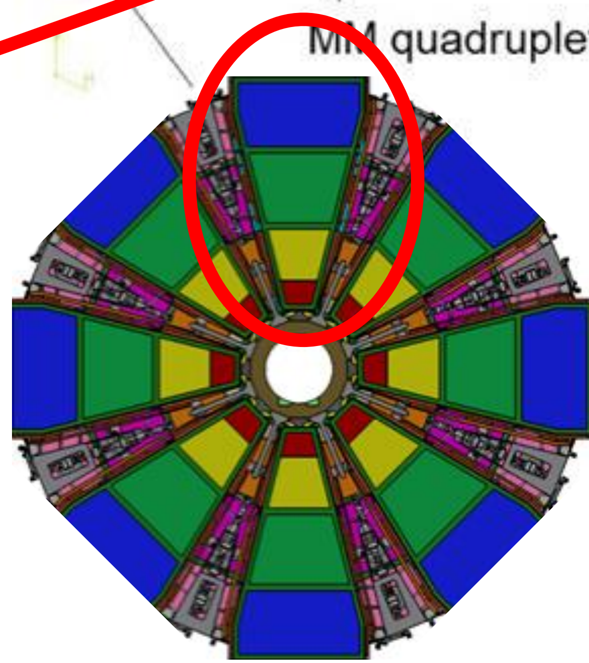
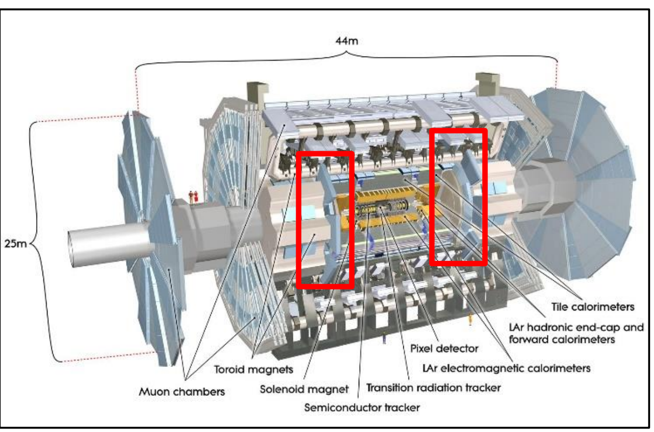
Work done during his Master-2 internship in CEA Paris-Saclay

Also thanks to Fabrice Guilloux (IRFU) for his expertise using CADENCE program

RD51 week, 21 - 23/10/2019 at CERN





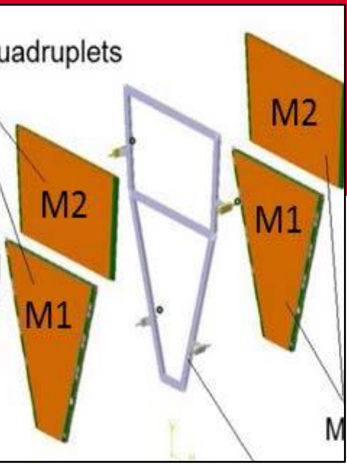


Each Micromegas (MPGD) and sTGC (MWPC) modules are 4 planes detector

For Micromegas there is :
8 sectors x2 modules
x 2 wheels

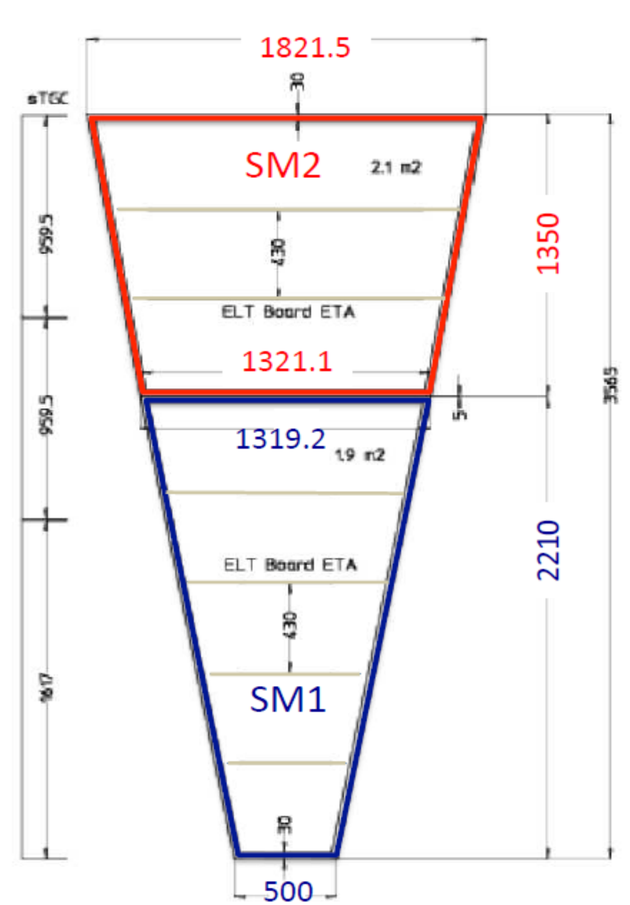
=> 32 modules of each type to be build (4 types)

Structure of MM detectors

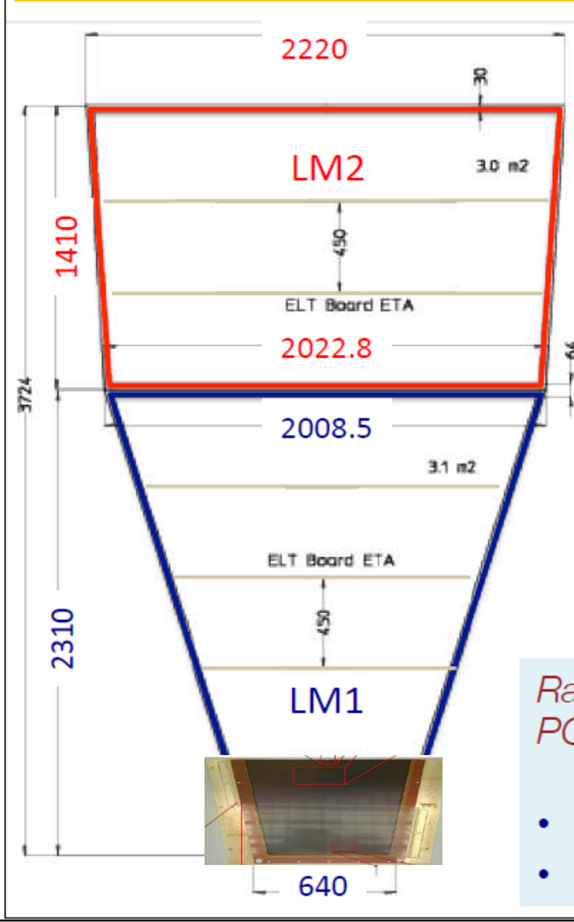


Micromegas Wedge Segmentation

Small sector modules



Large sector modules



Radial segmentation in 2 chambers per wedge

Construction Sites:

- SM1: Italy/INFN (Pavia, Rome1, Rome3, Frascati, Lecce, Cosenza, Napoli)
- SM2: Germany – Munich, Freiburg, Wurzburg, Mainz
- LM1: Saclay
- LM2: Thessaloniki + Dubna (+ CERN)

Radial segmentation of R/O PCB per plane

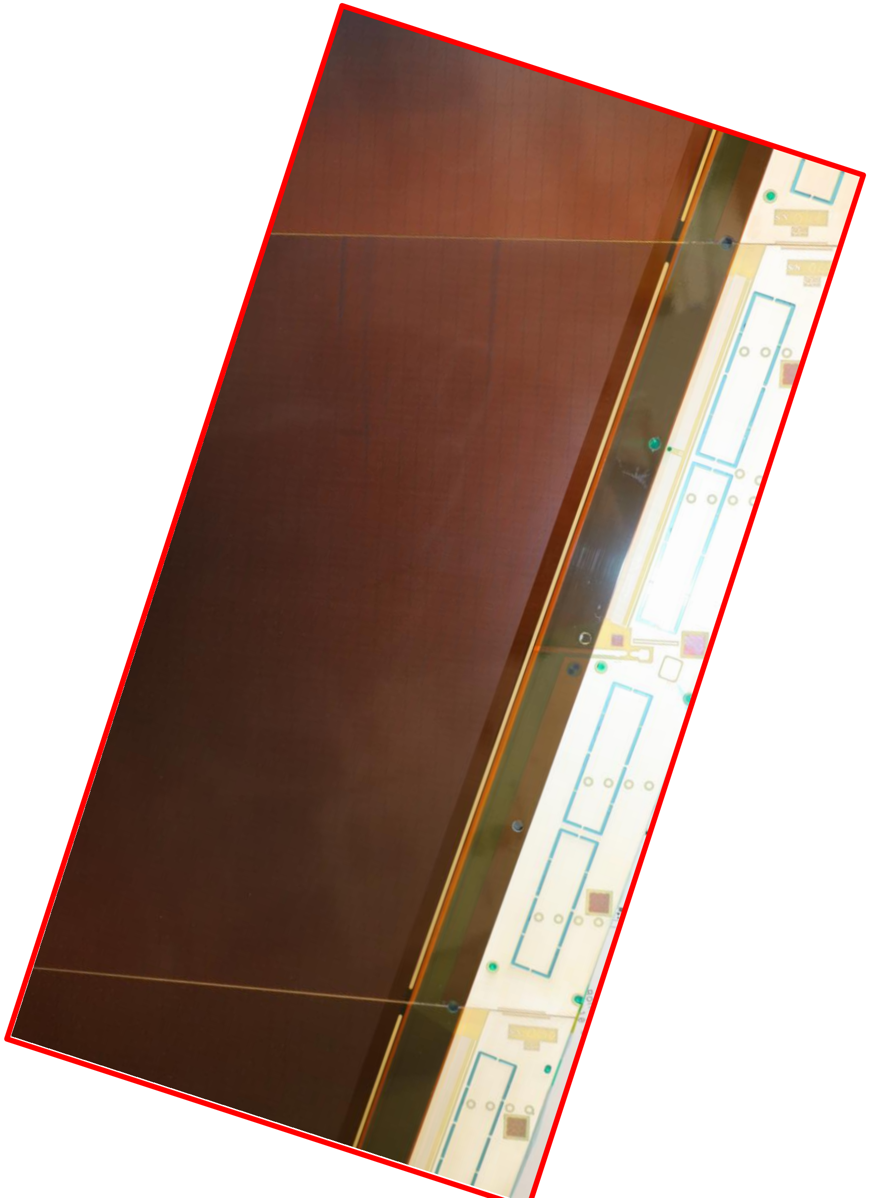
- SM1 and LM1: 5 PCBs
- SM2 and LM2: 3 PCBs

5 or 3 PCB/ plane of det.

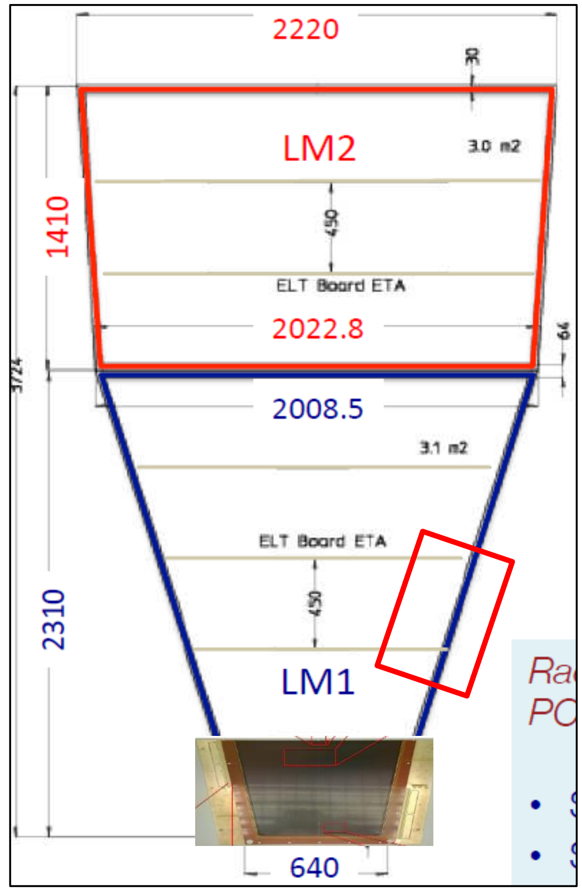
each PCB has 1000 strips (pitch 450 μm)

Resistive foils have been produced in Japan (production already done)

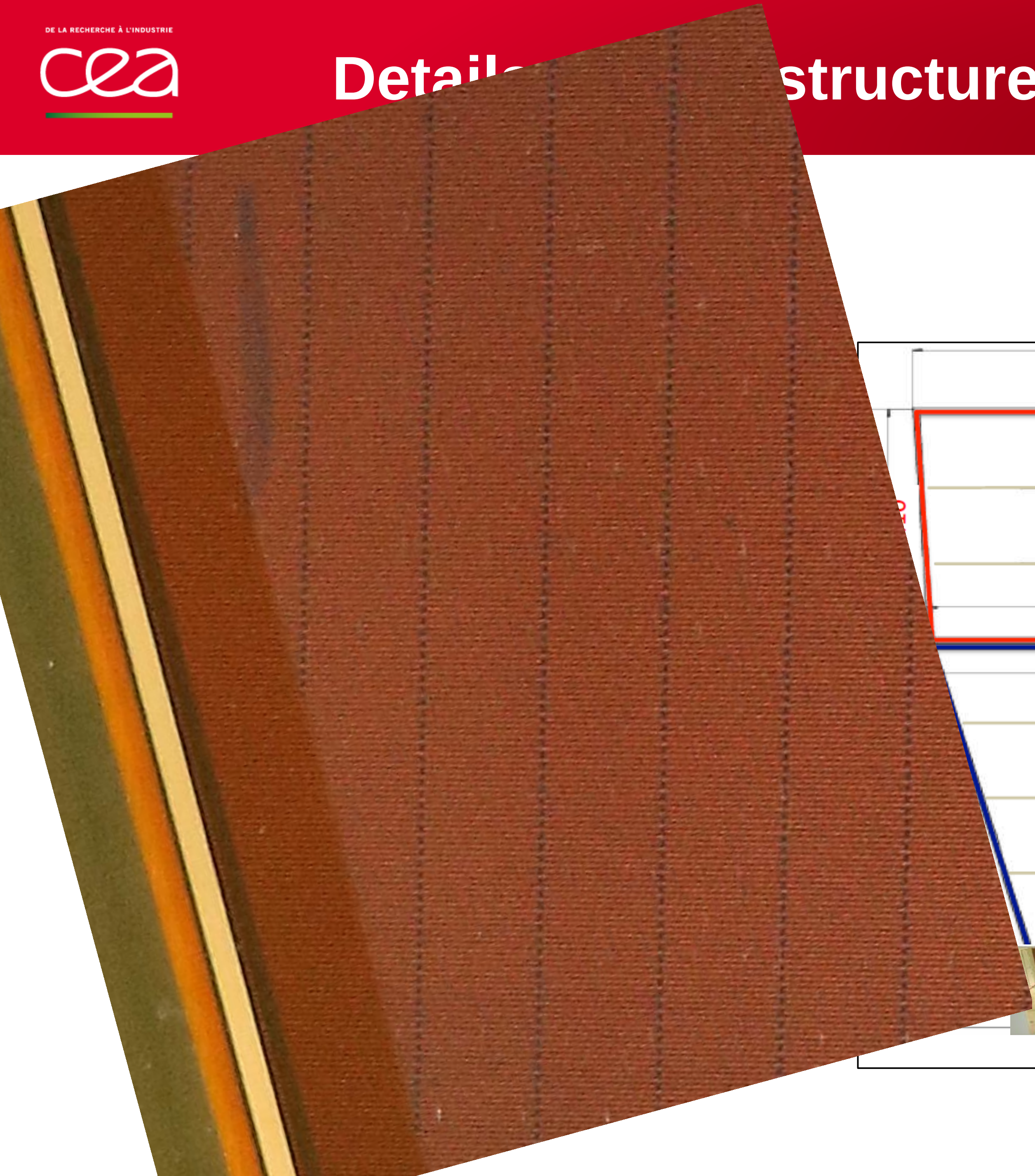
Details of PCB structure



Strips length from ~50 to ~200 cm
Width ~320 microns
Pitch 450 microns



Detai[illegible] structure



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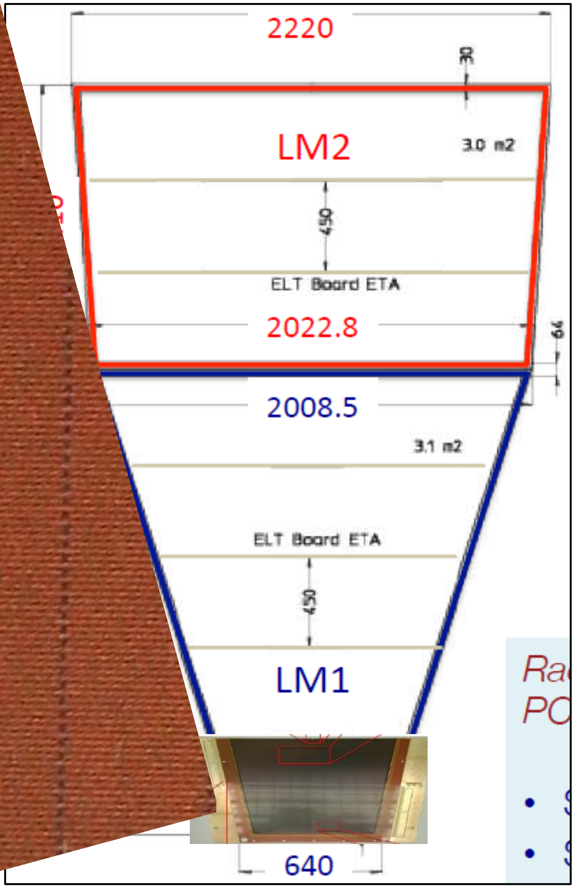
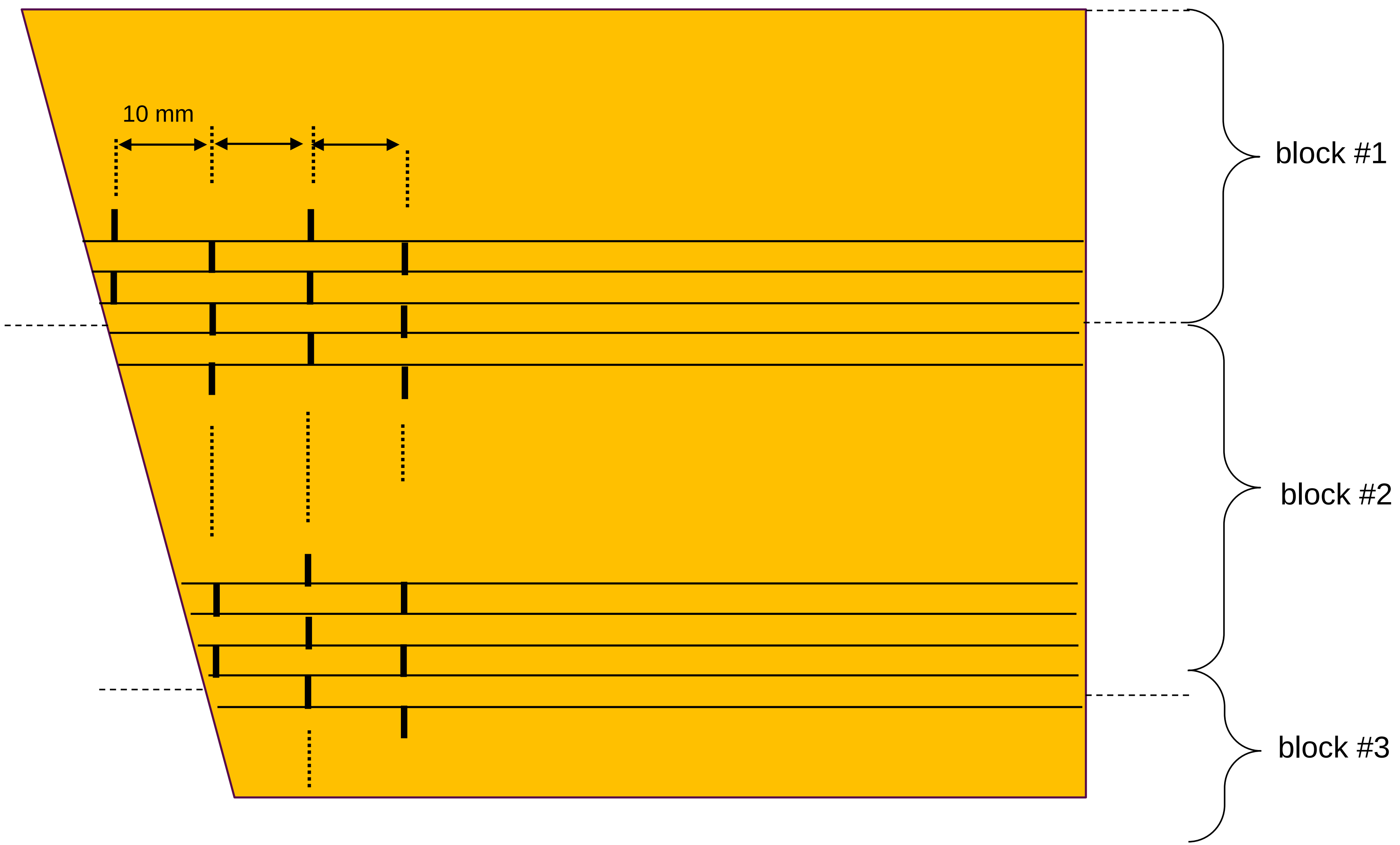


Resistive strips are on top of each copper strips

Strips connexion each 10 mm
One shifted w.r.t. the next.

Resistive layout



Readout Board Production

I. photolithographic creation of copper pattern
standard process.
complex due to: size of board, required precision & board elongation (humidity).

II. cutting of Kapton foil with resistive pattern
non-standard but simple & required accuracy only ±1mm

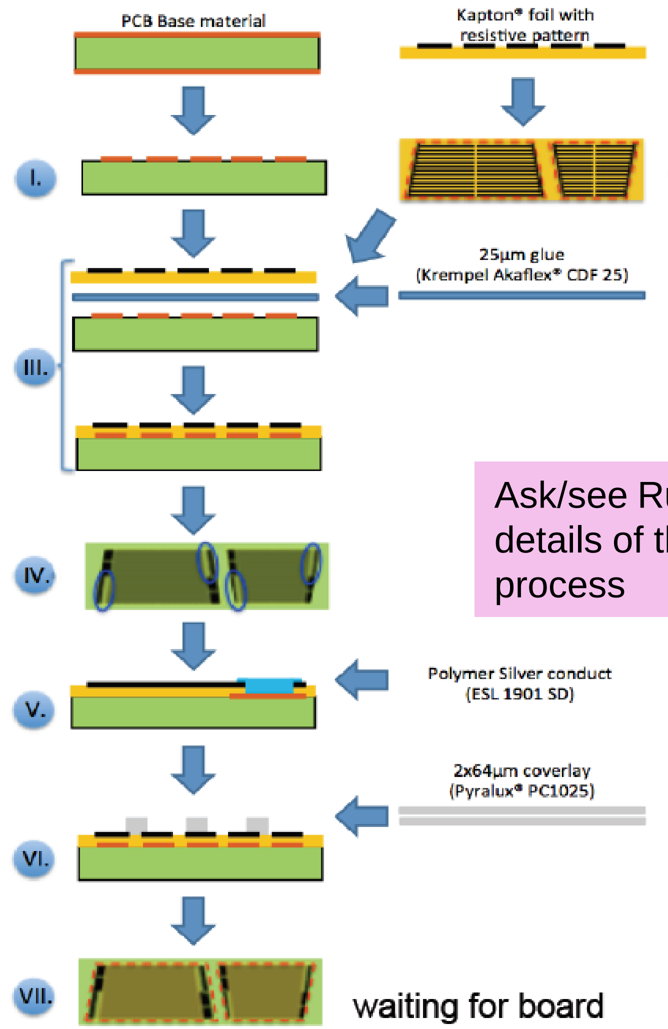
III. stacking and high-pressure & temperature gluing of Kapton foil, glue foil and board
standard process for small boards
complex due to: size of board & required cleanliness.

IV. chemical silver plating of copper pads
standard process

V. screen-printing of silver paste
non-standard but rather simple & required accuracy only ± 1mm

VI. lamination of coverlay & pillar creation
standard process for small boards.
complex due to: size of boards, highly non-standard pattern, required flatness

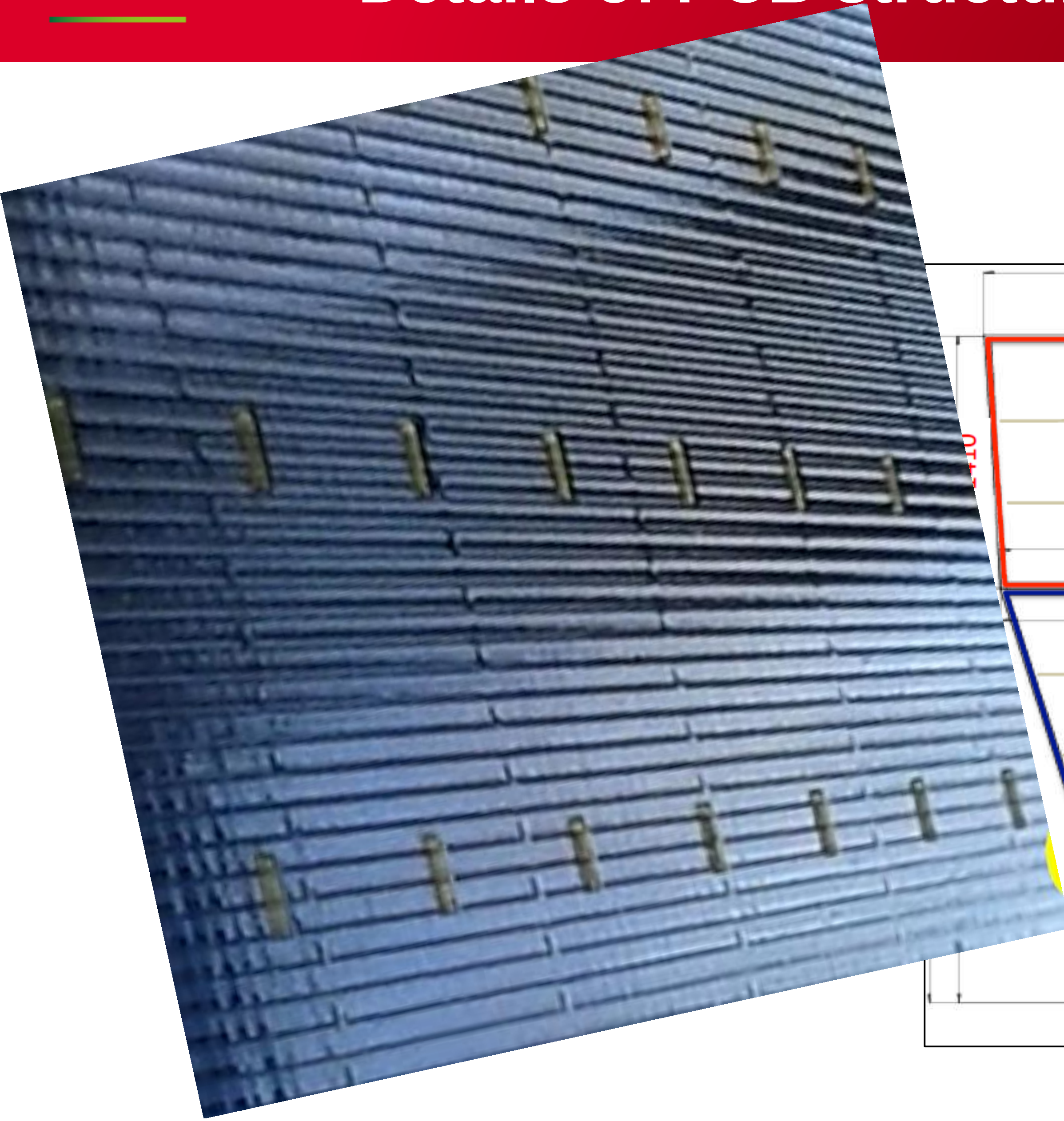
VII. cutting of boards and drilling of non-precision holes
standard process on CNC machine.
complex due to size of boards, required cutting precision & board elongation (humidity).

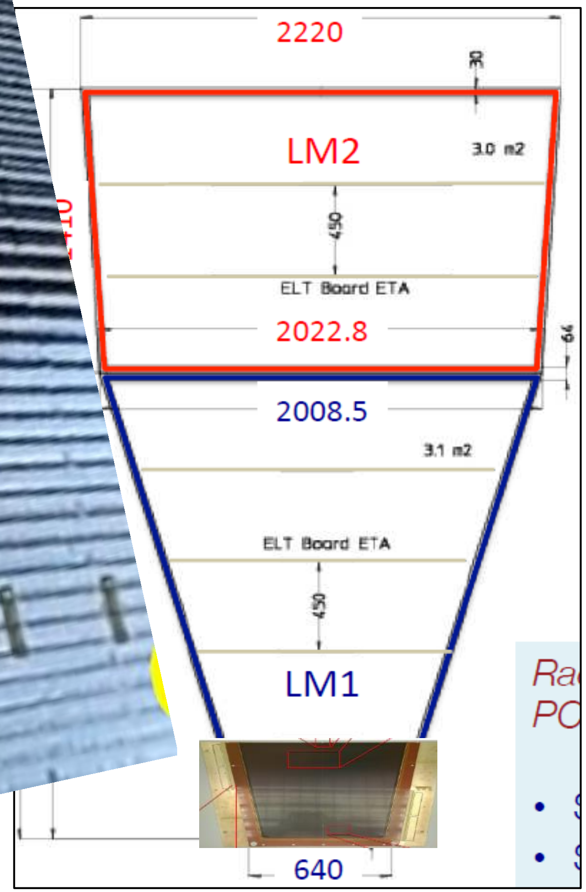


Ask/see Rui for more details of the production process

waiting for board expansion (>20 days)

Details of PCB structure





<u>Resistive area :</u>

Resistive strips are made with some resistive paste, deposited on top of a Kapton foil.

It is glued on top of the RO PCB (having the RO strips)

R foils have been made in Japan (KOBE et al. and industry)

<u>For our simulation we assume :</u>

R = 1 M-Ohm / mm

If some variations, one may interprete results in % of a reference value…

Some historical remarks on previous / these calculations

<u>2012:</u> First calculation made in Frascati-INFN, B.Ponzio and S.Franchino

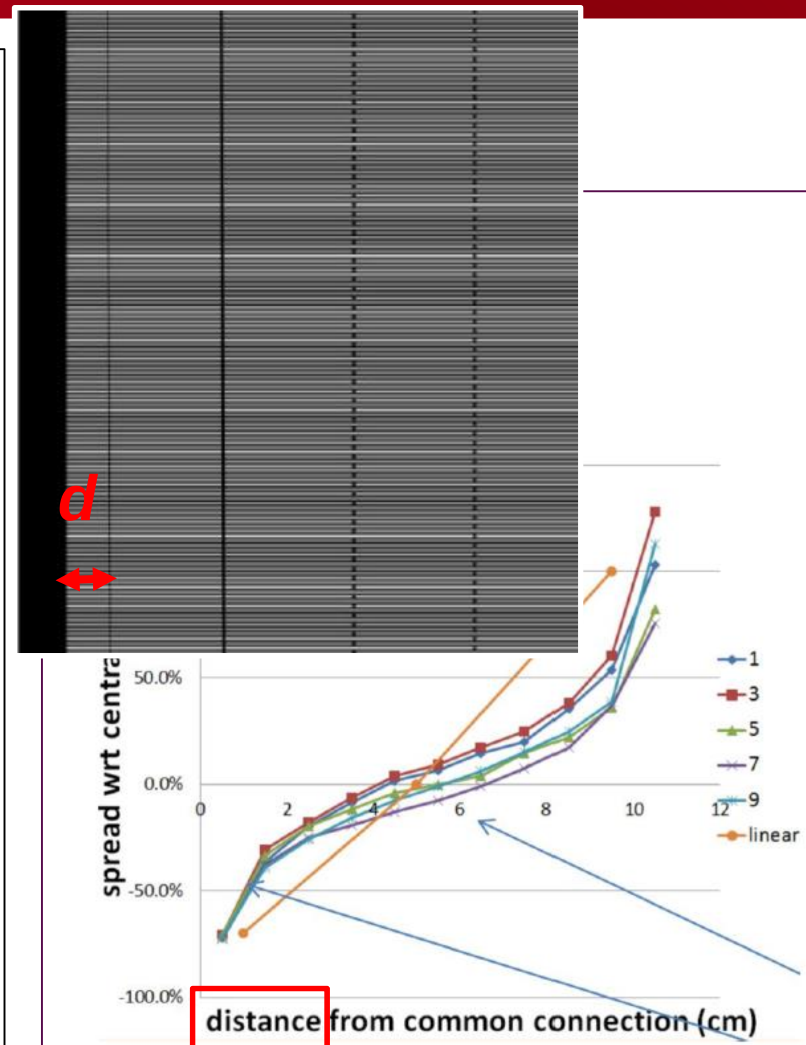
If distance "*d*" of minimum approach of first resistive interconnexion between resistive strips is too close to the HV silver line, then, close to the edge, the equivalent strip resistance decreases.

=> <u>passivation in industry (ELVIA and ELTOS) by ~10 mm</u>

<u>Beg. of 2019:</u> E.Delagne (CEA Paris - Saclay)

CADENCE simulation using an "elementary cell" based on a two (short-) strips layout having some strips-connexion, and varying injection points / test points along the strip.
Hyp.: R <u>linear</u> with strip length, as 1 M-Ohm / mm.

=> <u>"arcade" shape of 10mm due to resistive connexion pitch</u>

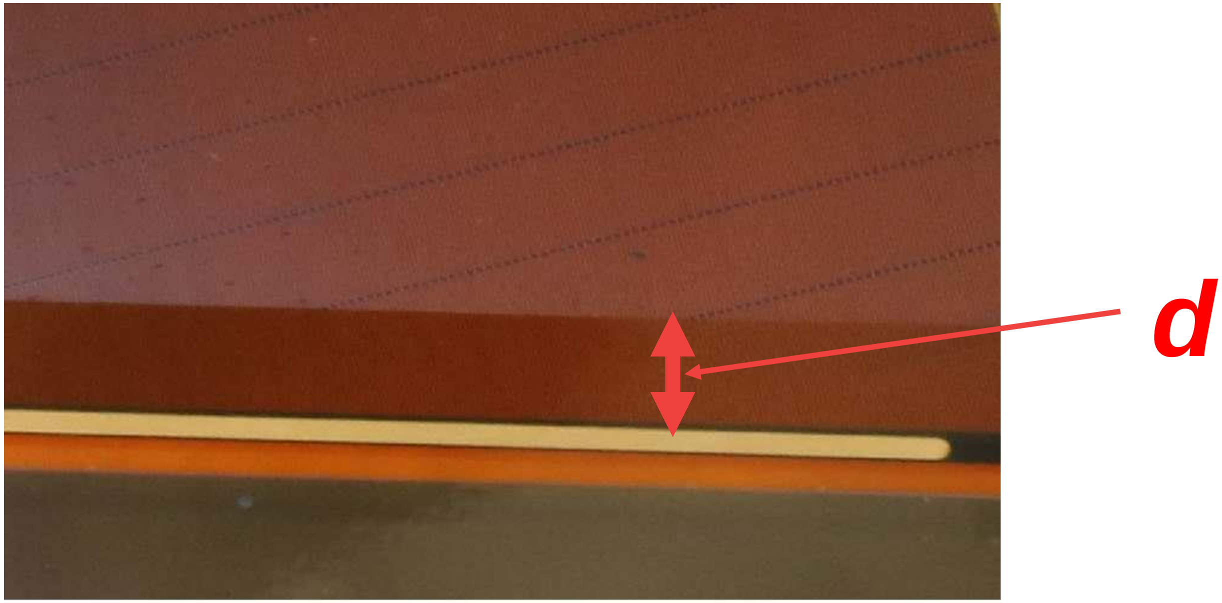


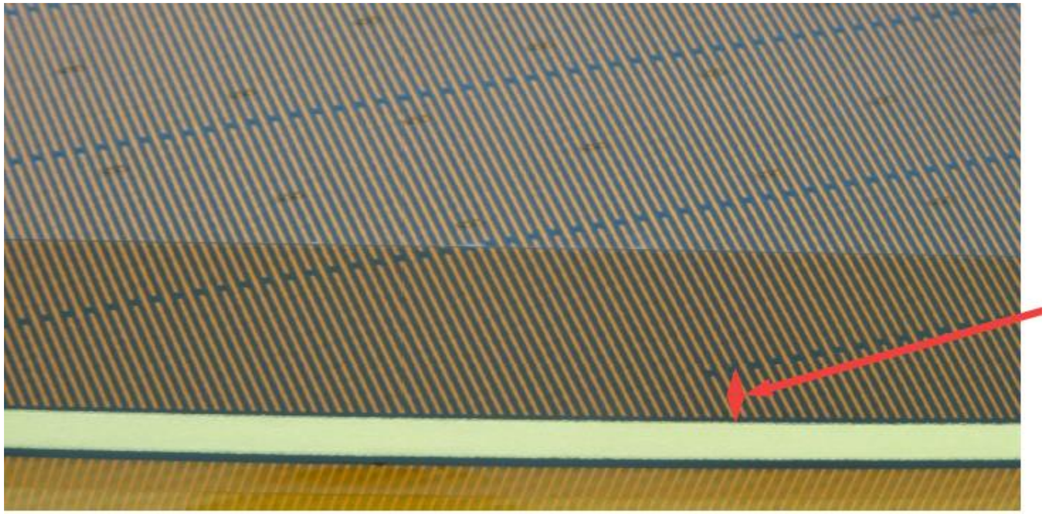
<u>Mid. 2019:</u> 2nd iteration in CEA (Th.Thavarajah, Ph.Schune *et al.*)

- Several cells to simulate trapezoidal shape
- Tests of different
    - R-connexion between strips
    - different strip length
    - different layout of R-connexion (i.e. different "*d*")

<u>Remind:</u> changing paste resistivity, is "equivalent" to re-scaled calculation.

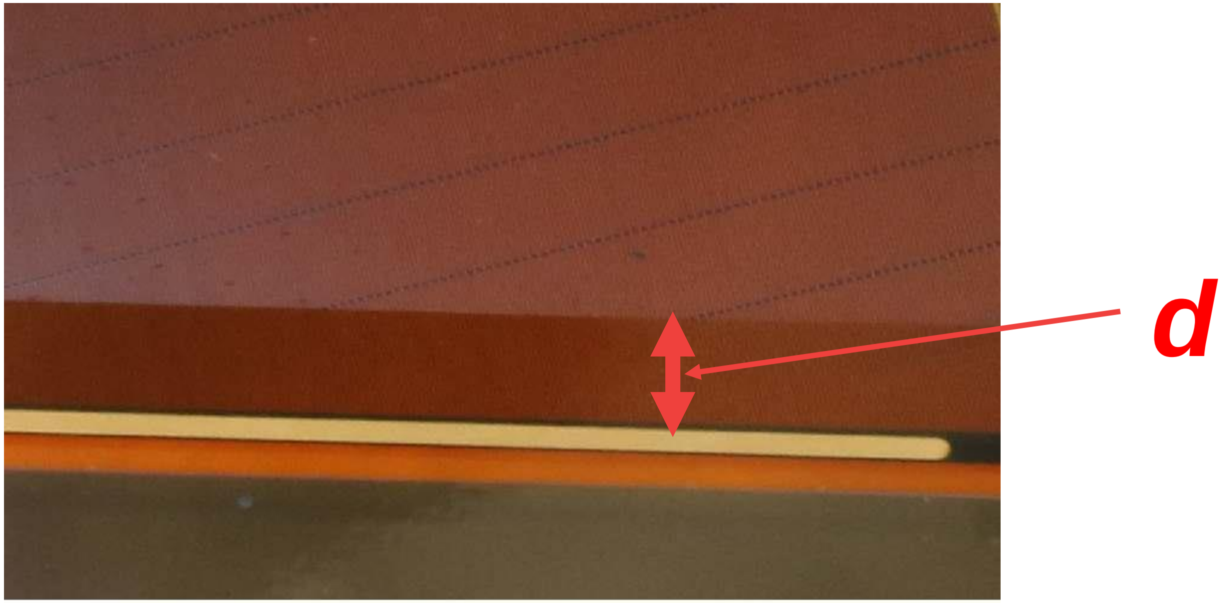
Several configuration, depending of the MM – NSW chamber type, side, etc.

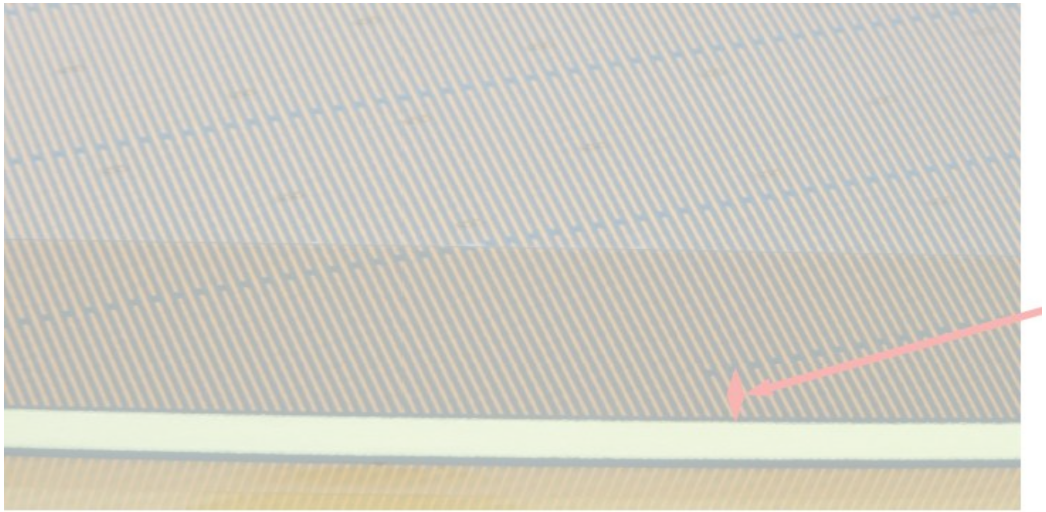




Pillars and side protection (“wall”) are made by Pyralux on top of the resistive layer.
2 x 64 microns.

In this simulation we assume that the start of the resistive connexion between strips, starts just after the **industry passivation**.



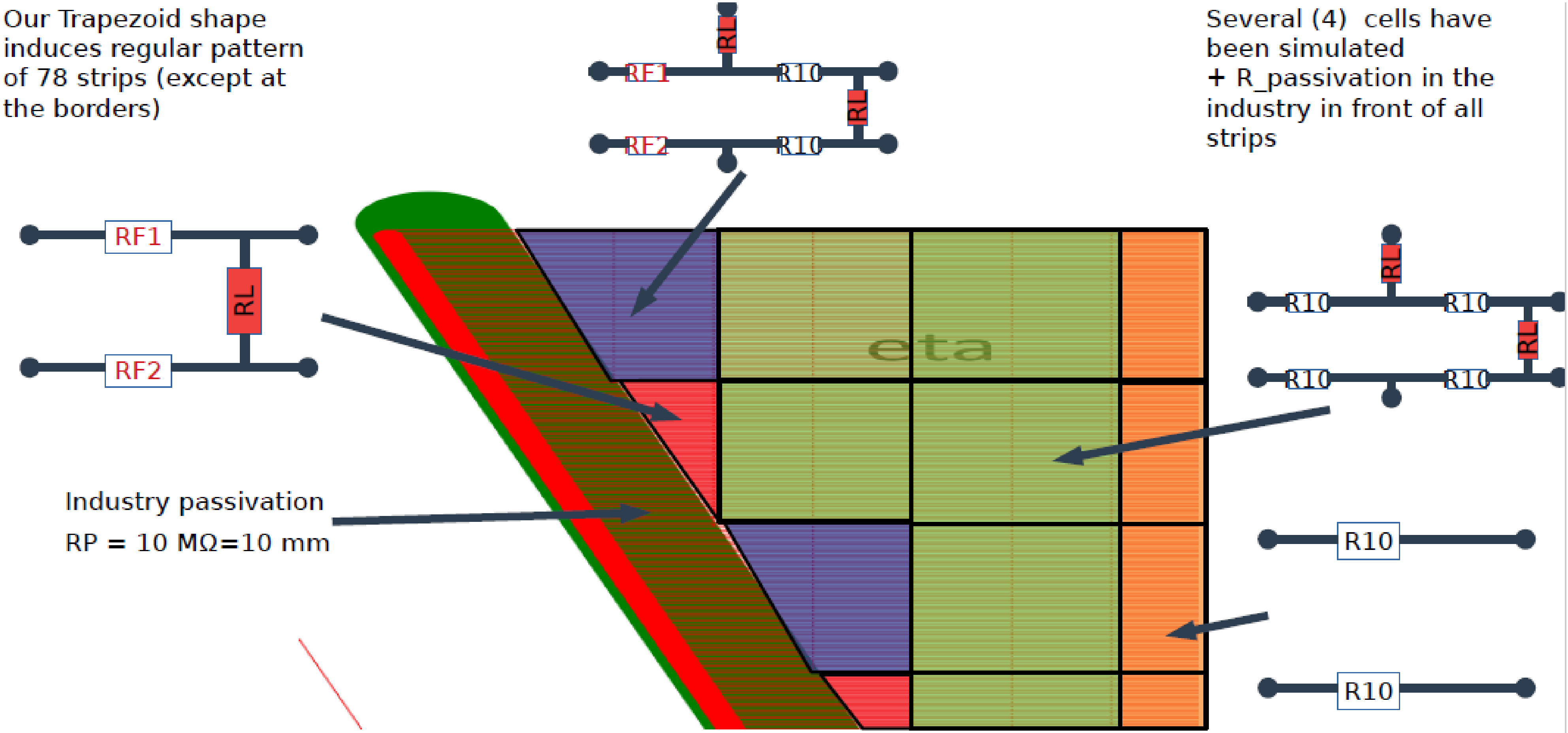


Pillars and side protection ("wall") are made by Pyralux on top of the resistive layer.
2 x 64 microns.

Several cells simulated

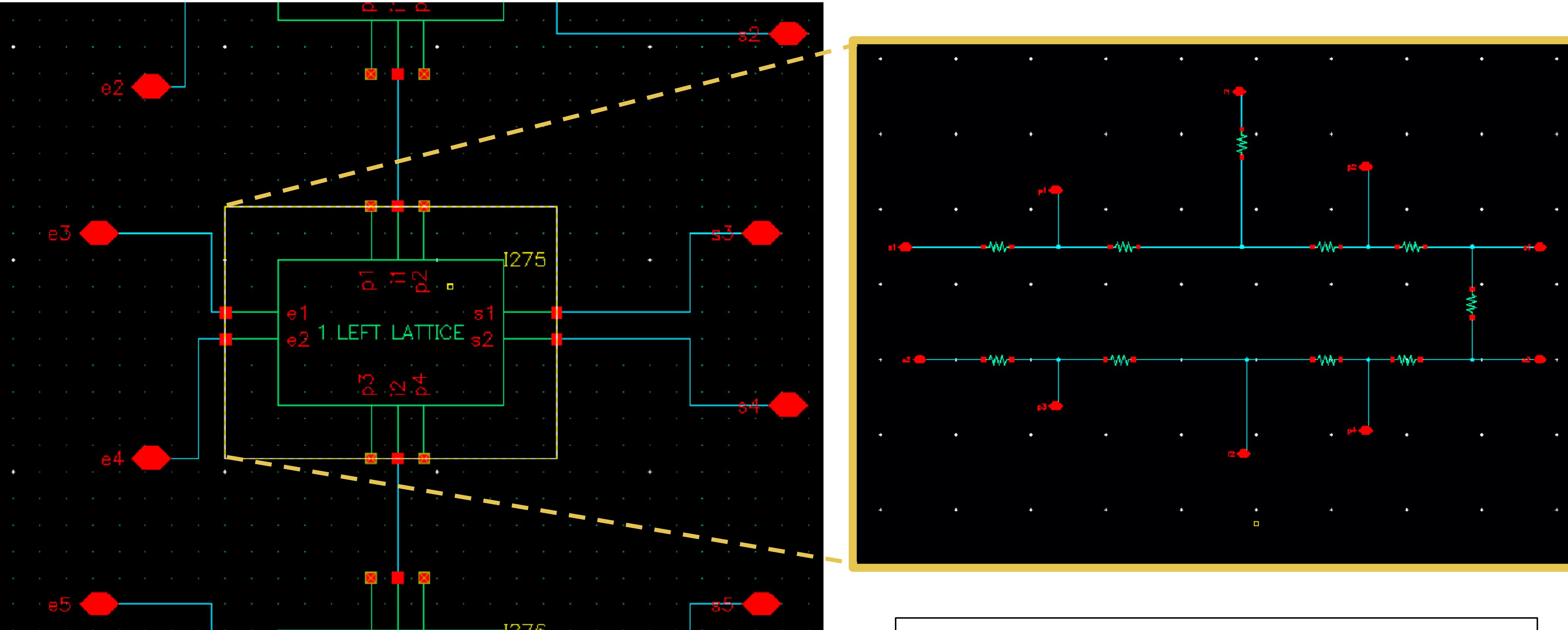
Our Trapezoid shape induces regular pattern of 78 strips (except at the borders)

Several (4) cells have been simulated
+ R_passivation in the industry in front of all strips



R10 =10MΩ

Single cell detail



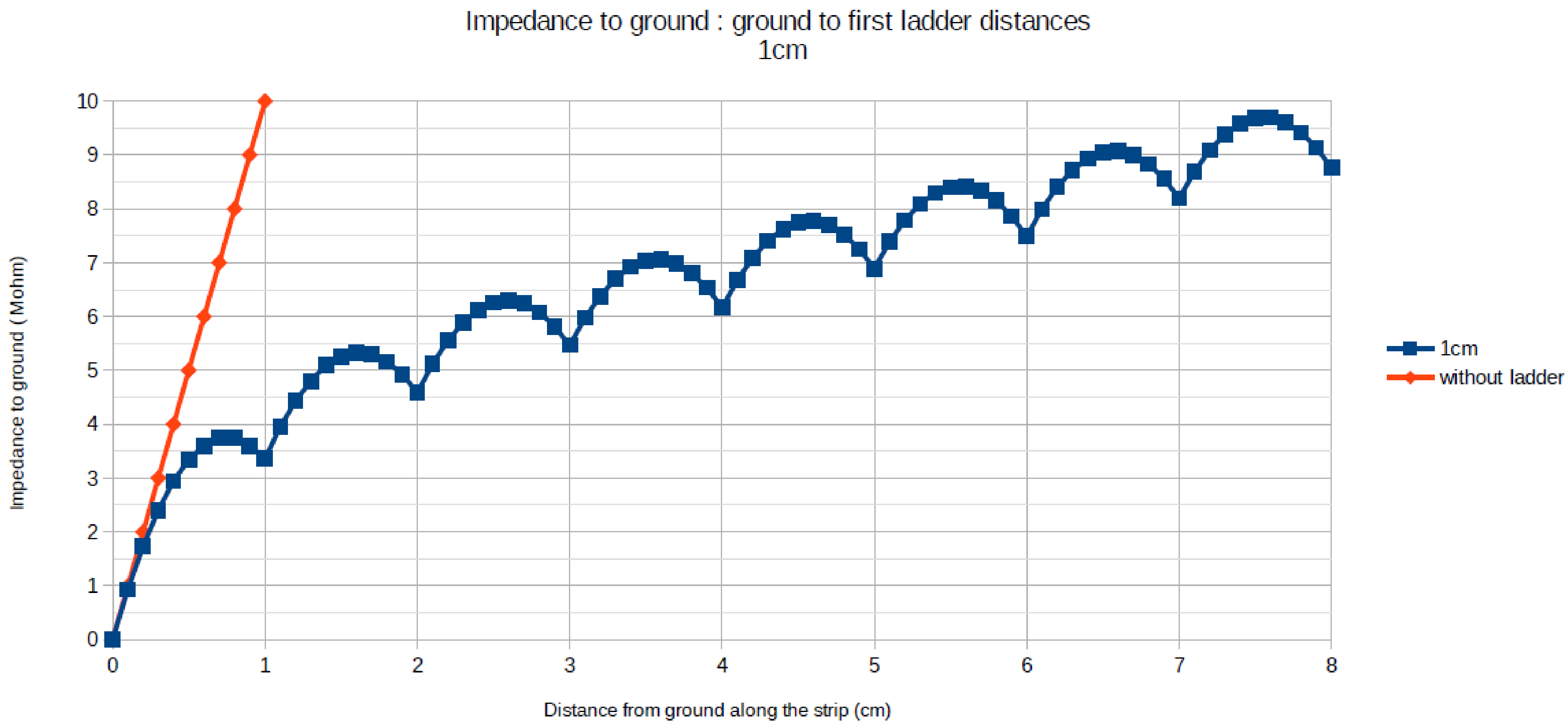
(elementary cell from E.Delagne, beg. 2019)

<u>CADENCE simulation :</u>

- Some **test points** where we inject a known current and where we measure V
- One can do this in each cell, one after the other

Some CADENCE results along a strip

Without connexions between strips : R-eq is simply 1 M-Ohm / mm, so linear with distance from strip origin



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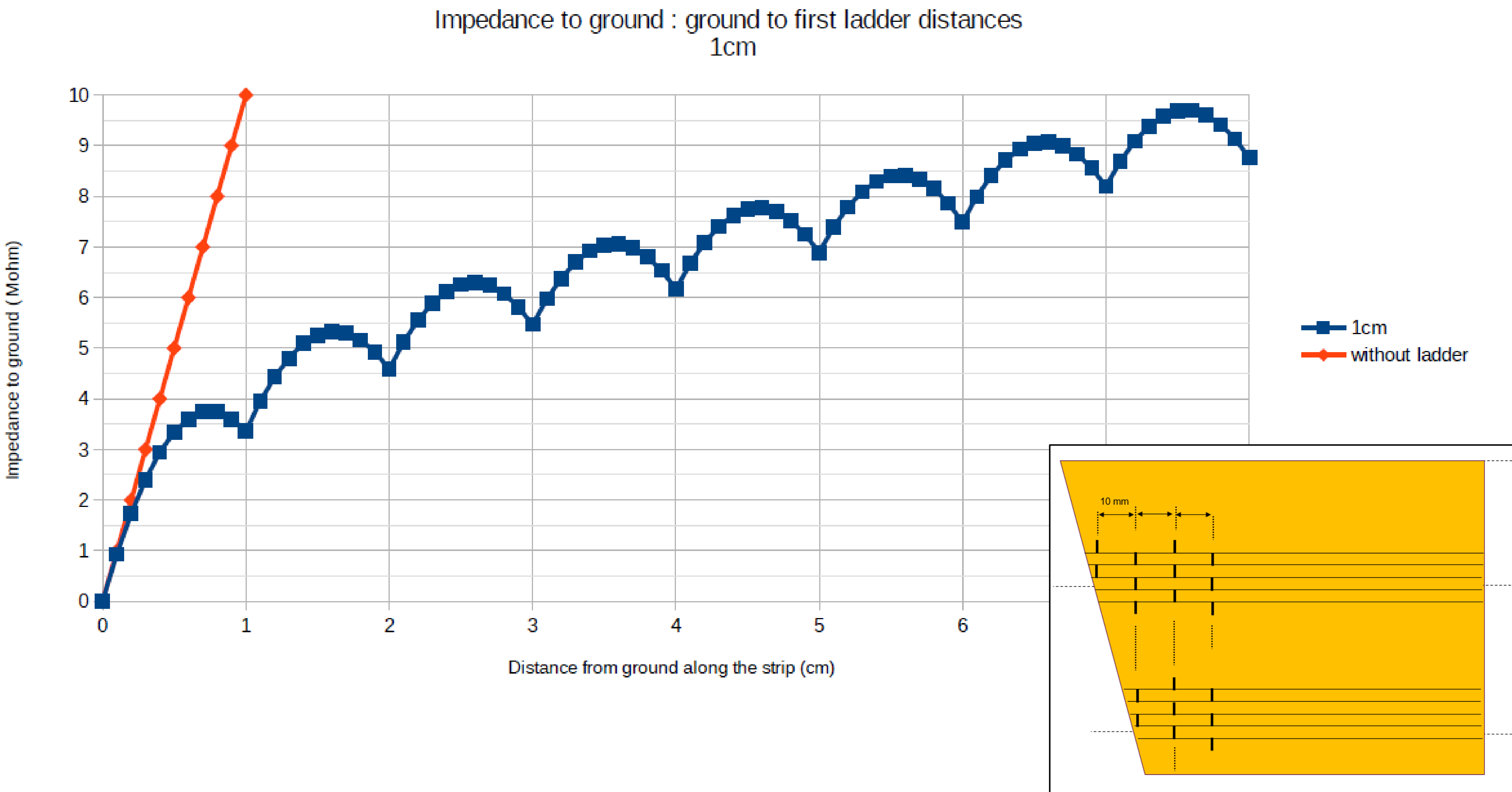
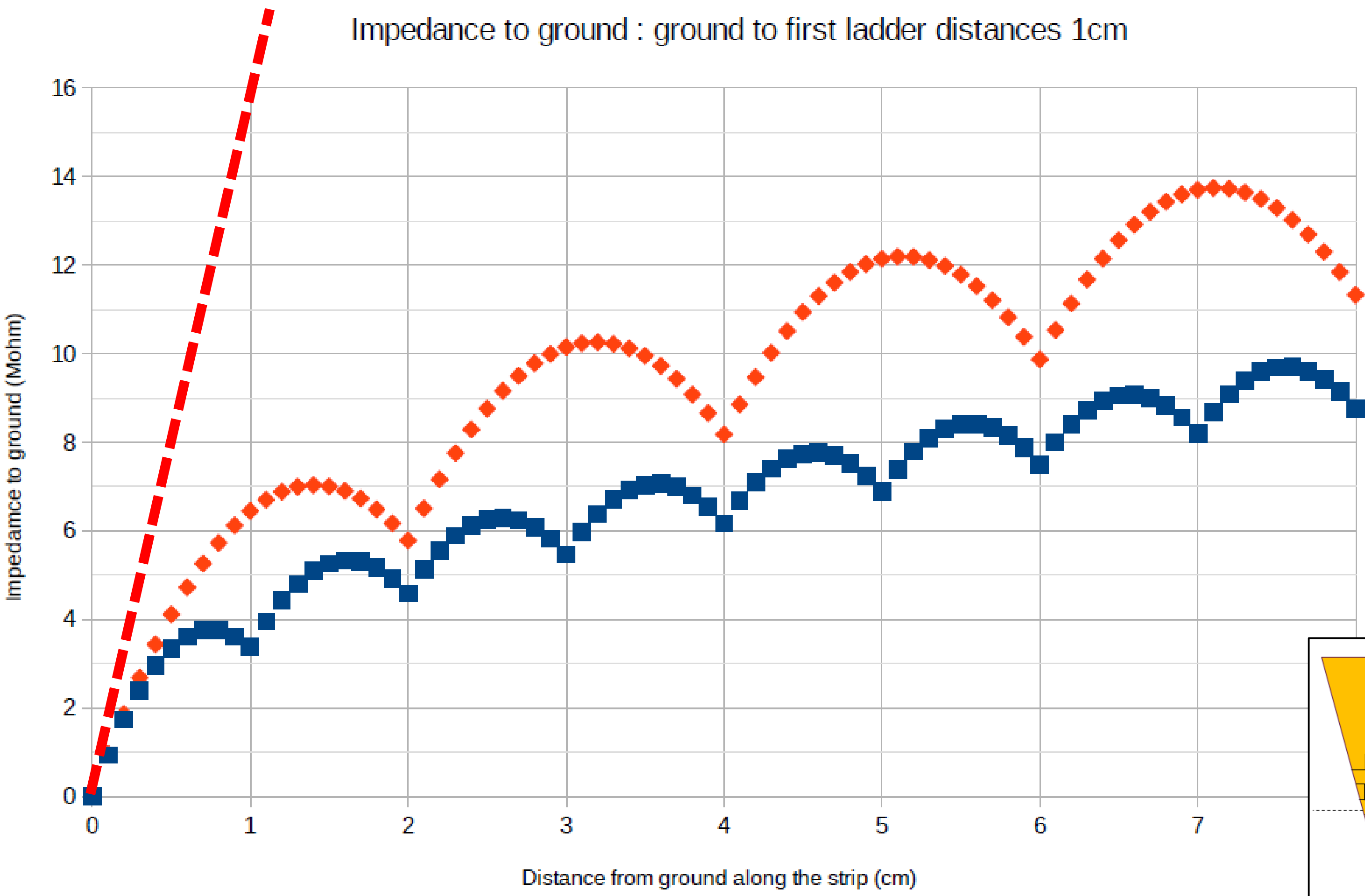
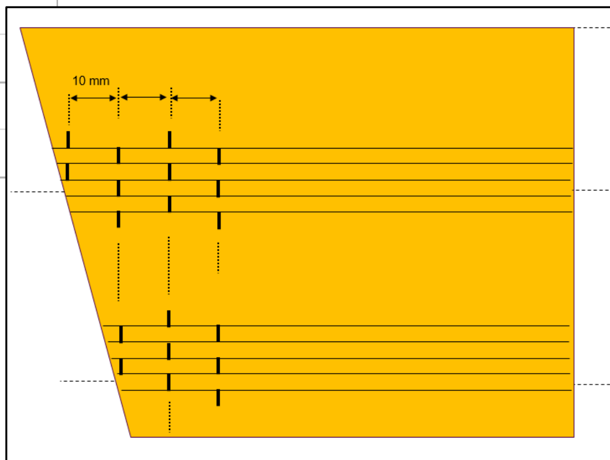
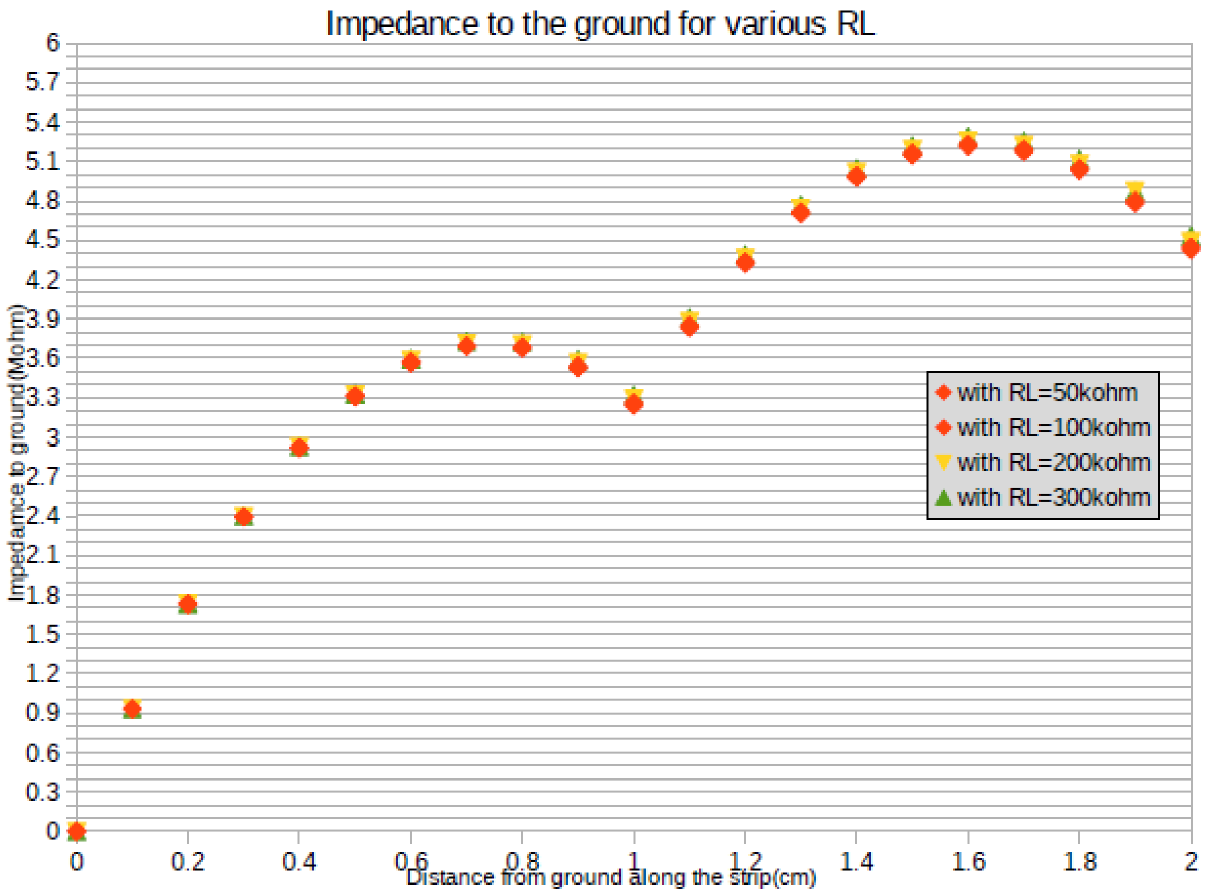


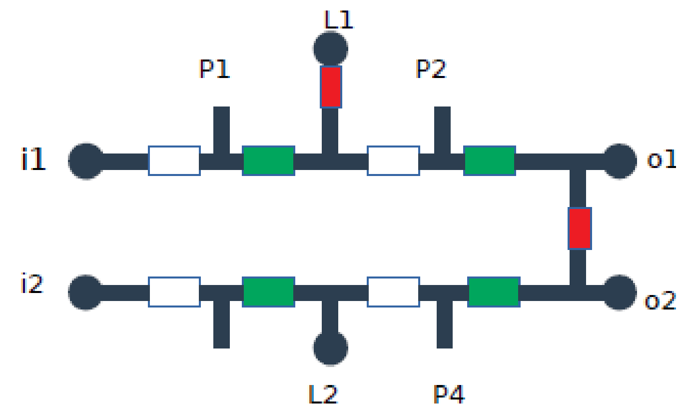


On the sides, one ladder over two only



Variation of R-eq with the resistance between strips

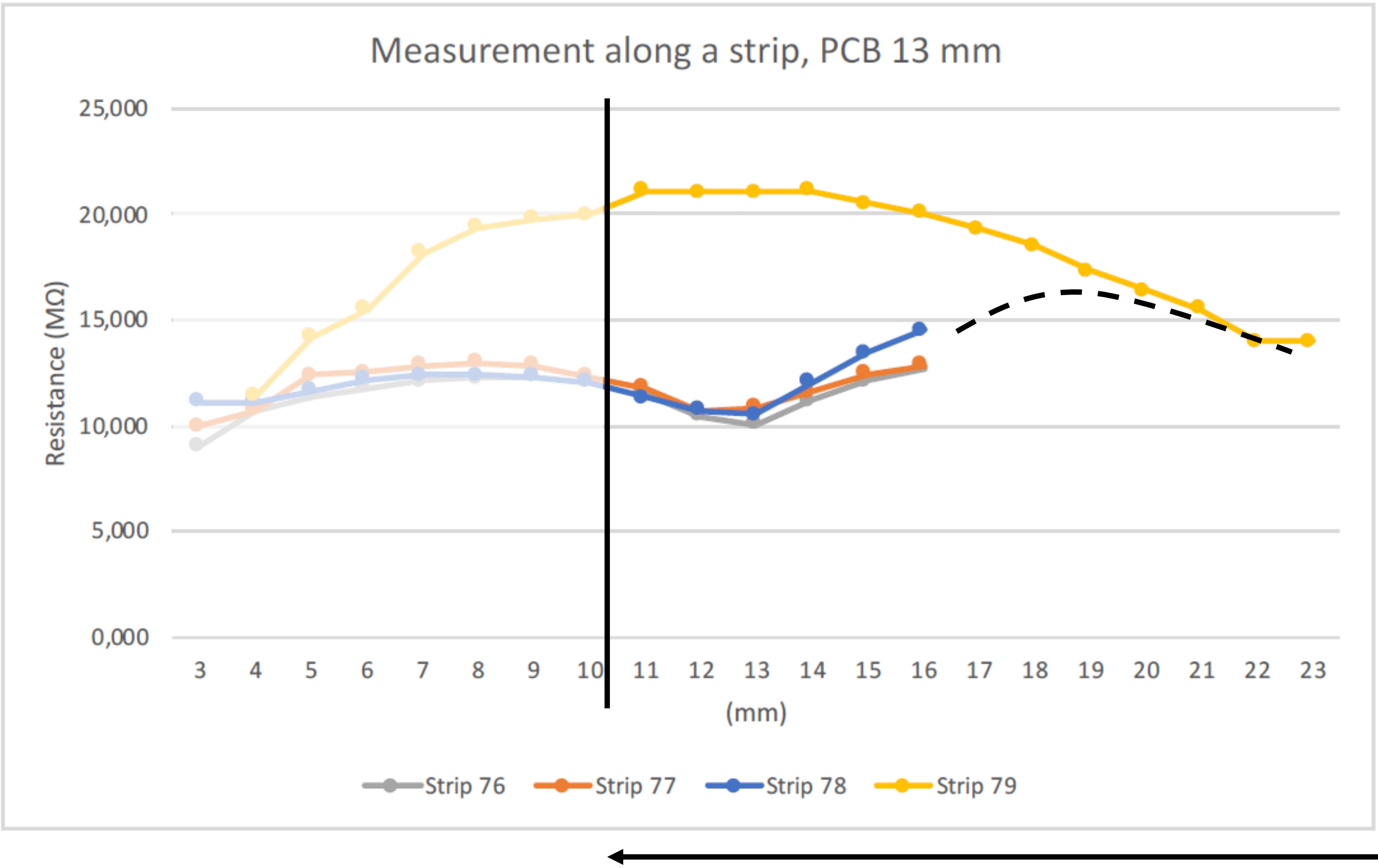




Measurements (on pre-serie NSW PCB)

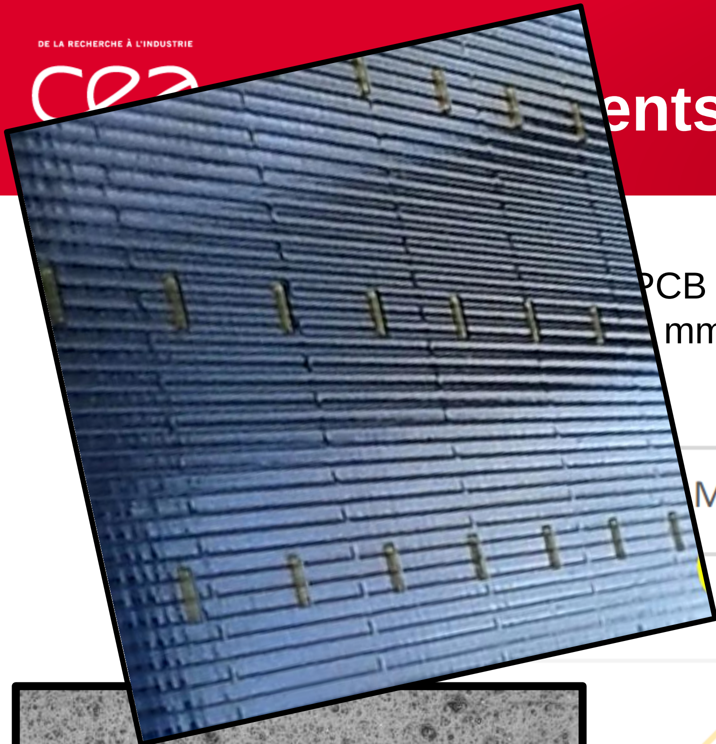
Measurements done on a PCB (type # 2) of LM1 type, from Module – 0 serie.
Industrial passivation was 3 mm only (ie an area with no signal)

<u>Measurements error :</u>
~+/- 10 % (at least)



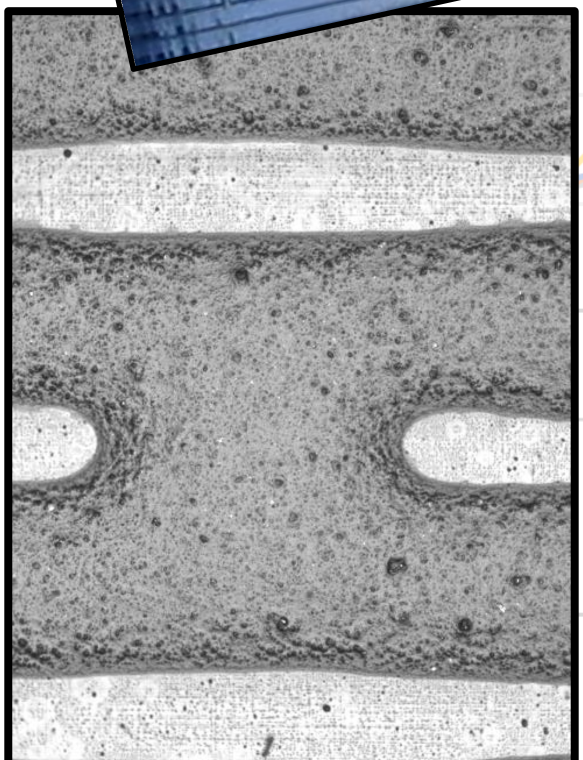
Accessible area in PCB of the production detectors

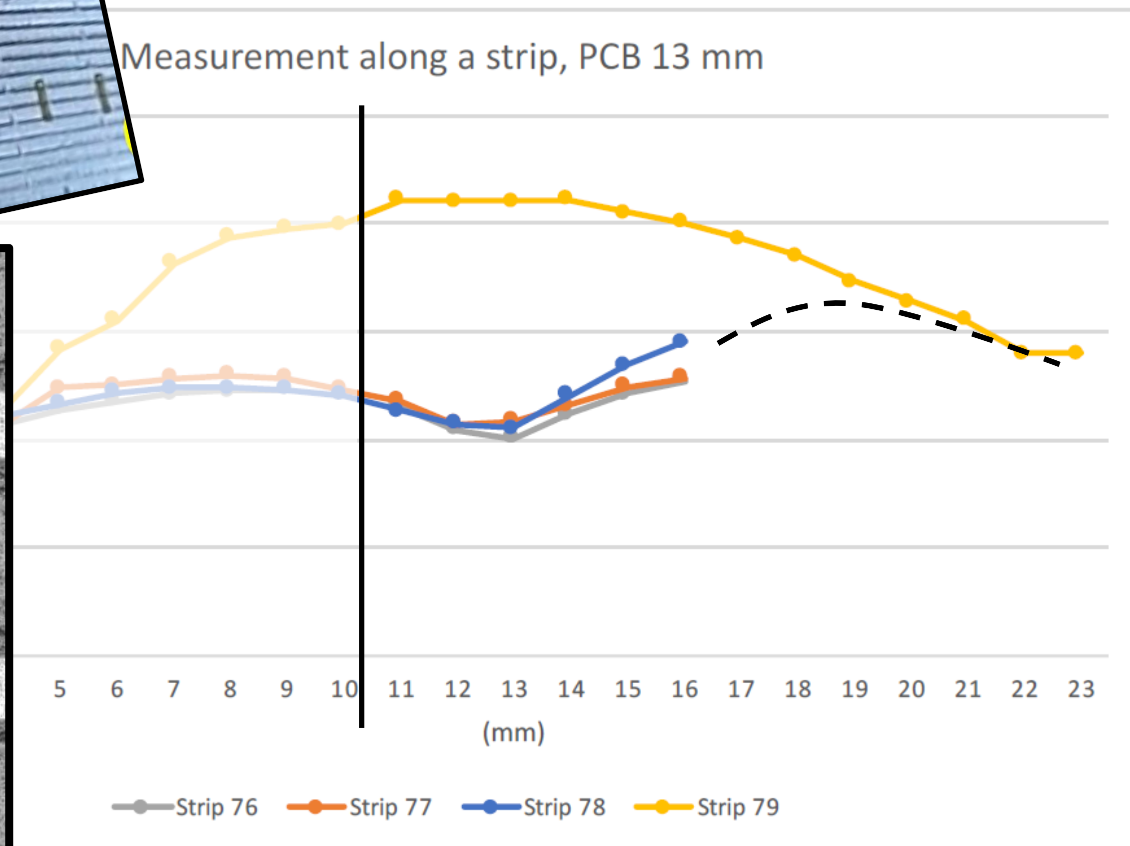
ents (on pre-serie NSW PCB)



PCB (type # 2) of LM1 type, from Module – 0 serie.
mm only.

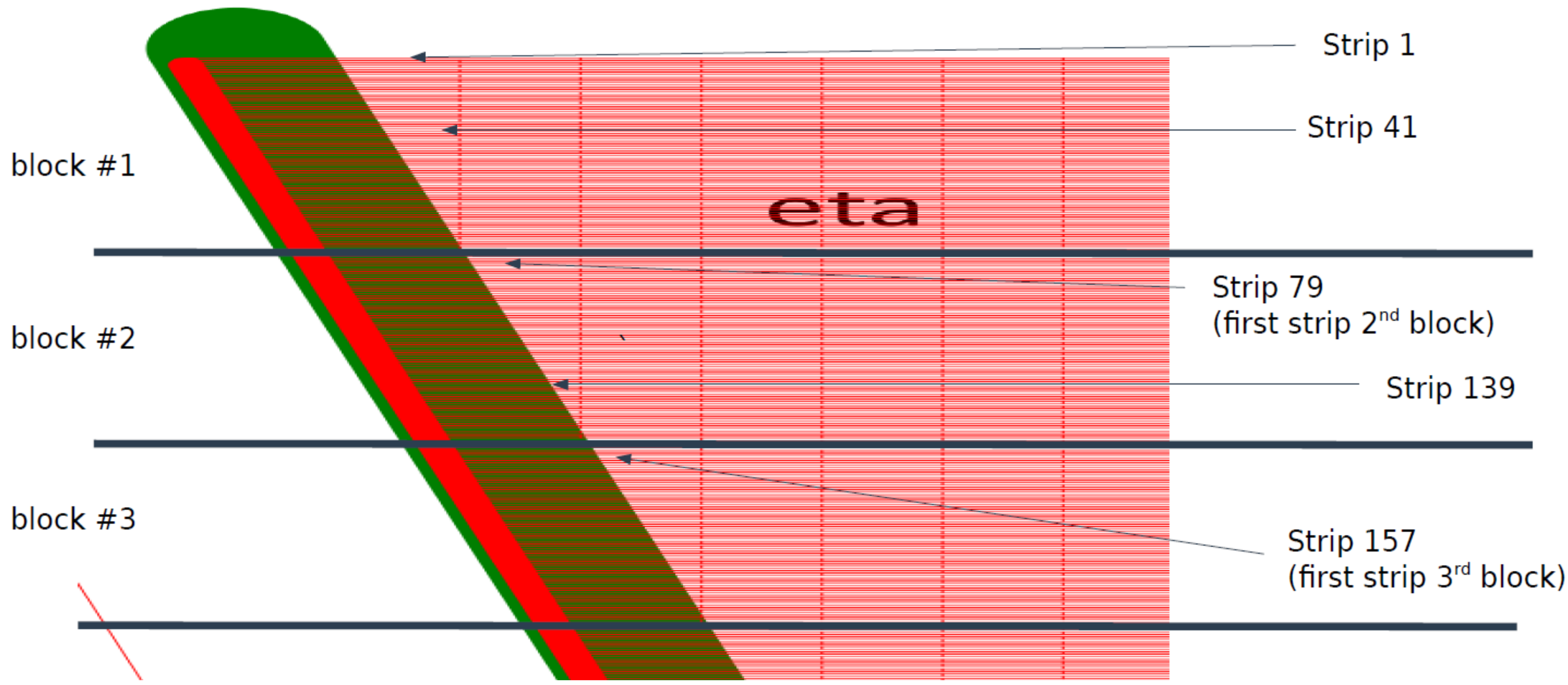
Measurements error :
~+/- 10 % (at least)





Accessible area in PCB of the production detectors

Different strips R-eq. calculated in CADENCE simulation



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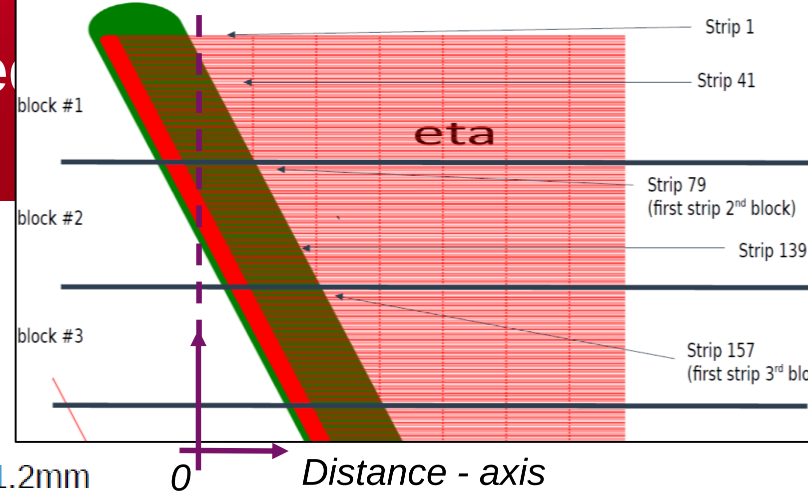
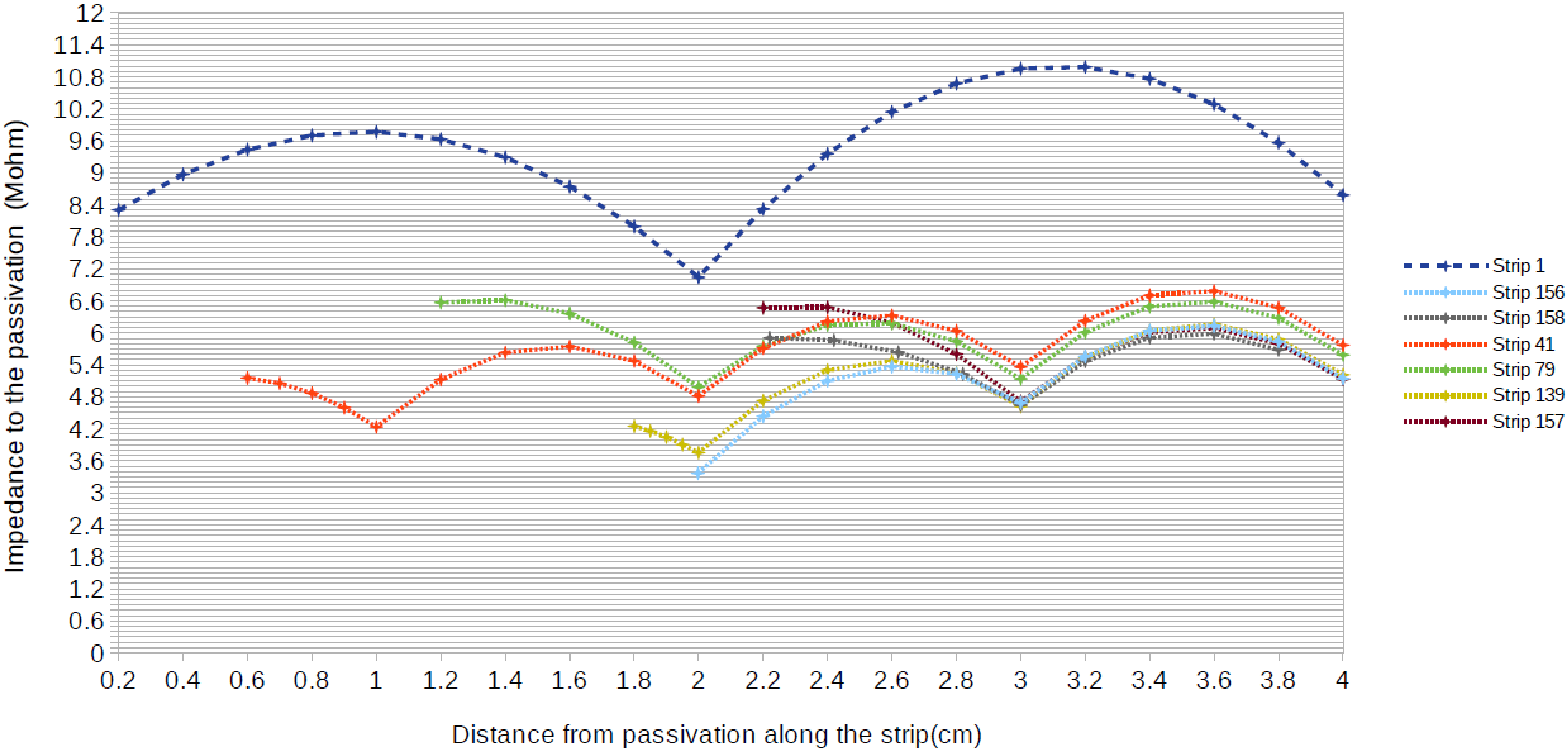


Trapezoidal shape of ETA pannel for 1010mm*421.2mm



Conclusions

- We developped a CADENCE program to calculate the R-equivalent of the ATLAS NSW Micromegas resistive layer
  (on top of the copper strips)

- We calculated some of the configurations corresponding to LM1 MM type
  (those built by CEA - Saclay)

<u>Future :</u>

We will calculate if some areas have some weakest R-eq value, due to the exact resistive layout

And compare to more measurements, on different types of NSW MM PCBs

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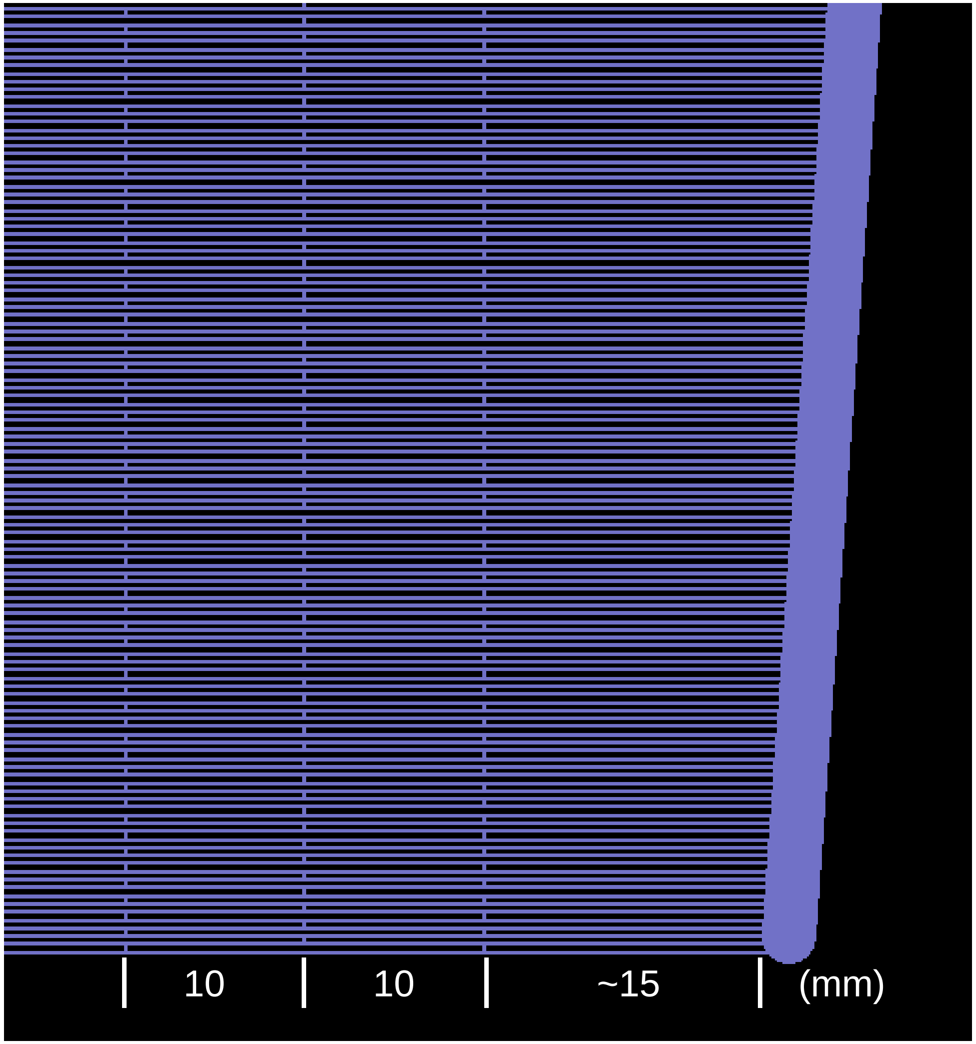
(CEA Paris – Saclay, DRF – IRFU)

spare

SM2 PCB type



LM2 type eta-8 board : closest distance of resistive interconnexion to silver line is ~15mm