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# SRS-BASED TIMEPIX3 READOUT

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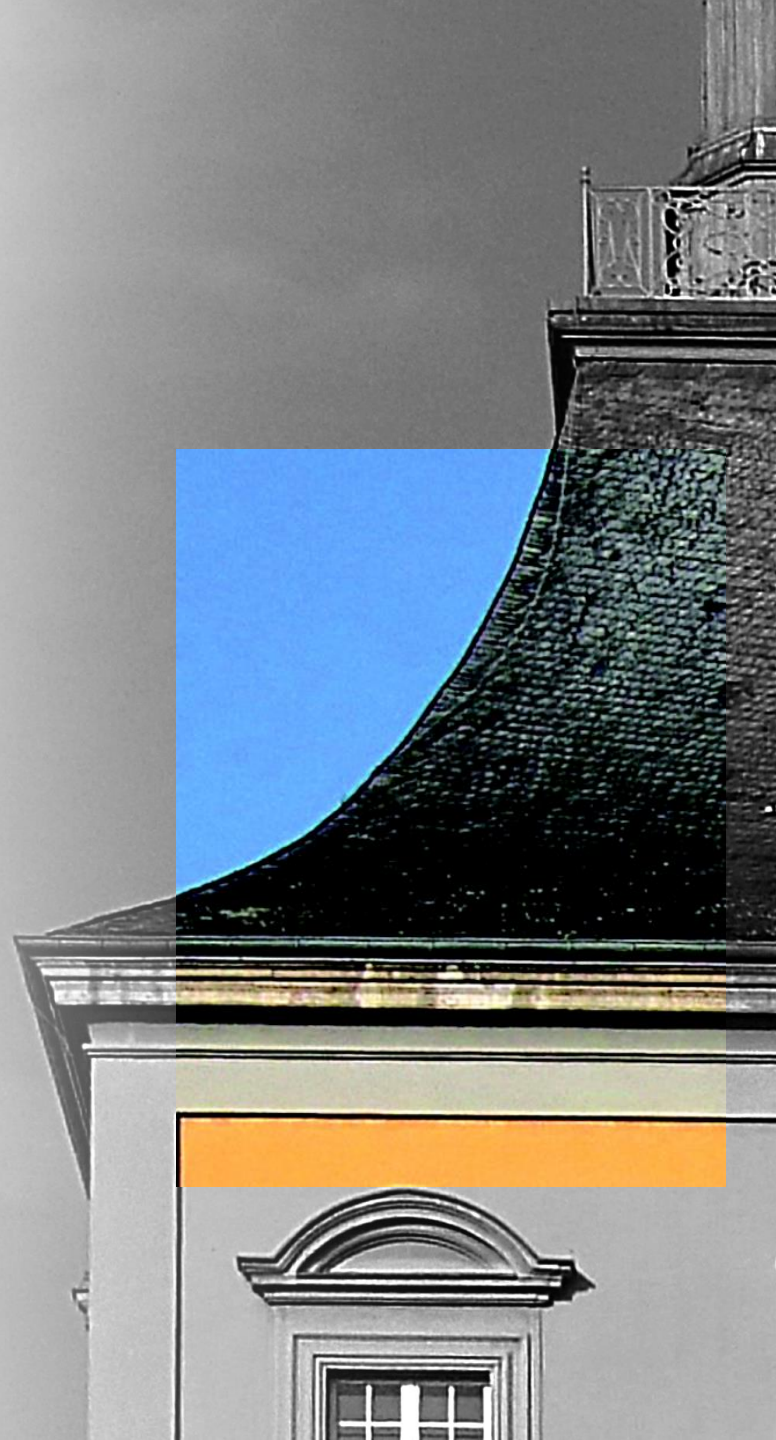
23.10.2019

RD51 collaboration meeting



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# KEY INFORMATION

- Hardware concept same as for Timepix@SRS
- Firmware written in Verilog
- Software written in Python
- Usage of the basil framework
- Open source (GPL-3.0 license)
- Usage of a continuous integration pipeline for testing

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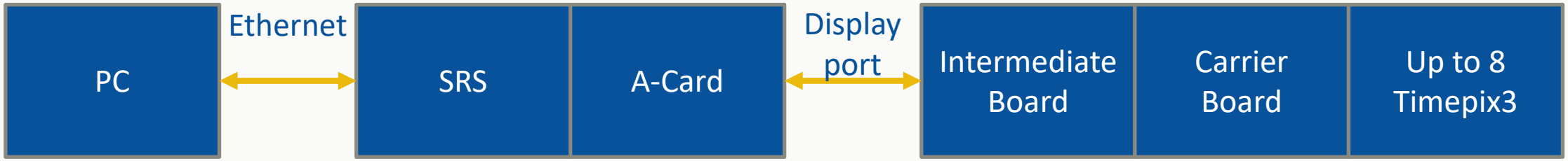
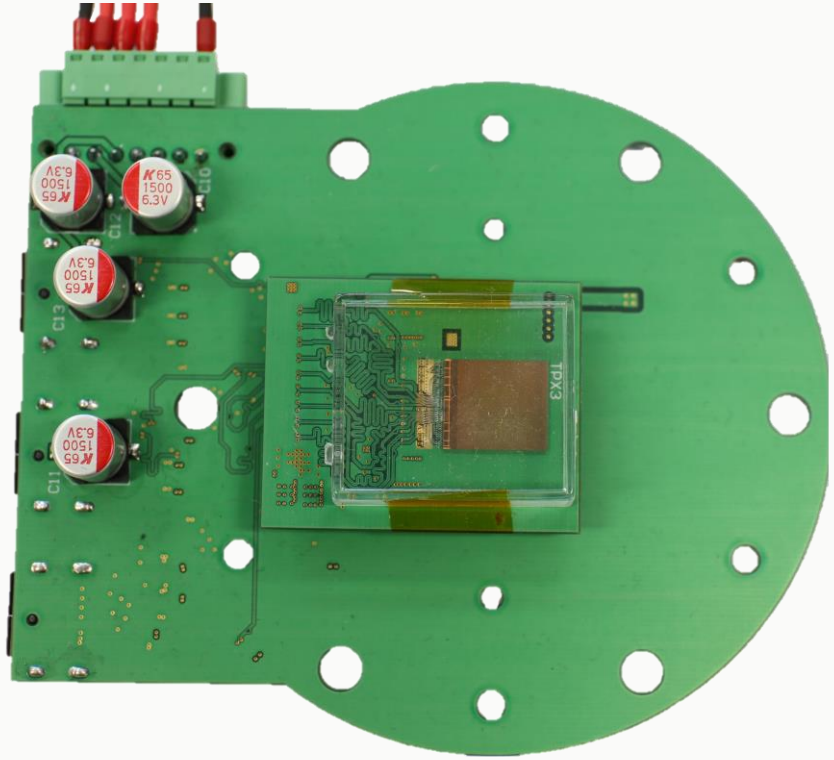
# HARDWARE AND SOFTWARE

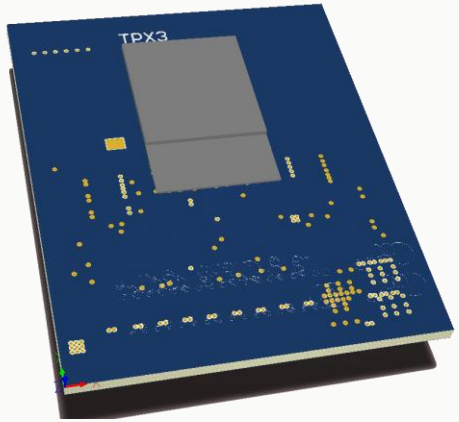
# HARDWARE CONCEPT



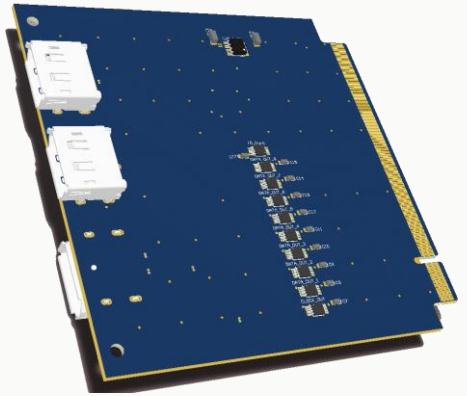
# HARDWARE




Intermediate board with chip carrier and Timepix3




Chip carrier



Adapter card

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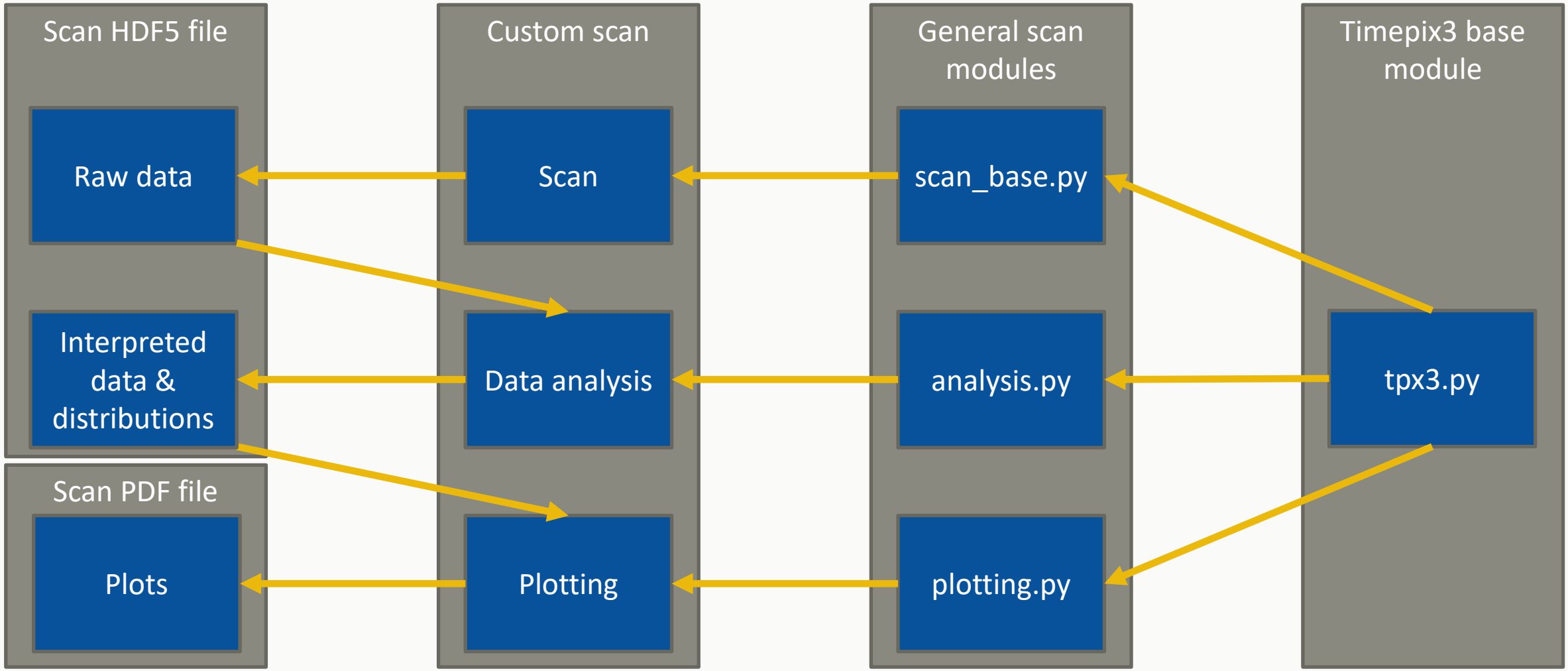
# SOFTWARE

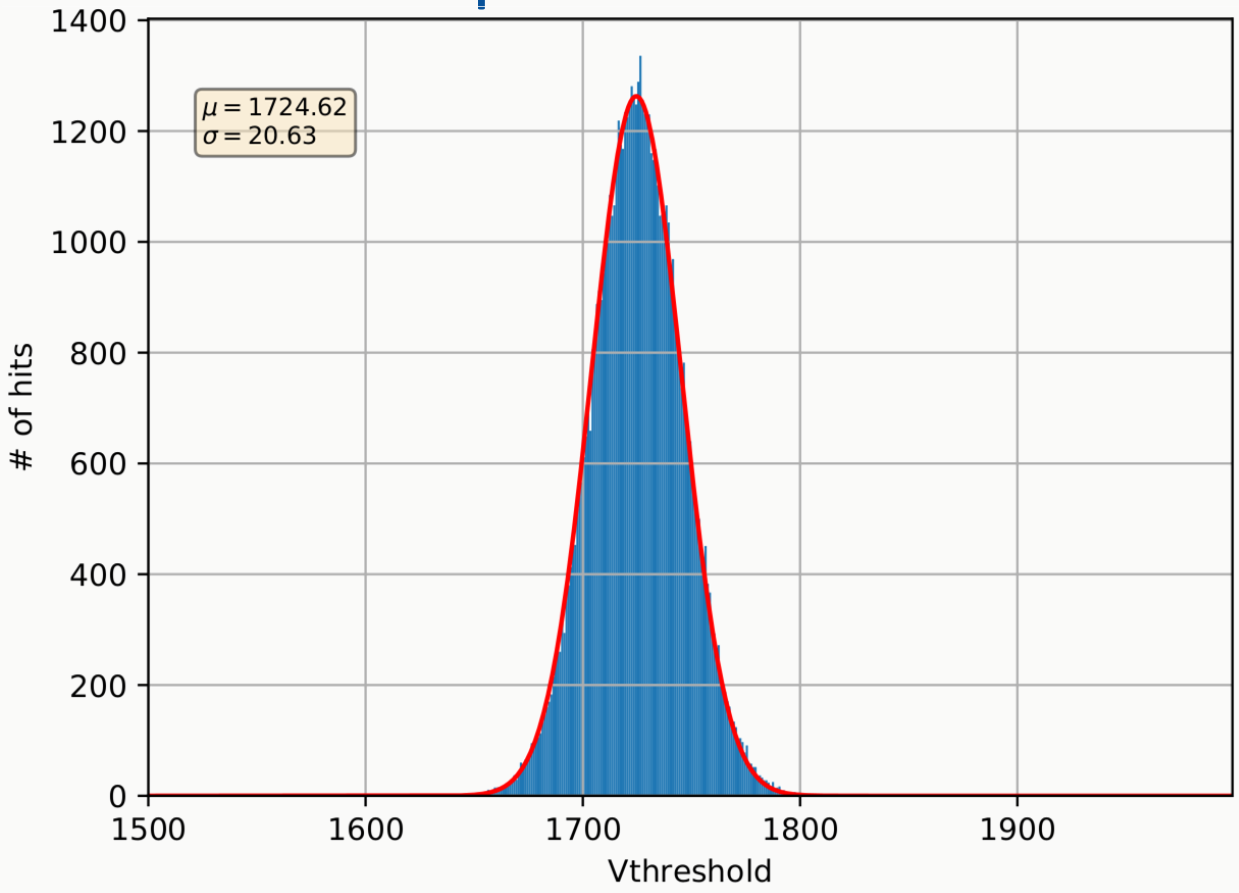
- One base module: tpx3.py
- Offers all functions of the Timepix3 to other modules
- Settings via YAML files
- Data storage in HDF5 files

# SOFTWARE - SCANS

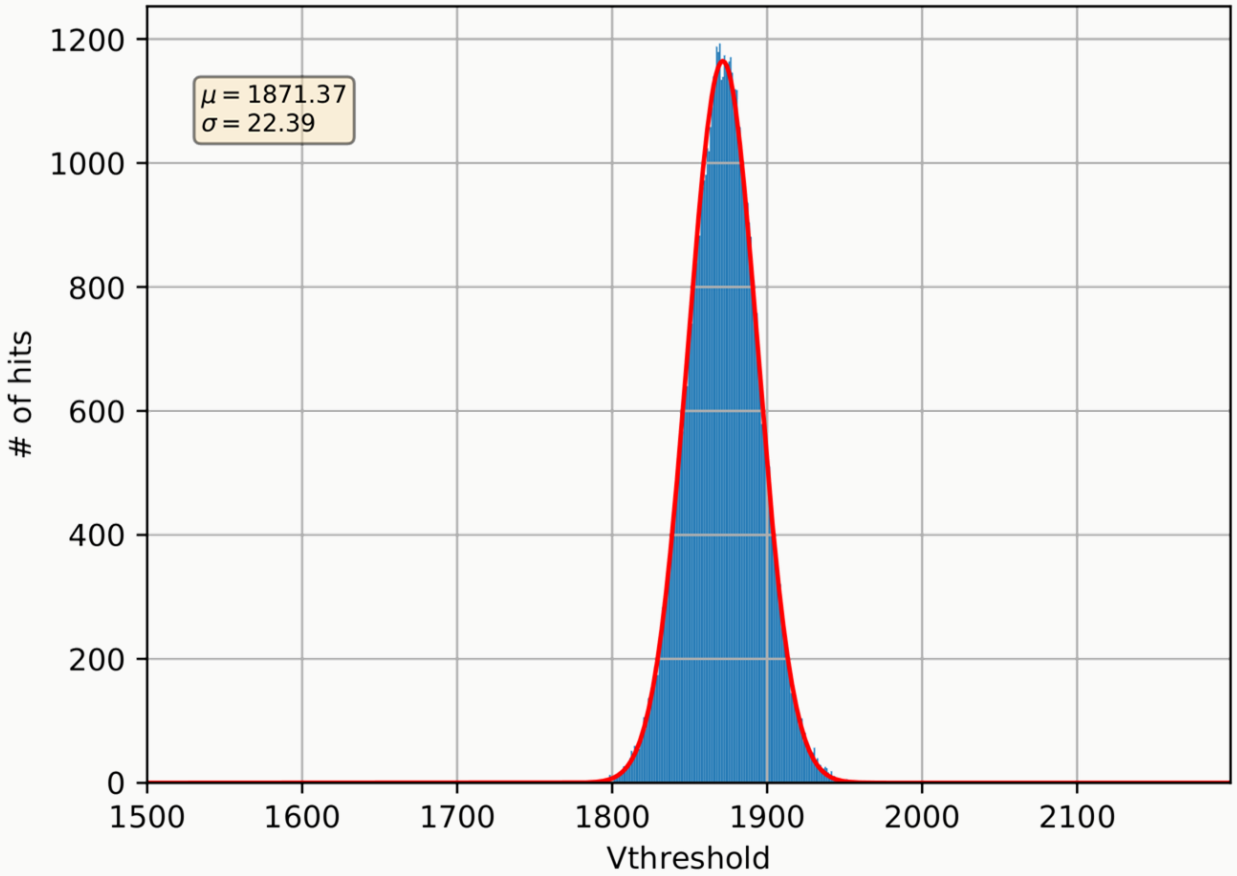


# EQUALISATION

## Scan at pixelthreshold 0




## Scan at pixelthreshold 15



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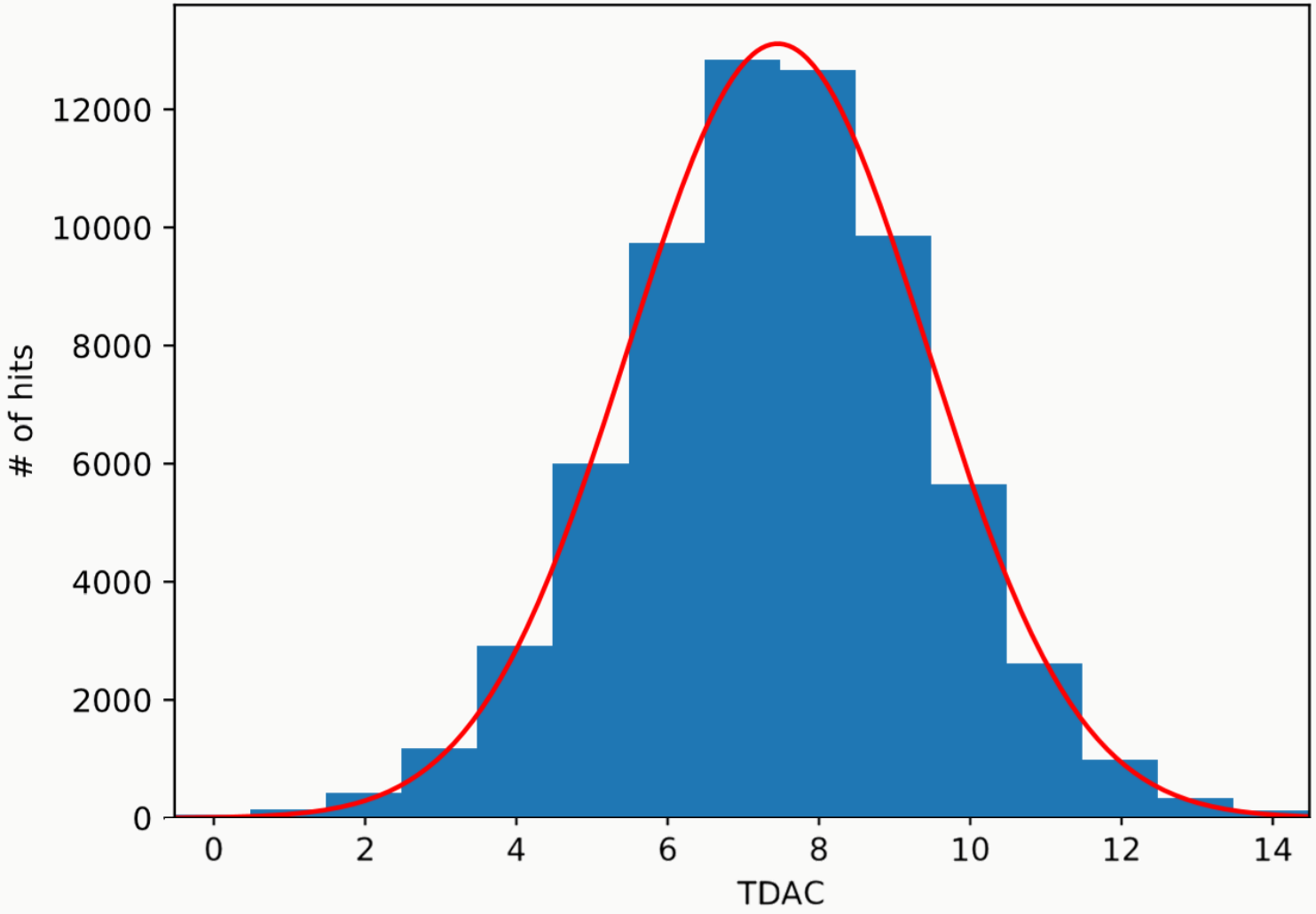
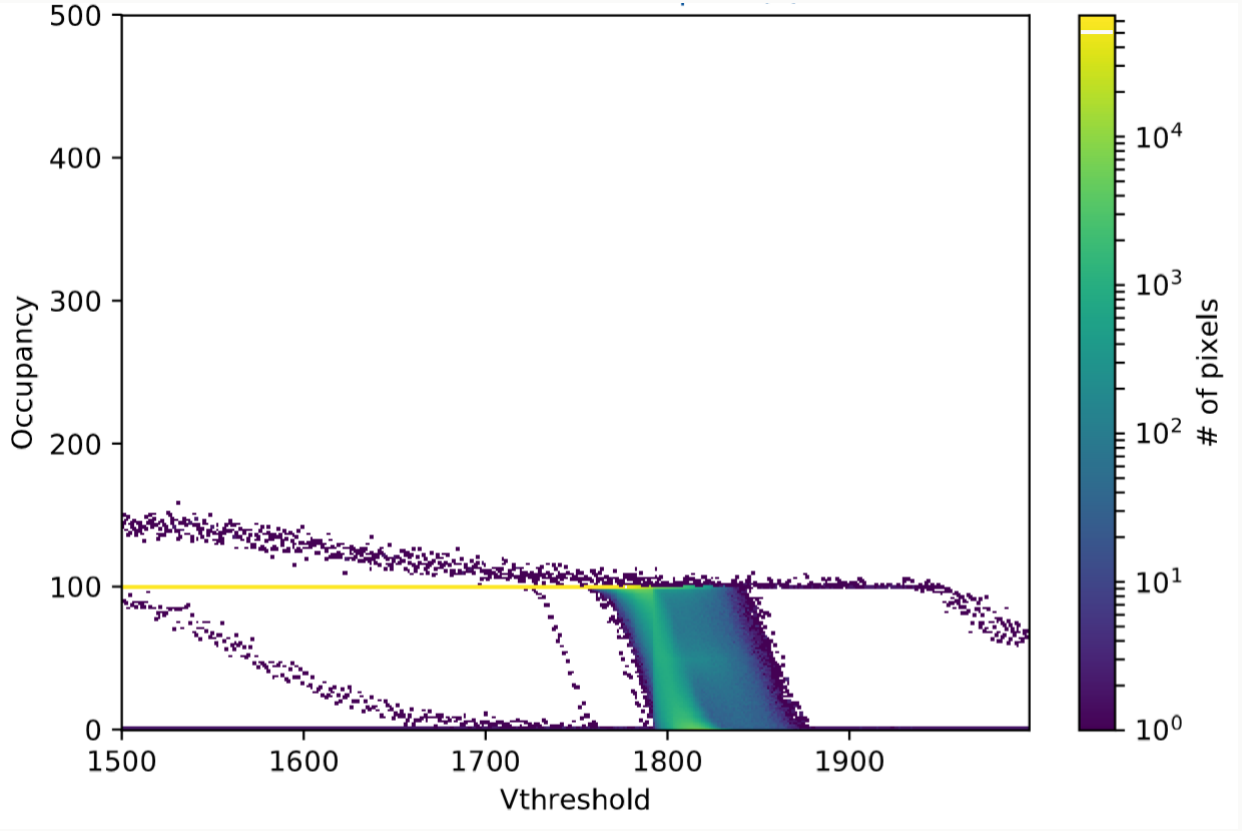
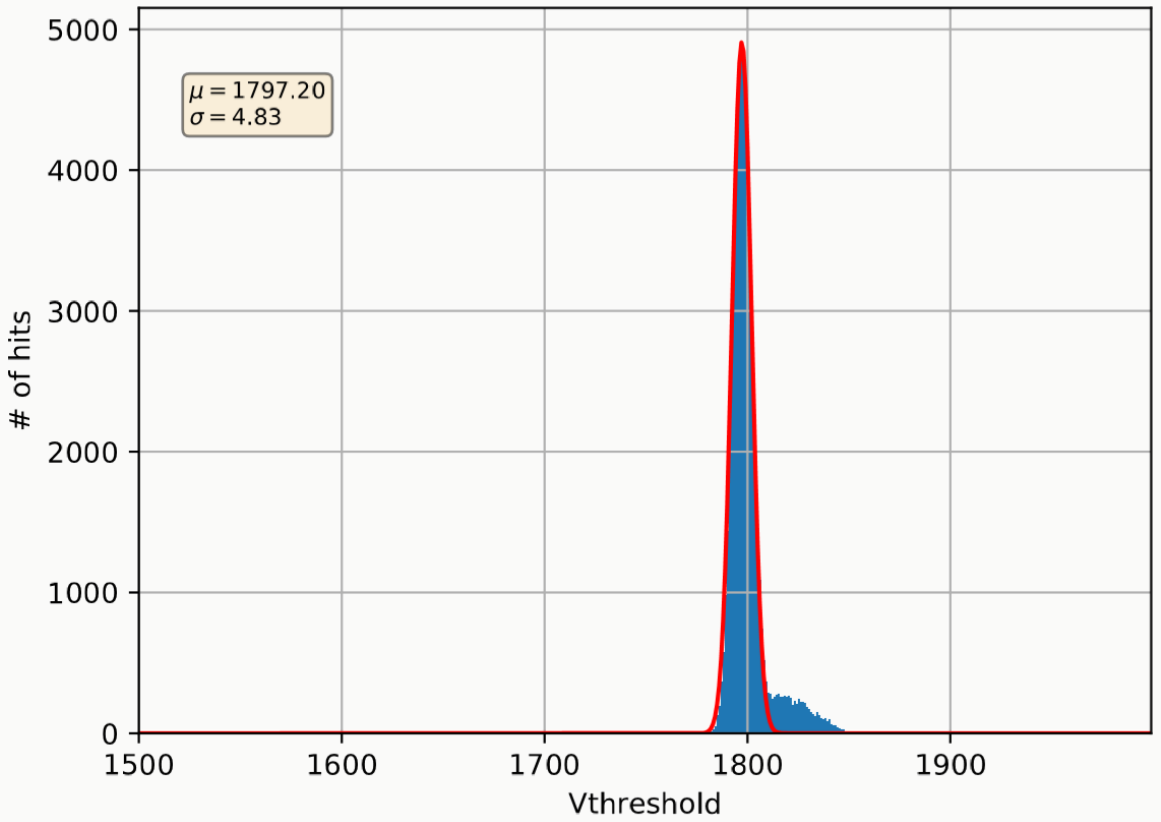
# EQUALISATION – PIXELTHRESHOLD DISTRIBUTION



# S-CURVES


Occupancy
Vthreshold
# of pixels
500
400
300
200
100
0
1500
1600
1700
1800
1900
$10^4$
$10^3$
$10^2$
$10^1$
$10^0$


$\mu = 1797.20$
$\sigma = 4.83$
# of hits
Vthreshold
5000
4000
3000
2000
1000
0
1500
1600
1700
1800
1900

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# TESTING

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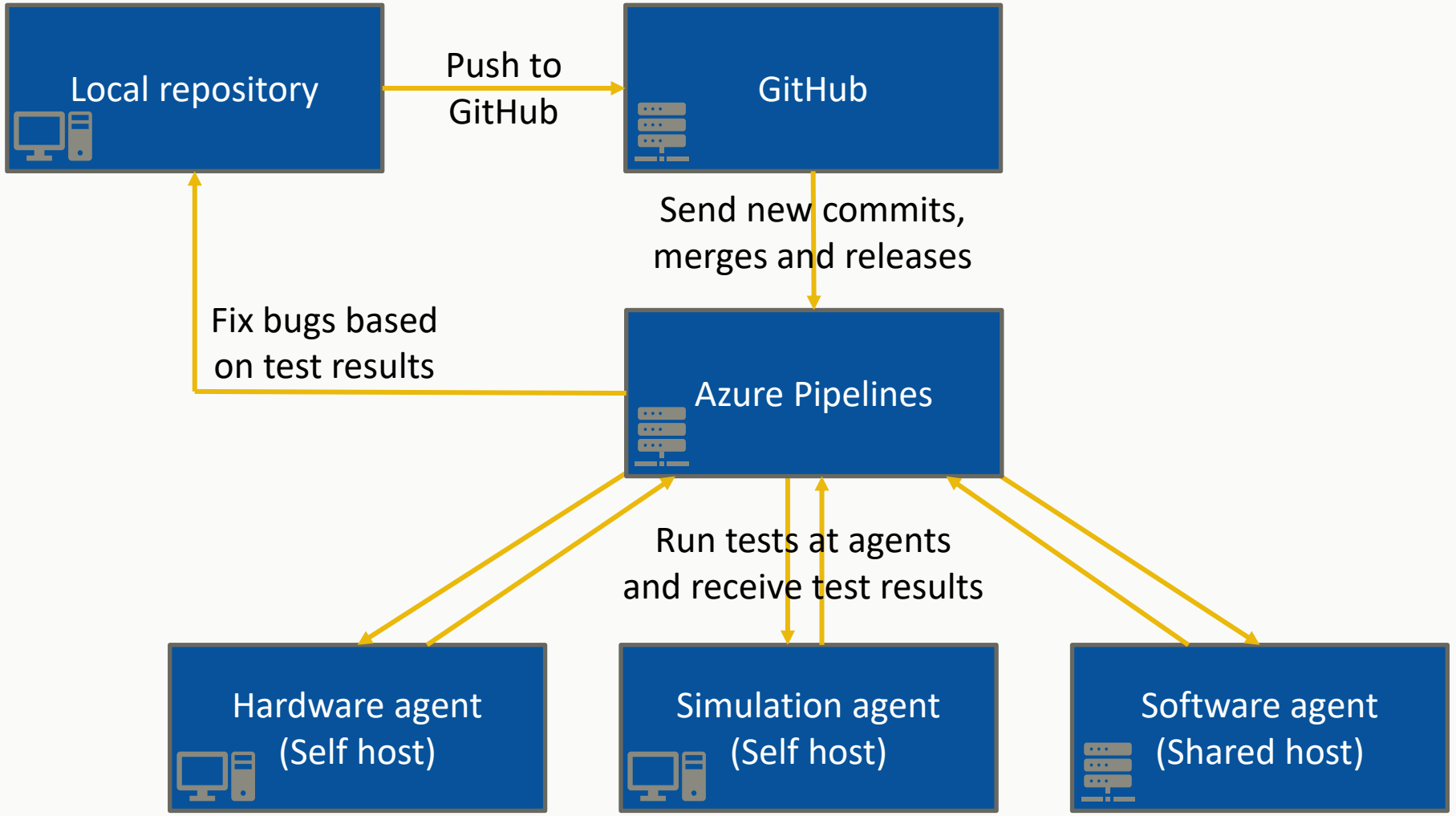
# TESTING



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# TESTING – CURRENT TESTS

- Write and read all DACs with all possible values
- Write and read all config registers with all possible values
- Write and read random pixel matrices
- Check the ChipID
- Check of software error messages

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# TESTING – ADDITIONAL FUTURE TESTS

- Test of analysis and plotting functions
- Check of communication based on local headers (chip specific communication)
- Check of the data storage backend
- Tests of DAC voltages / currents and of chip temperature

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# DESIGN GOAL

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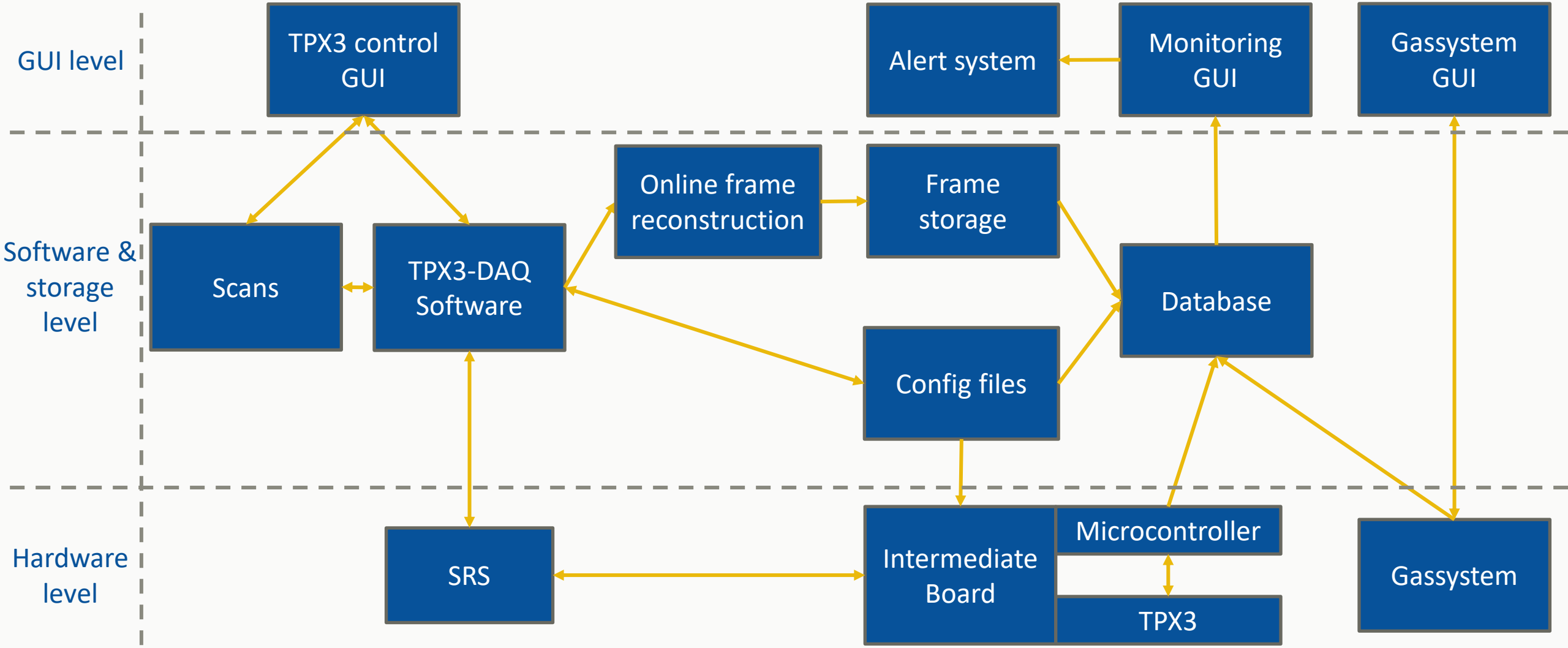

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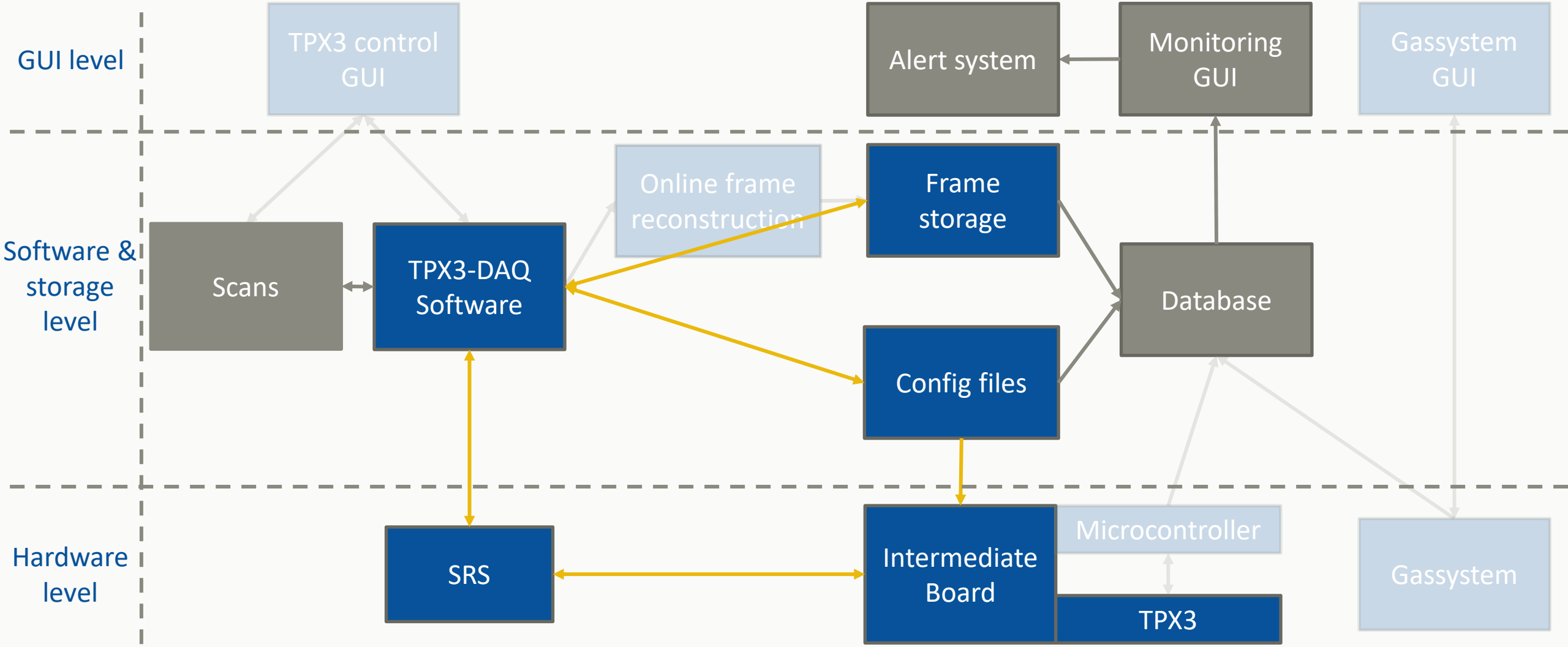
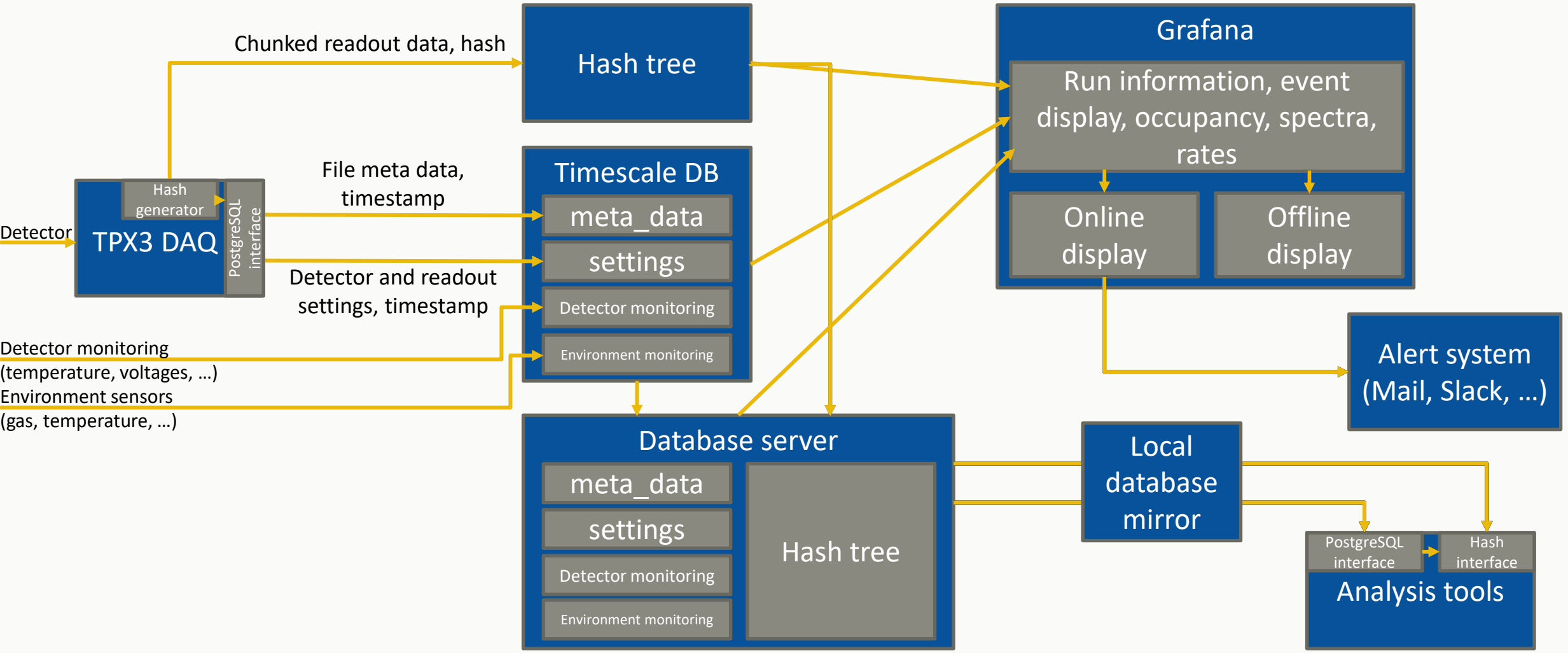
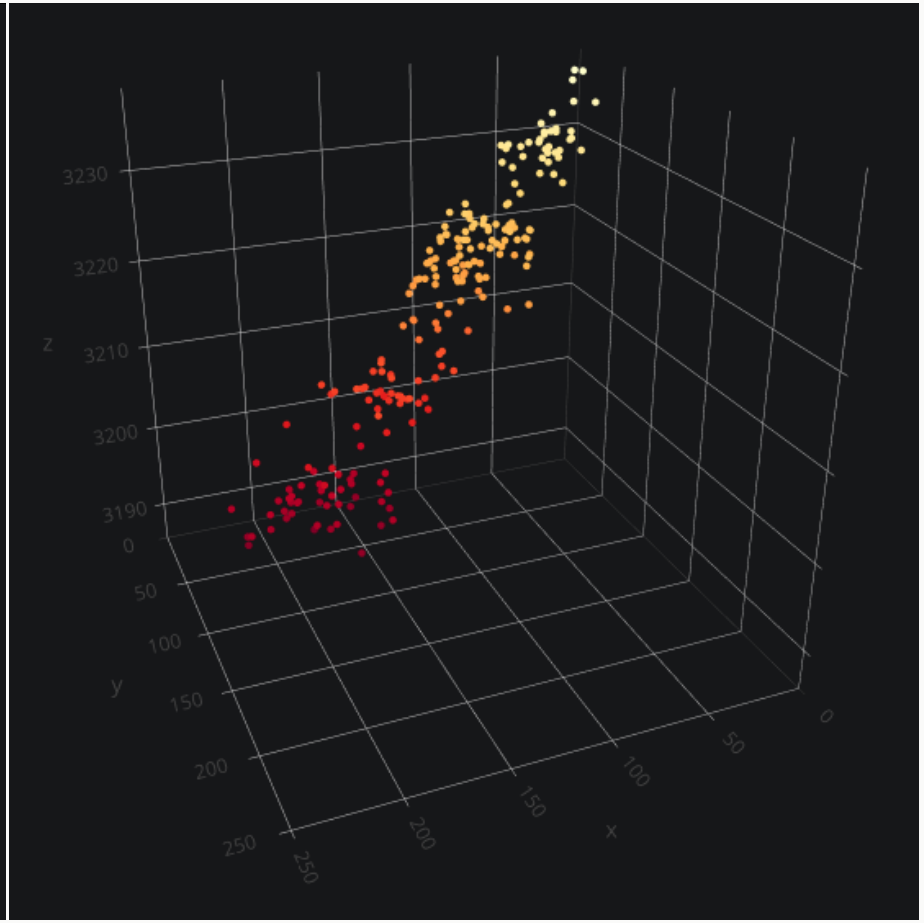
# DESIGN STATUS



# DATA STORAGE AND MONITORING



# GRAFANA AND DATABASE TEST WITH TIMEPIX

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# GAS MONITORING

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# CONCLUSION

- Development of base functions (nearly) complete
- Scans in development
- Next steps:
  - Storage backend
  - Multiple chips
  - Monitoring

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# LINKS

- Tpx3-daq: https://github.com/SiLab-Bonn/tpx3-daq
- Basil: https://github.com/SiLab-Bonn/basil
- Grafana: https://grafana.com/
- TimescaleDB: https://www.timescale.com/