New SRS Hardware

SRS video

https://drive.google.com/open?id=1I4WKhdKDPnL8NvRtvZsY6-sGOQZDwVZn

SRS full transition completed

VMM3 hybrid , 50 hybrid pilot production rev.4 success, volume production (SRS Tech)

VMM3 coolers, completed & available as kit

DVM card rev 5 for VMM, full revision FW and HW,

2 protos built, volume production (SRS Tech)

CTF card rev 6, 5 built, volume production(SRS Tech)

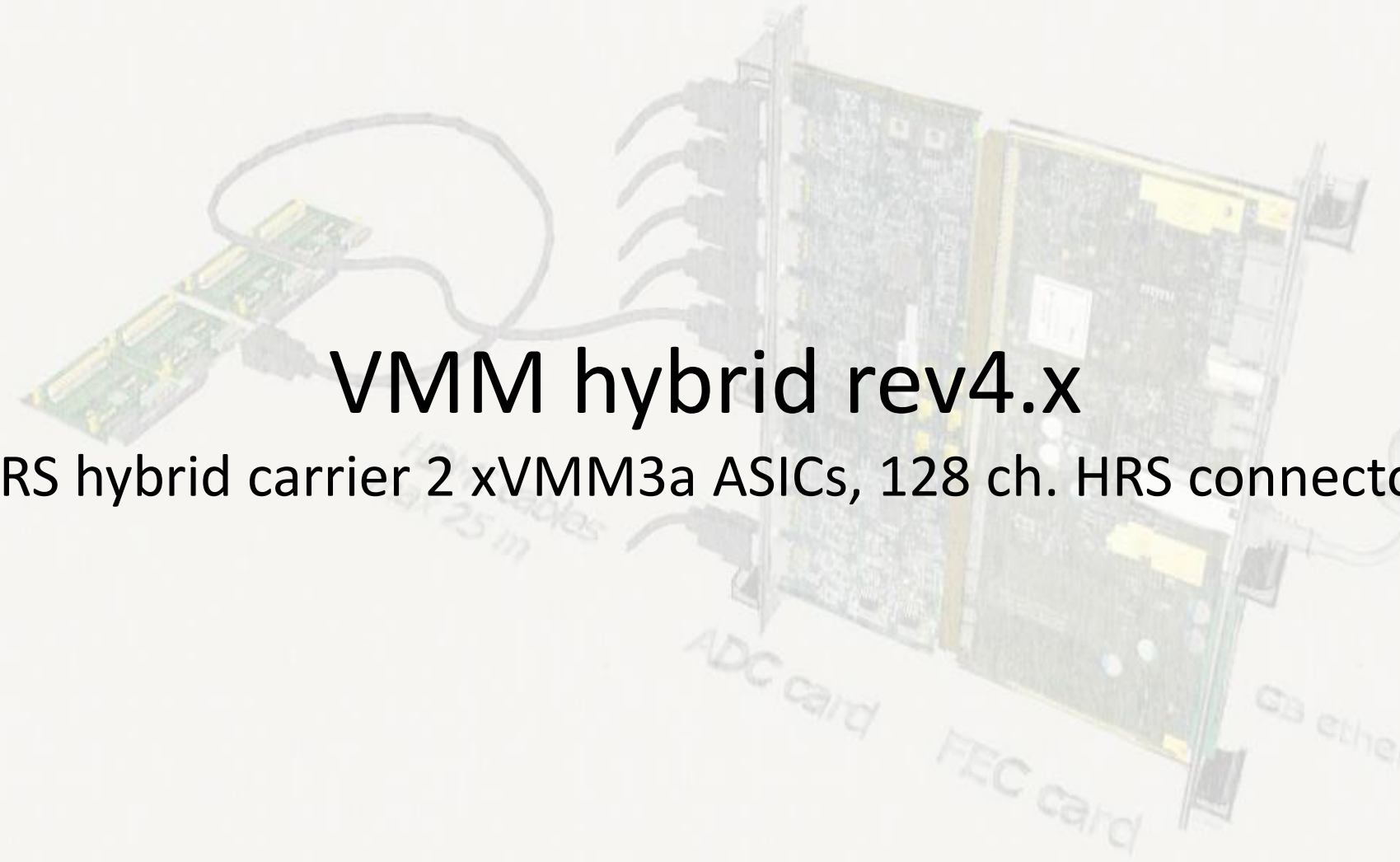
Minicrate ABC, 10 prototypes built, commercial production started (NEOHM) => CERNstore

HRS adapters, variants available

APIC preamp-shaper, 10 protos built, 5 on order

ongoing, coming

- Eurocrate V2, 8 FEC slots prototypes built, commercialization planned 2020
- MCA plugin for APIC (wireless) , very successful summer student project, much advanced and being continued
- Powerbox for VMM, delayed due to higher priorities, to be resumed

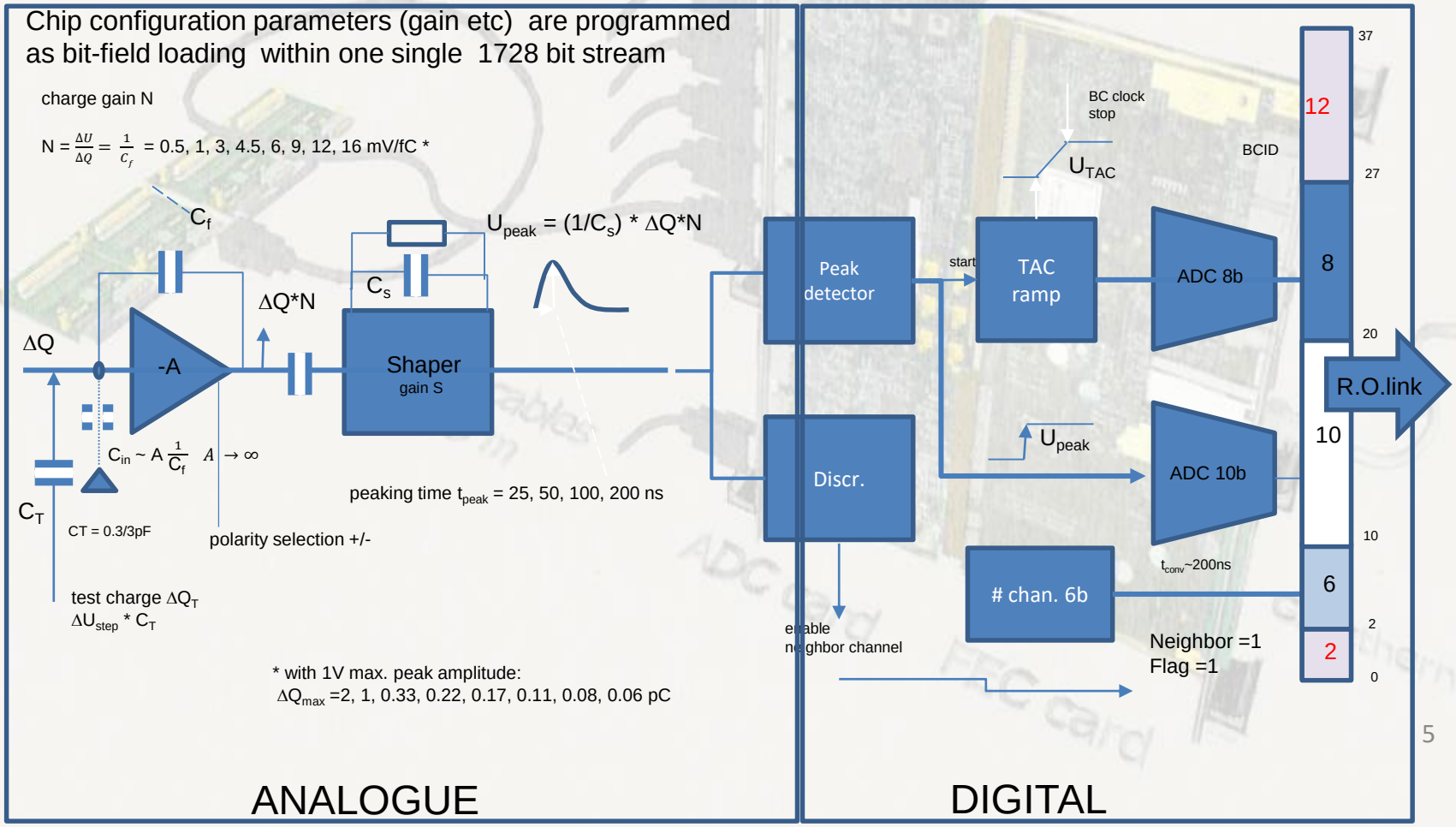


VMM hybrid rev4.x

SRS hybrid carrier 2 xVMM3a ASICs, 128 ch. HRS connector

One of
32 channels
per VMM ASIC

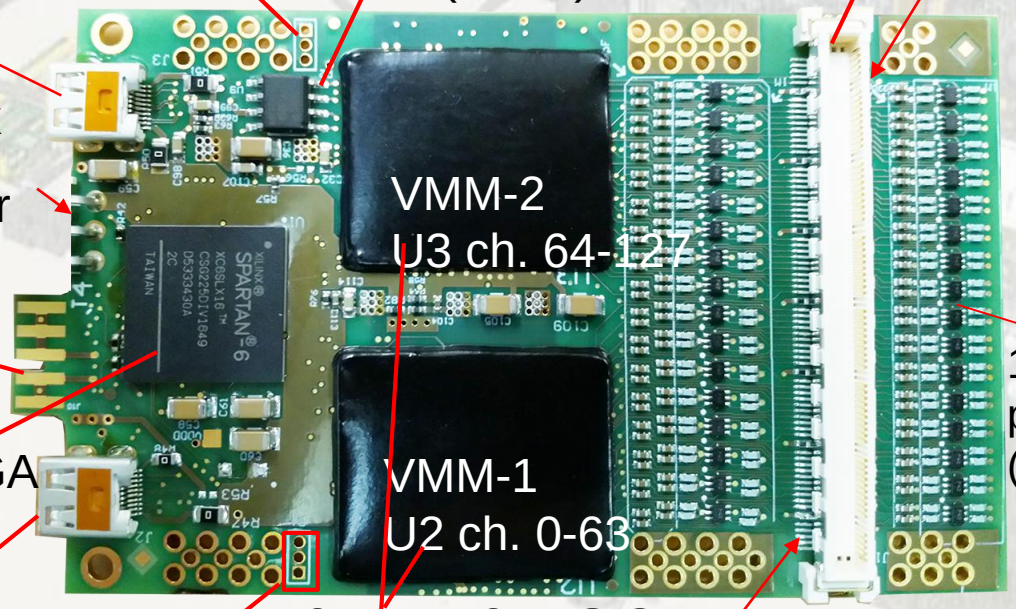
VMM3 ASIC in continuous* readout mode



38 bit, data-driven event frames

* so far, only continuous mode implemented in SRS readout

SRS hybrid V4.x bottom side



analogue signals VMM-2

U9 (Flash)

J1 140 –way HRS connector FX10A

channel 127 (4th pin from top

J3
HDMI micro
opt. Slave link

J4 AUX power

J10 (JTAG)
+I2C (new)

U1 Spartan FPGA

128 x input AC and spark protection network (default 470pF)

J2
HDMI-Micro
default Master link

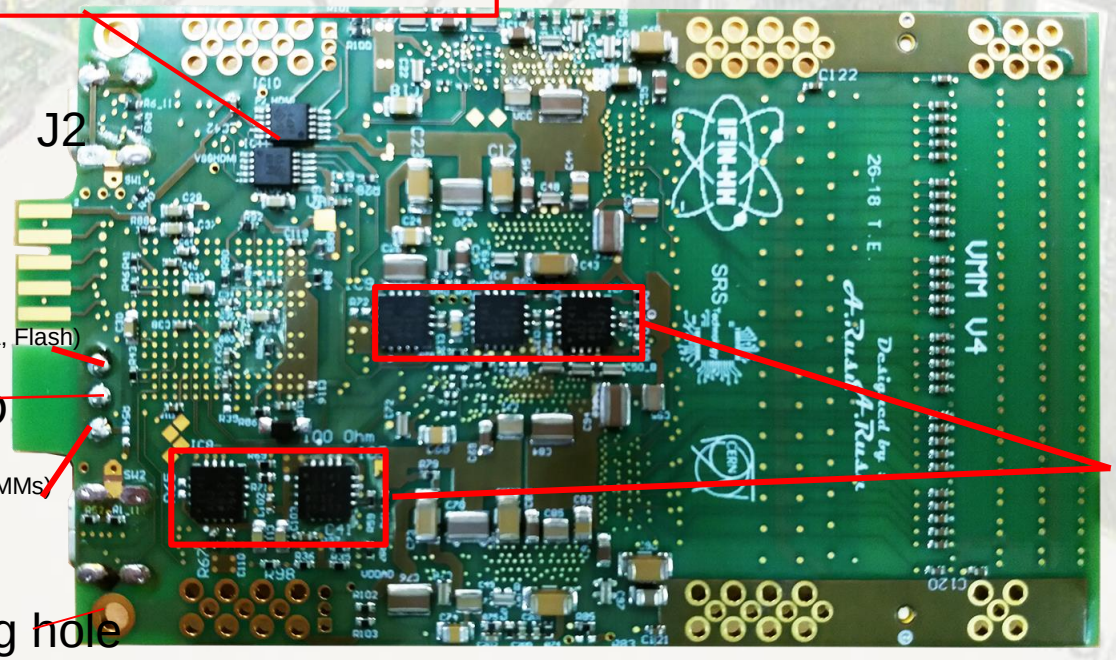
2x VMM3a ASICs
(below globtop)

channel 0 (4th pin from bottom)

analogue signals VMM-1

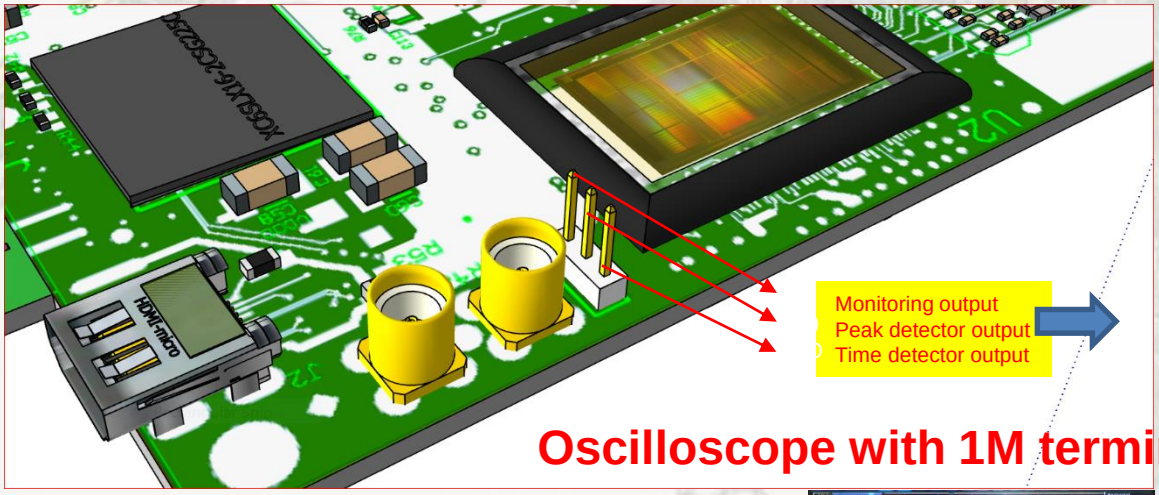
SRS hybrid V4.x (top side)

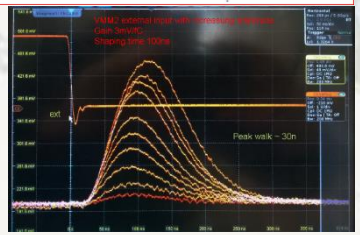
uADCs ADS1015, 12 bit 4 channels (readout via I2C)
Connected to PDO, PTO, MO analogue lines on P1,P2
IC10 - U2 VMM1
IC11 - U3 VMM2



LDOs: IC5-9 are 2-Ampere CMOS LDO's of type ADP174ACPZ-R7
IC7 VDPP, 1.2V , 150 mA preamplifiers
IC6, VDD, 1.2V, 400mA analogie section
IC9, VDDAD, 1.2V 200mA , ADC's
IC5, VDD, 1.2V 150 mA,Digital +SLVS drivers
IC8, VAUX, 2.5V, 150mA, FPGA and Flash

access to analogue VMM signal (1 selected channel of 64)





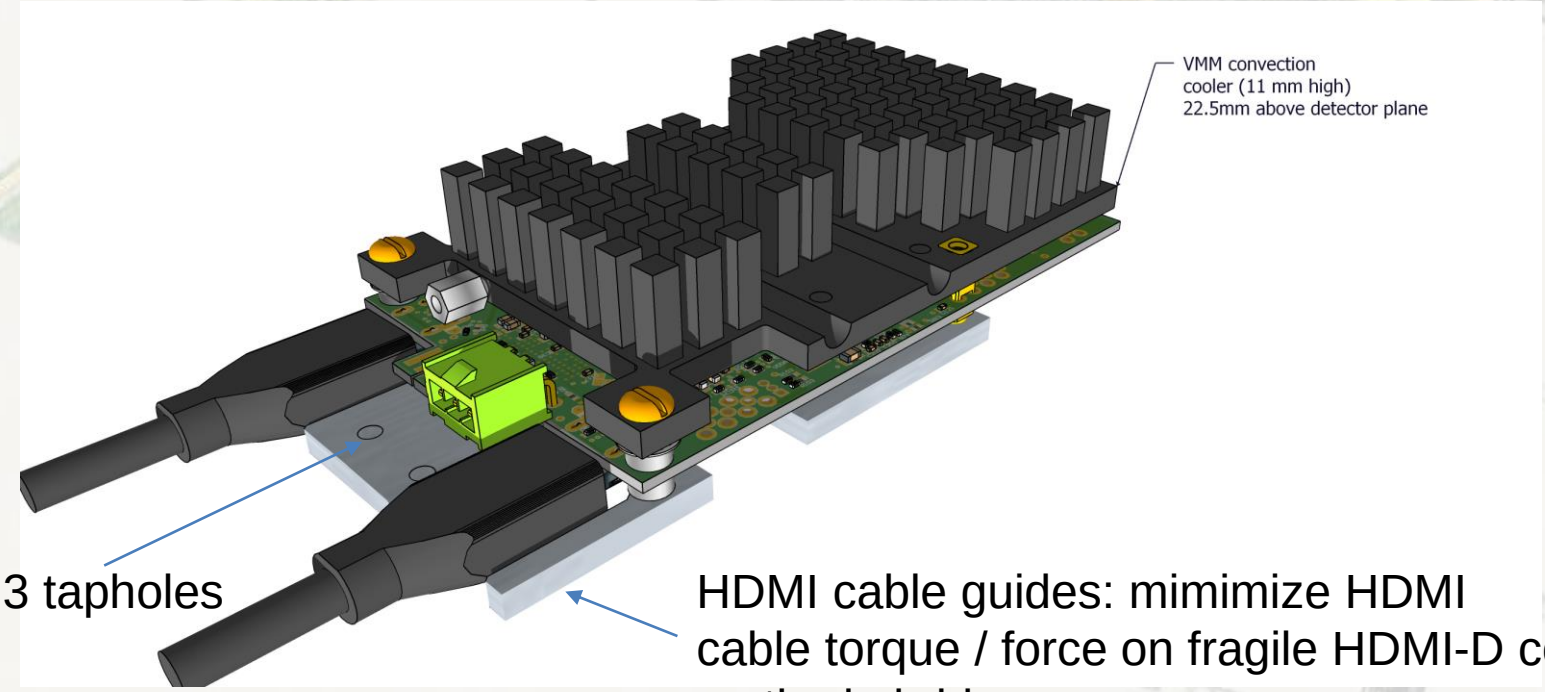
analogue MO signal output
for different pulser amplitudes

12 bit micro ADC's have been added on V4: I2C readback of
pulser DAC, threshold DAC, band-gap reference,
core temperature, analogue pulse peak, analogue time ramp

VMM convection cooler

keep chip core < 55 C

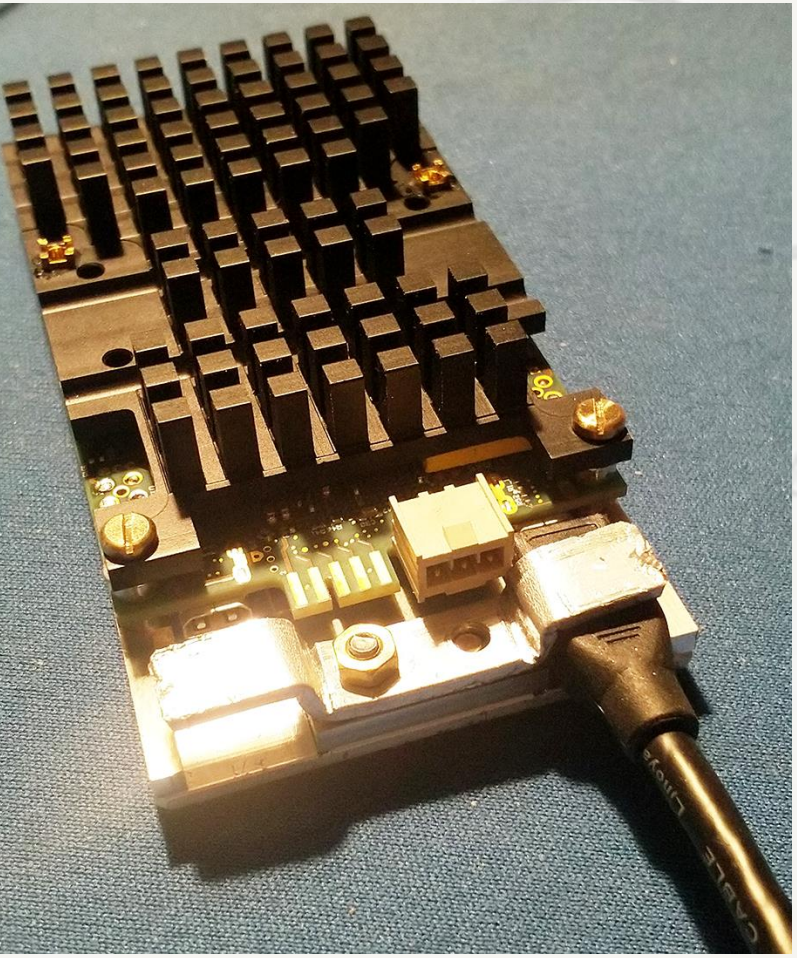
reduced height, cable un-stress guides, M3 holes for fixation screws



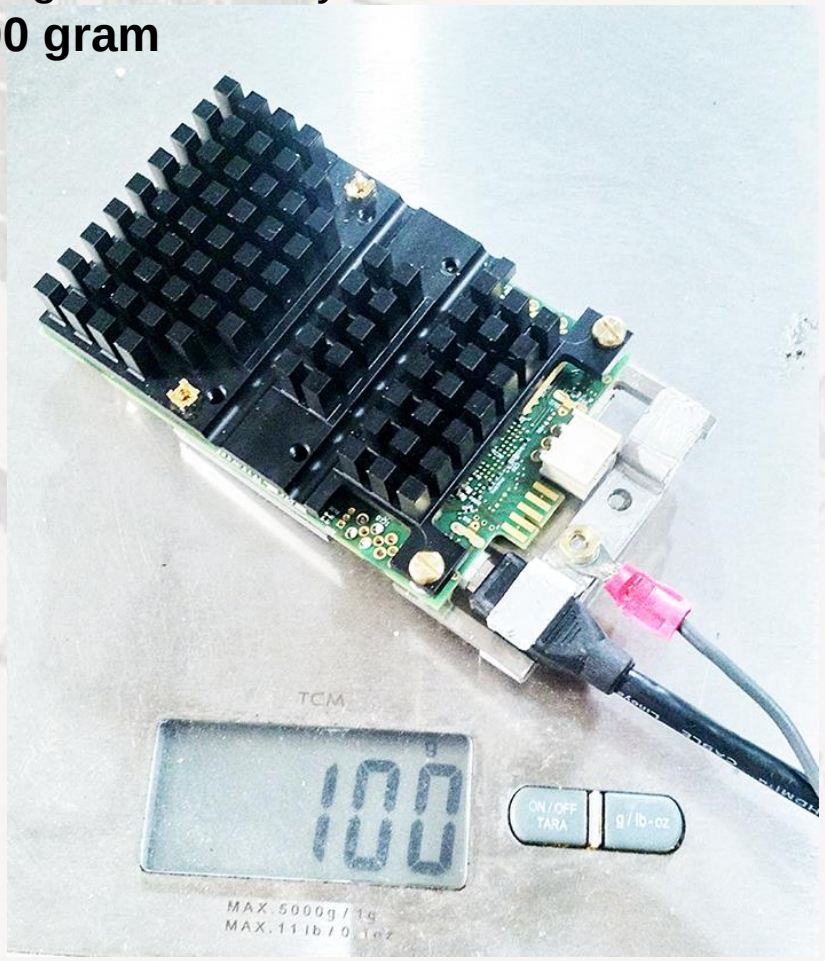
Two M3 tapholes

HDMI cable guides: mimimize HDMI cable torque / force on fragile HDMI-D connectors on the hybrid.

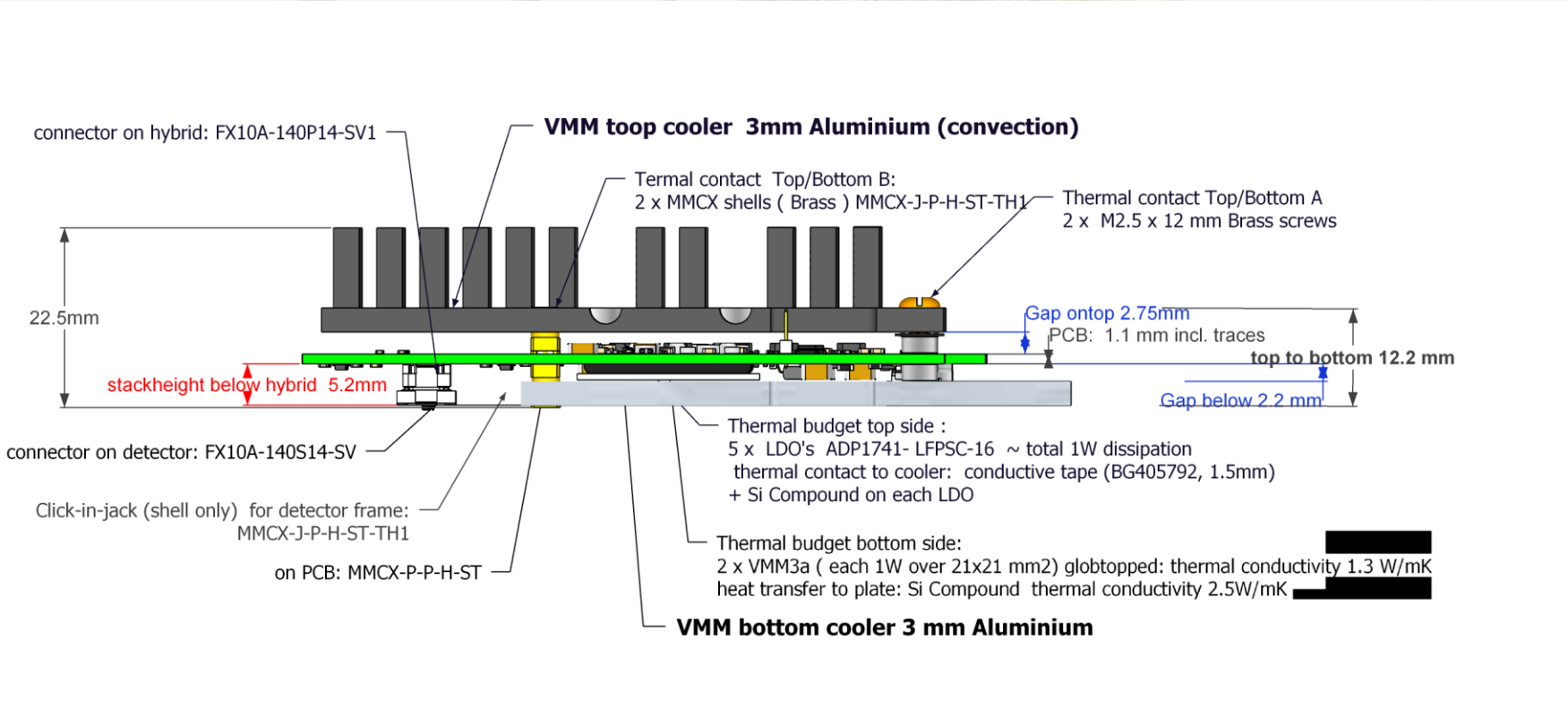
cable brackets & hybrid weight



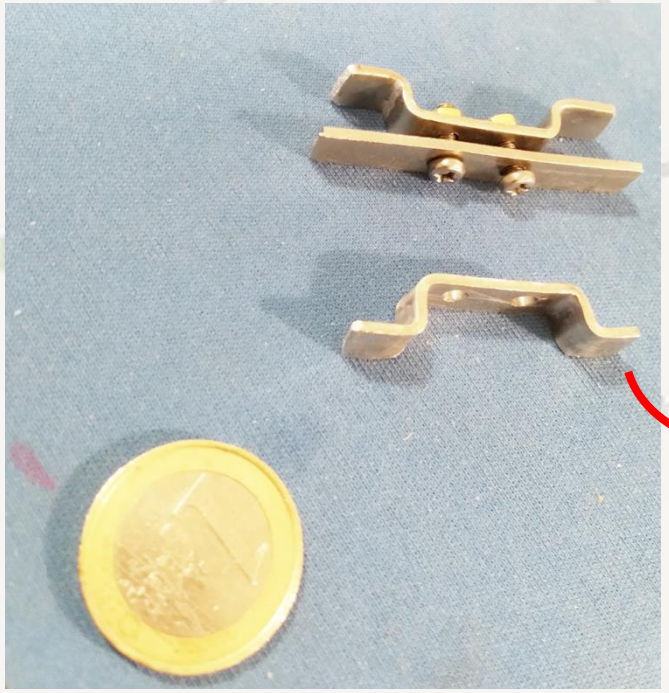
Weight of VMM hybrid incl. cooler + cable:
100 gram

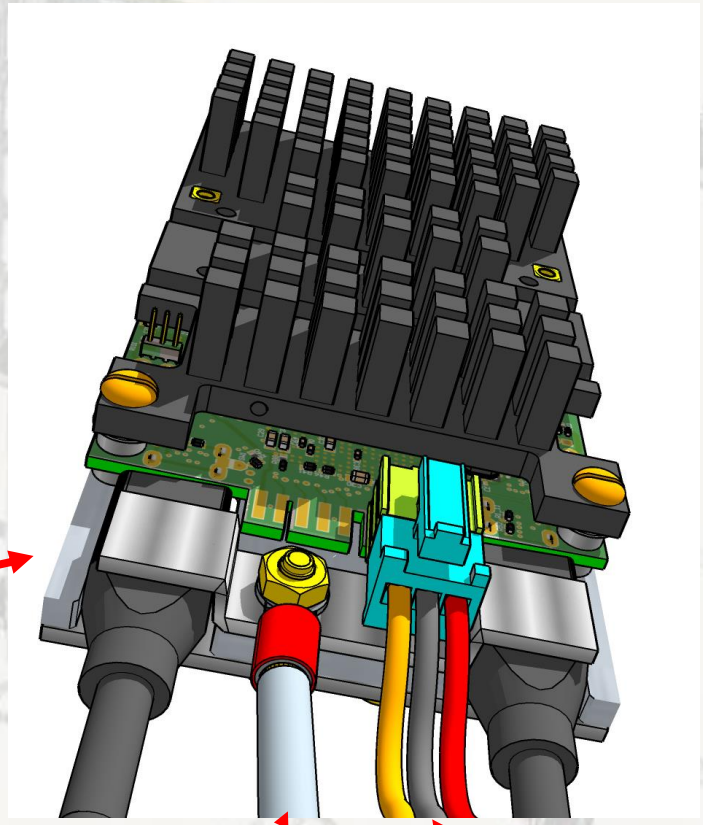


Height over detector plane with convection cooler: 22.5 mm



Cable brackets





VMM “cooler kit* ”

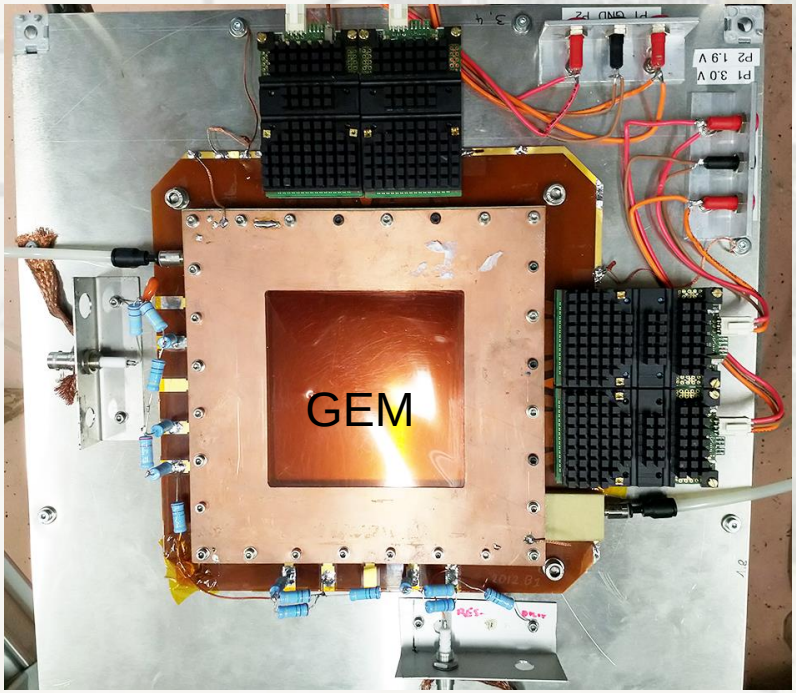
*Cooler kit:
-top convection cooler
-bottom cooler plate
-screws and spacers
-AUX connector
-Cable bracket
-MMCX shells
-thermal pads

Material prov. by user
-thermal paste
-cables and lugs
-dongles
-Tools

Fully detailed VMM assembly document and 3D files:
https://drive.google.com/open?id=1I8jf9ibZB9mMRGNDUH20axg6y3e07zfc

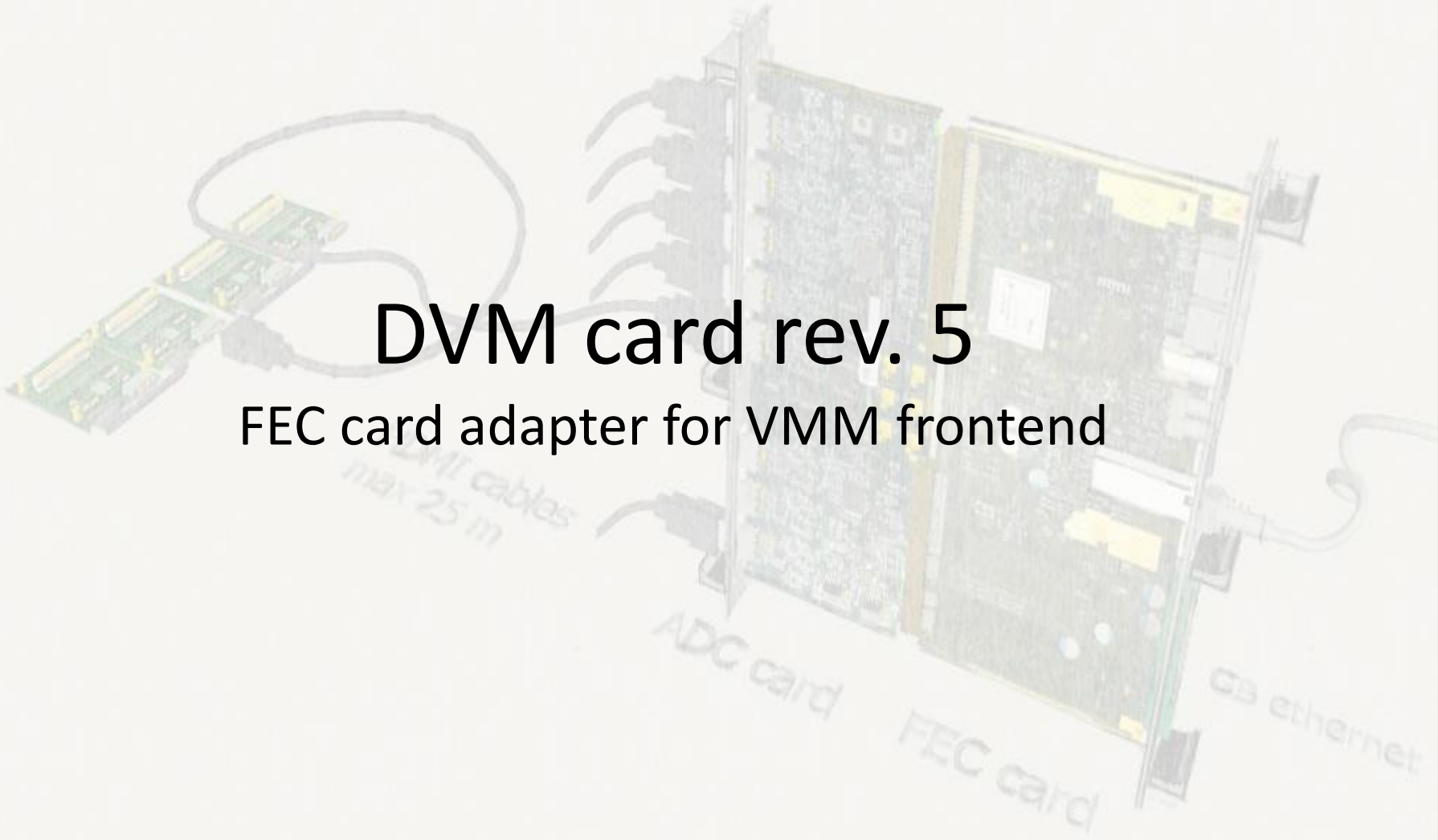
10x10 GEM with 4 VMM hybrids (256+256 channels)

See talk by : Lucian Scharenberg



Connectors
for AUX VMM power

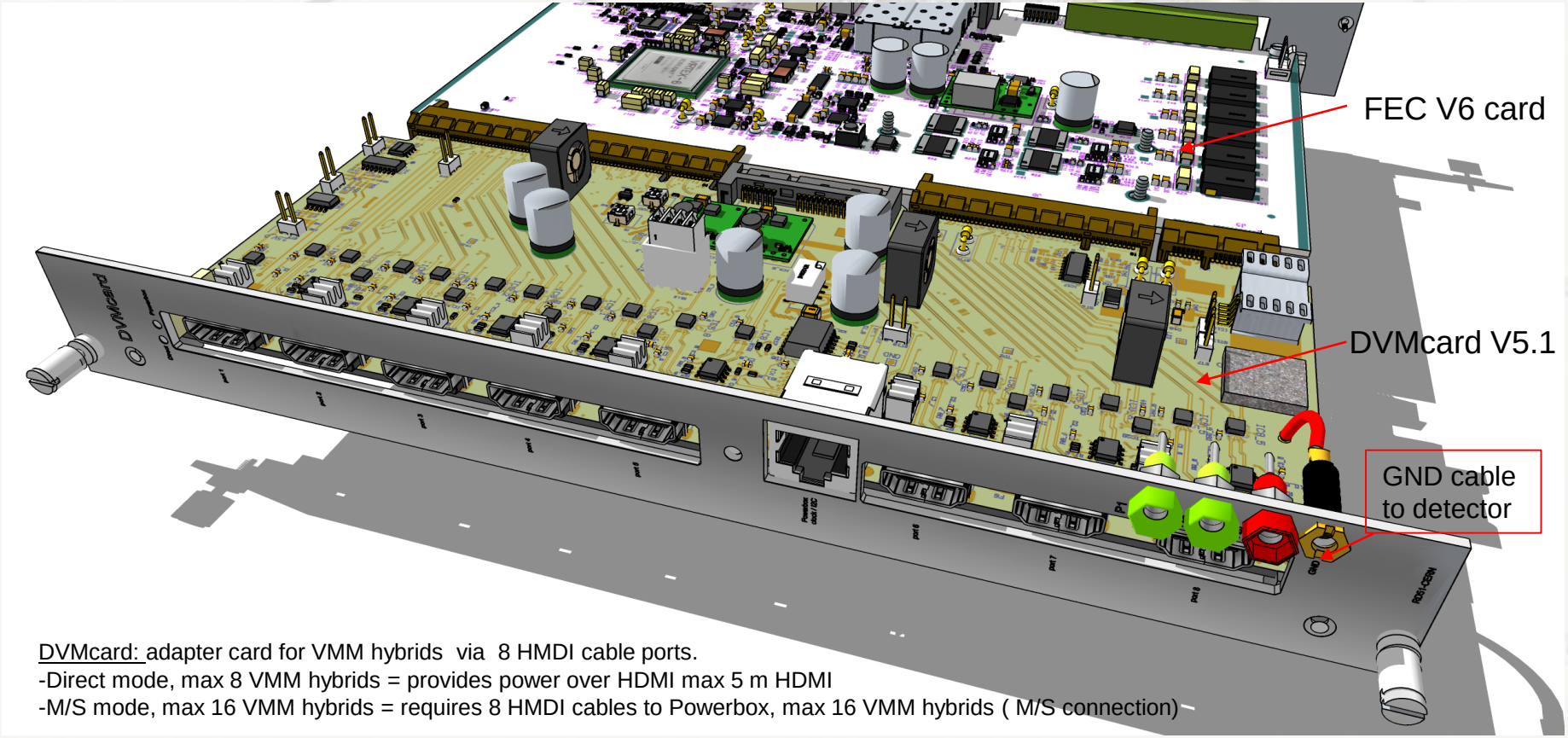
4x VMM hybrids
with convection coolers



DVM card rev. 5

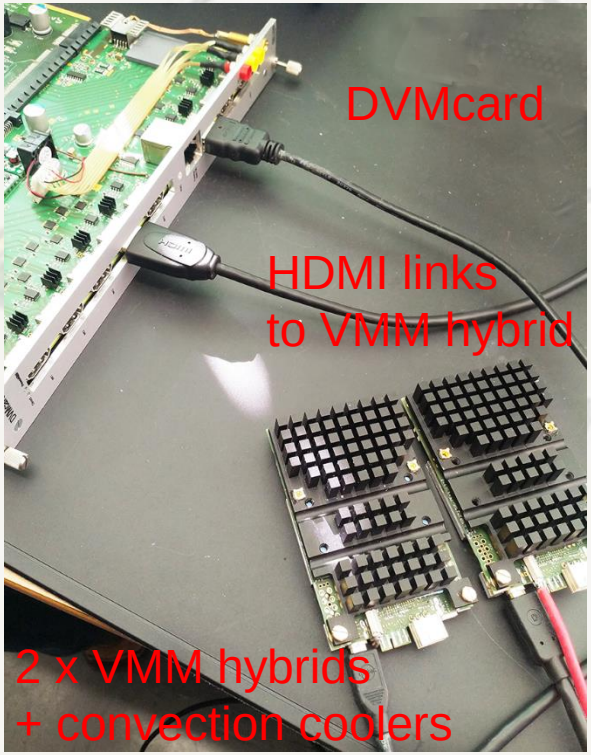
FEC card adapter for VMM frontend

DVMcard (VMM frontend)



DVMcard: adapter card for VMM hybrids via 8 HMDI cable ports.
-Direct mode, max 8 VMM hybrids = provides power over HDMI max 5 m HDMI
-M/S mode, max 16 VMM hybrids = requires 8 HMDI cables to Powerbox, max 16 VMM hybrids (M/S connection)

direct HDMI power for VMM hybrid



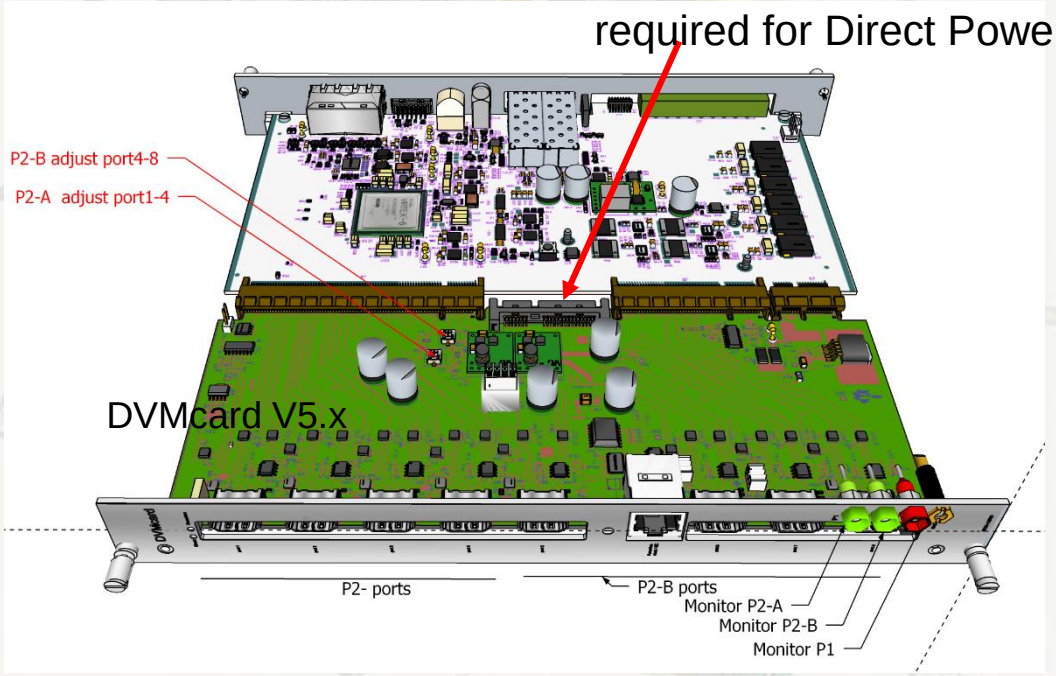
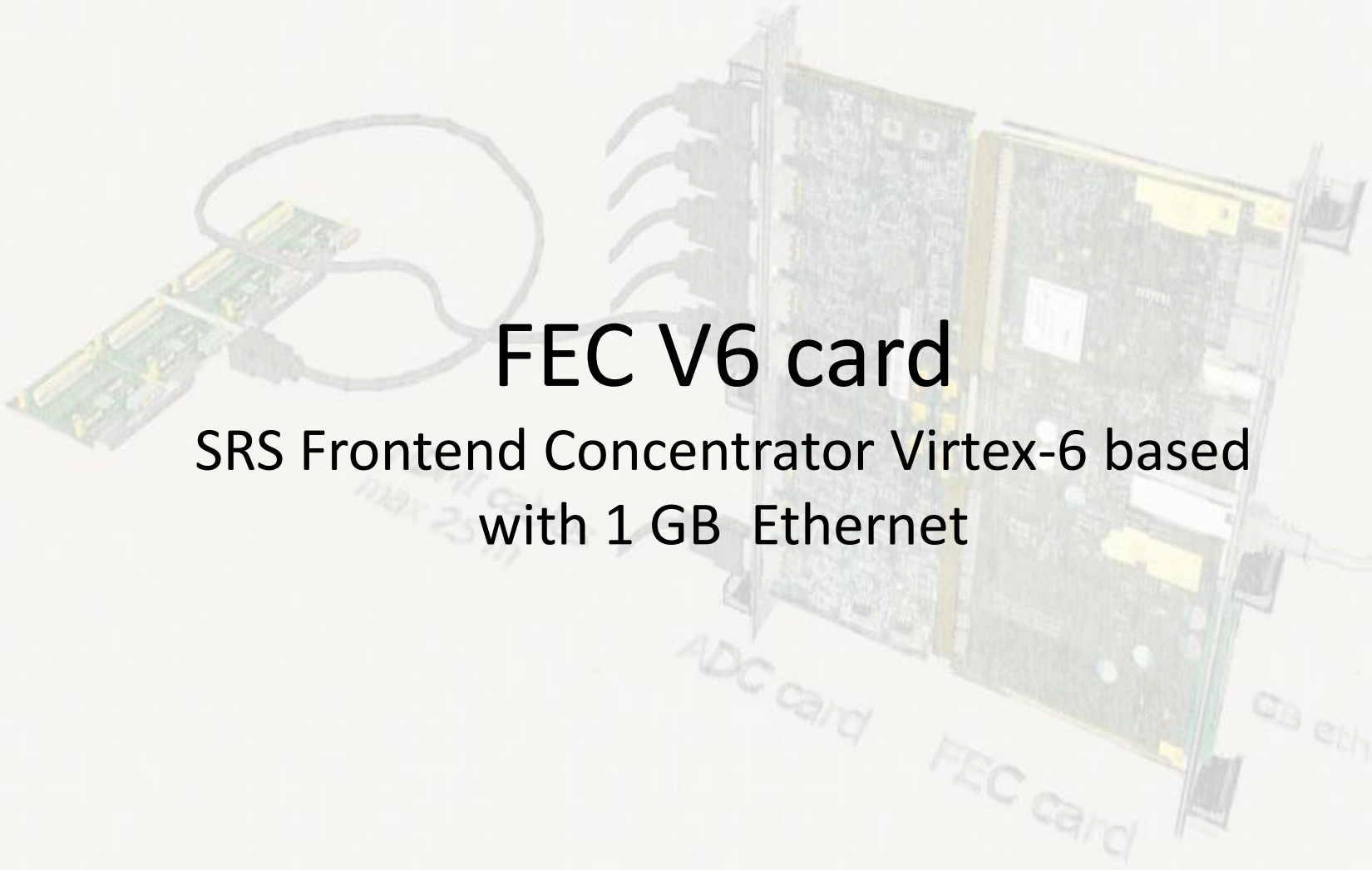


Photo: two VMM hybrids directly connected/powered by DVMcard V5.1
up to 8 VMM hybrids can get connected in direct mode

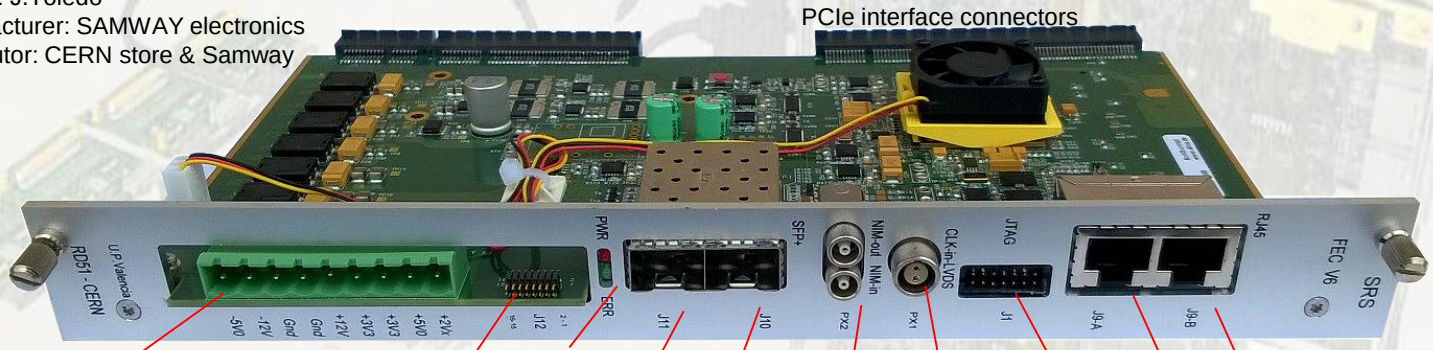


FEC V6 card

SRS Frontend Concentrator Virtex-6 based with 1 GB Ethernet

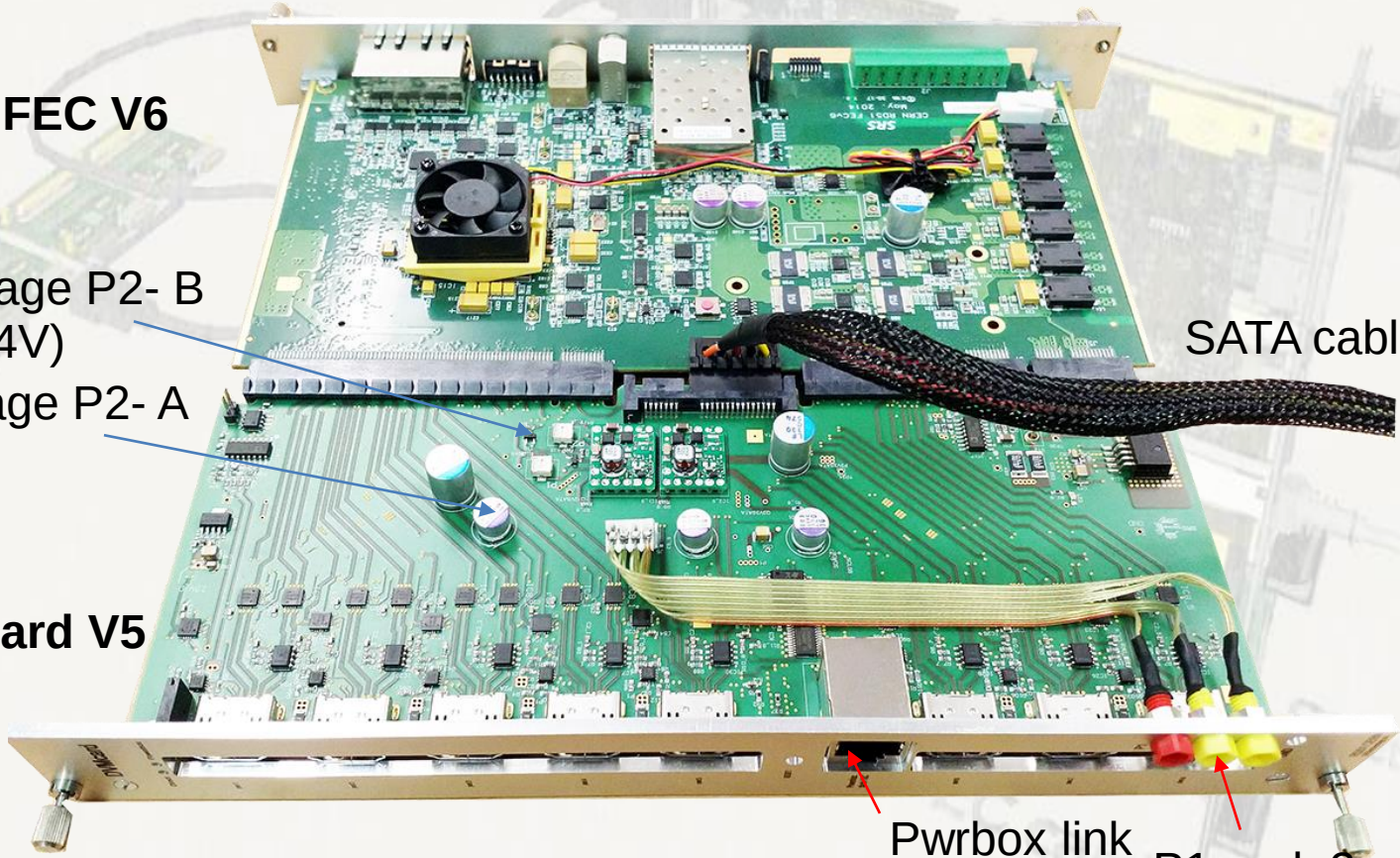
FEC Frontend Concentrator Card

Design: J.Toledo
Manufacturer: SAMWAY electronics
Distributor: CERN store & Samway



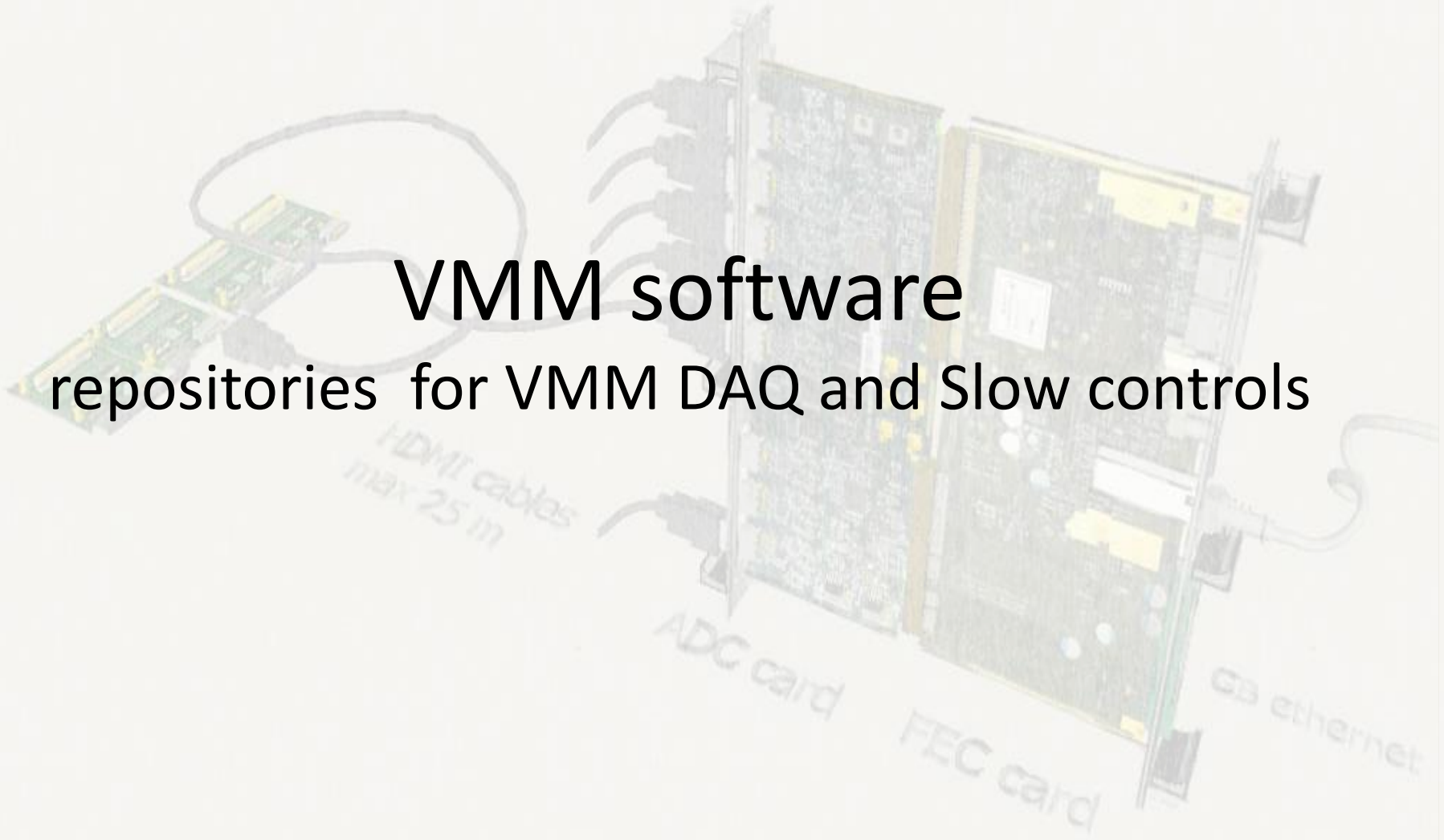
The FEC card is built around a Virtex-6 FPGA with firmware resident Ethernet/UDP core. Three PCIe connectors provide the interface to SRS Adapter cards with 18 x high –speed I/O channels, 4 x I2C branches and power for adapter cards including power for 8 APV frontend links. A back-side SODIMM connector allows for addition of a DDR3 extension memory. Several User interfaces are available for custom-programmed applications (Virtex-6 Firmware). The default firmware binaries for either APV frontend or VMM frontend can be programmed v the frontpanel JTAG connector (fits with Xilinx Dongle). Downloads are available on https://gitlab.cern.ch/SRS_firmware/fec_firmware/projects_fecv6

FEC / DVMcard combo



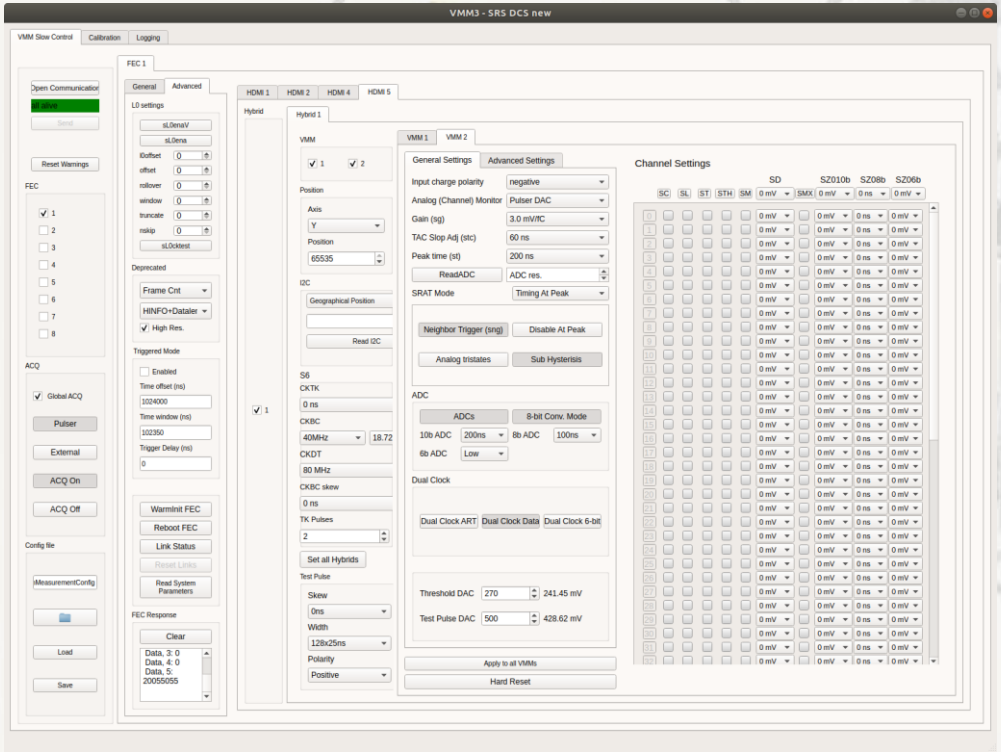
VMM software

repositories for VMM DAQ and Slow controls



2019 DAQ system for SRS with VMM

Credits: D. Pfeiffer et al.



ESS DAQ : https://github.com/ess-d

Analysis tool for ESS DAQ data : https://github.com/ess-dmsc/vmm-h

VMM3a slow control: https://gitlab.cern.ch/mguth/VMM-sc

Slow Controls GUI for SRS run con with VMM3 frontend connected via

https://cds.cern.ch/record/2296761/files/document.pdf

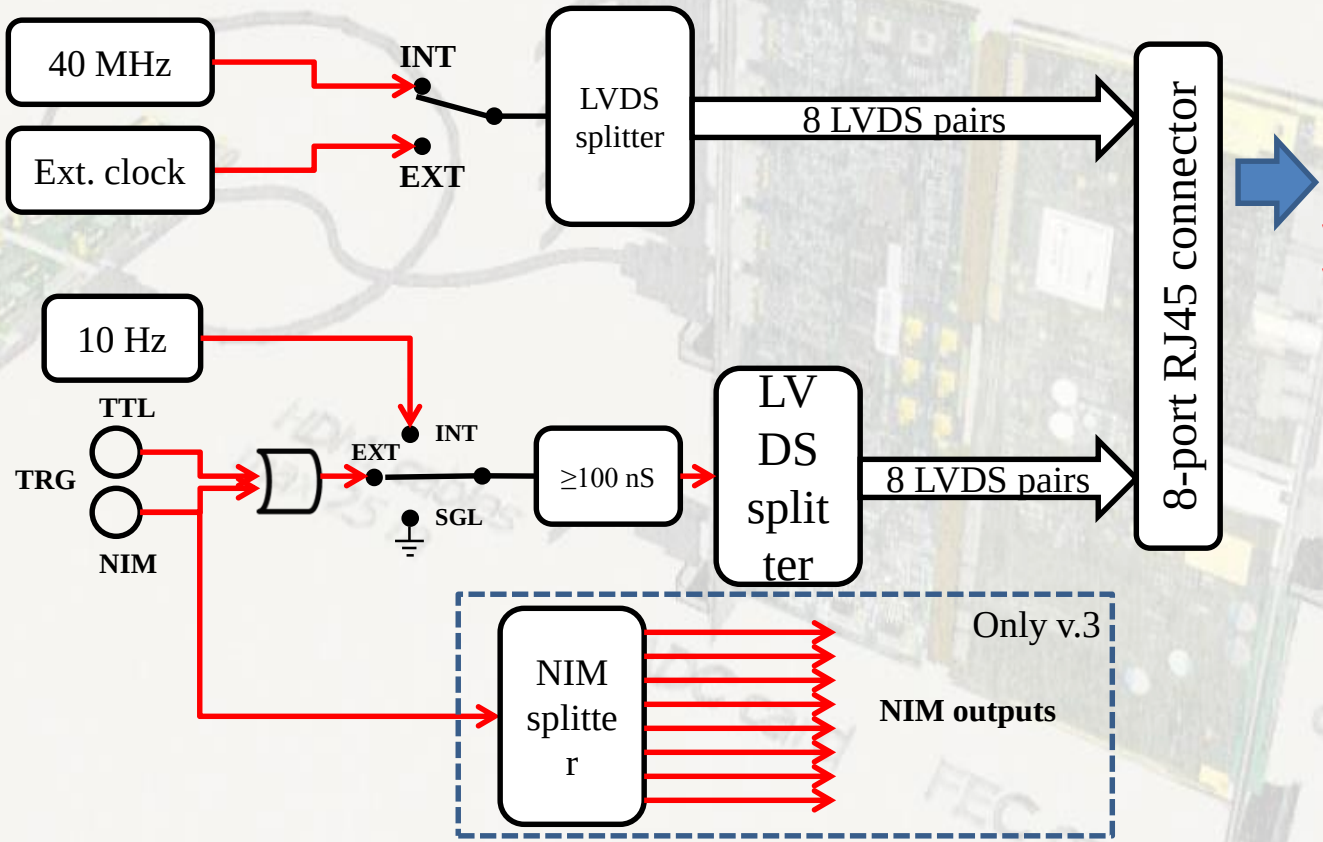
Note: for DVMcard V5.x FEC firmware needs to be flashed with new version

CTF card rev 6

common cock and trigger for several (max. 8) FECs

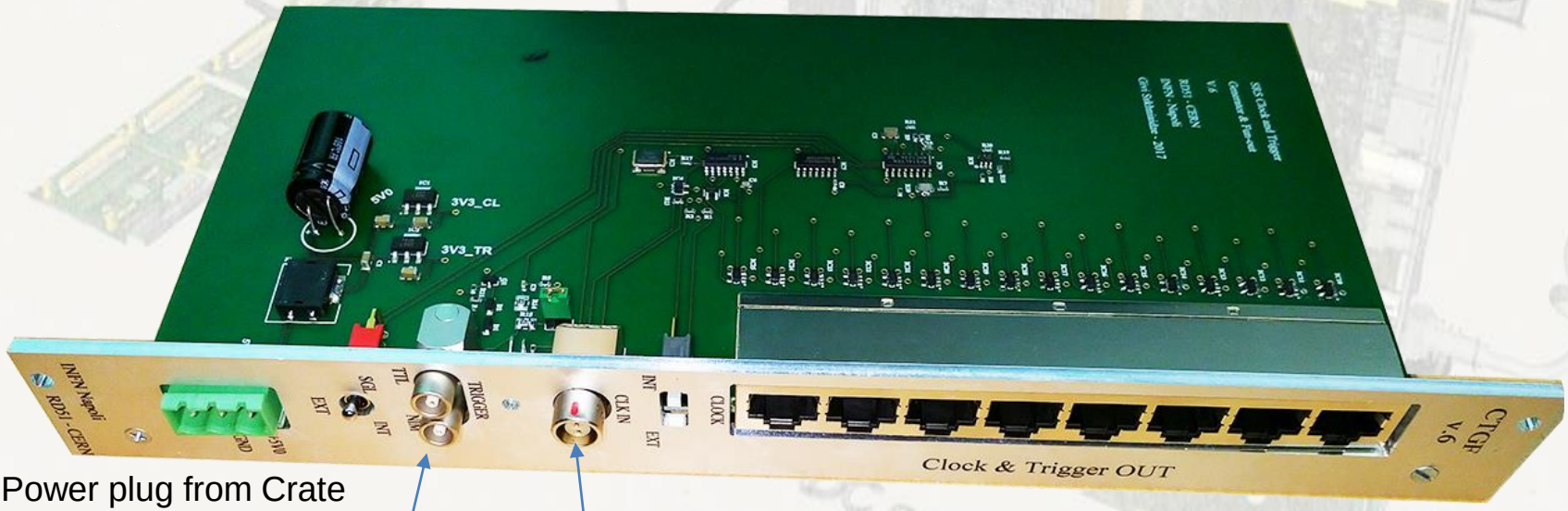
CTGF block-diagram

see G. Sekhniaidze
December 2017
Miniweek RD51 WG5



CTF clock and trigger Fanout

Design: G. Sekhniaidze
Distributor: SRS Technology



Power plug from Crate

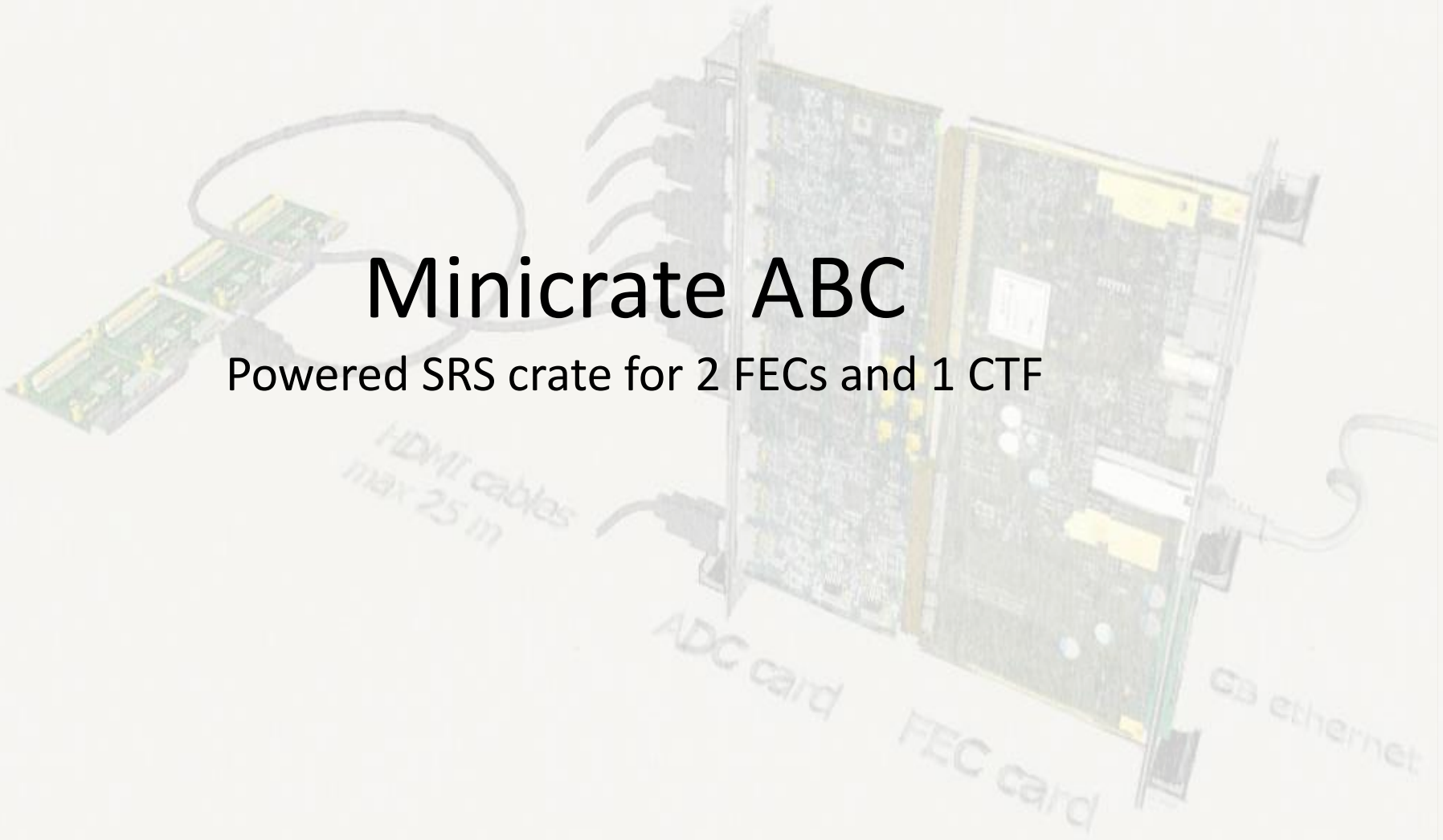
Ext/Int/Man Trigger

Ext/Int clock
differential LVDS

8 x XTCX links (clock and trigger) to FECs
(requires short CAT6 cables)

Minicrate ABC

Powered SRS crate for 2 FECs and 1 CTF

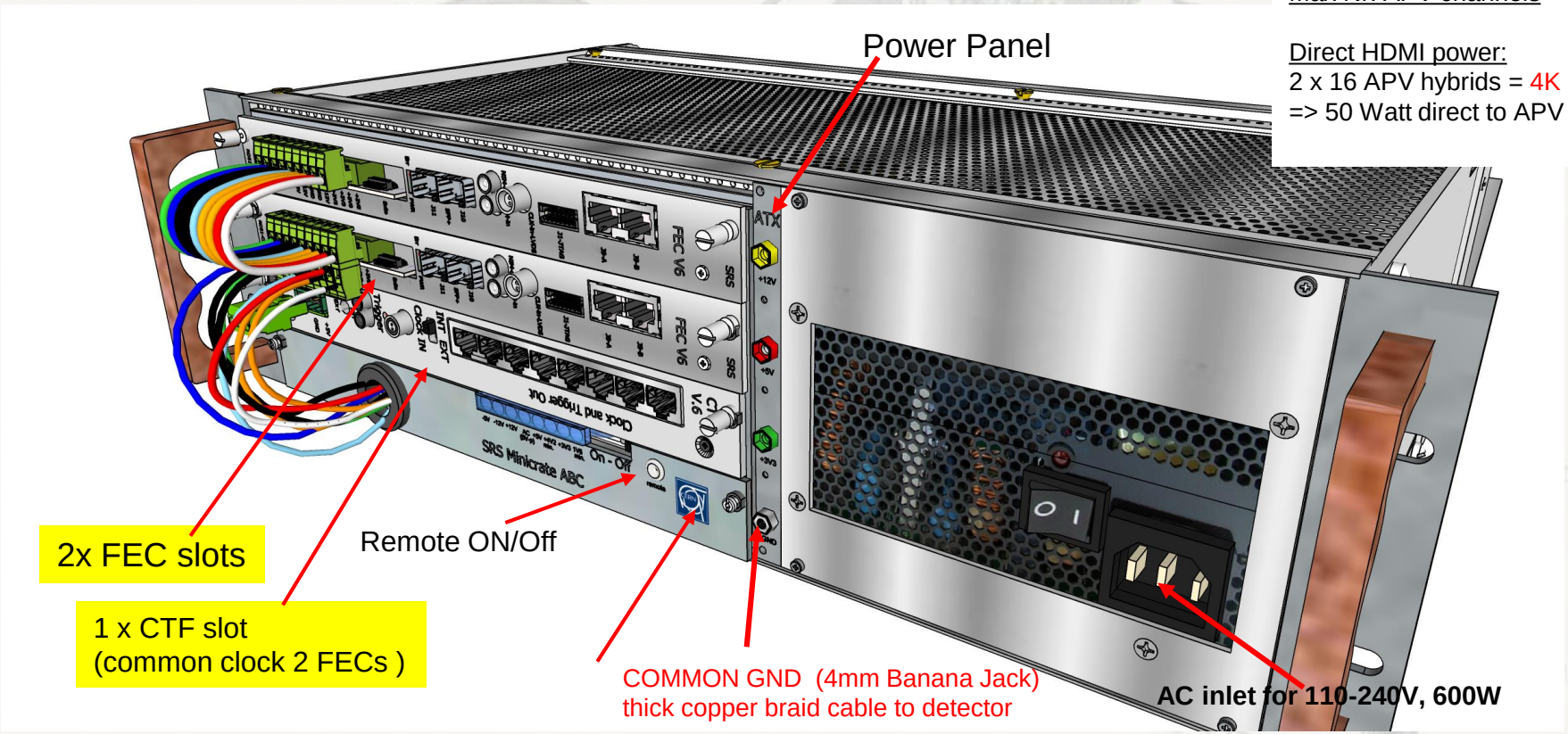


Minicrate ABC (APV frontend)

slots for 2 FEC + 2 ADC, 1 CTF and direct HDMI power for APV

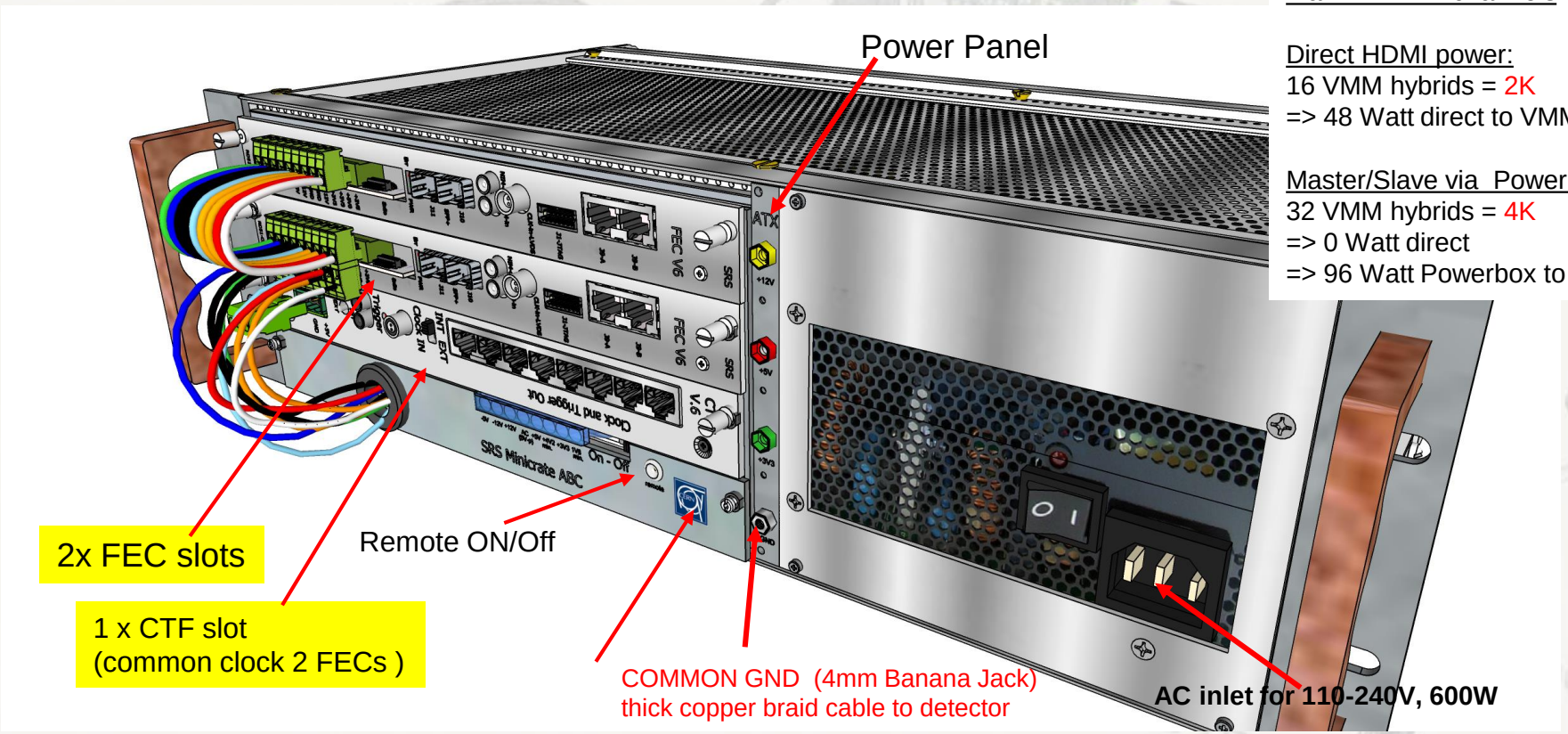
Max Nr. APV channels

Direct HDMI power:
2 x 16 APV hybrids = 4K
=> 50 Watt direct to APV



Minicrate ABC (VMM frontend)

slots for 2 FEC + 2 DVM, 1 CTF and direct HDMI power for VMM

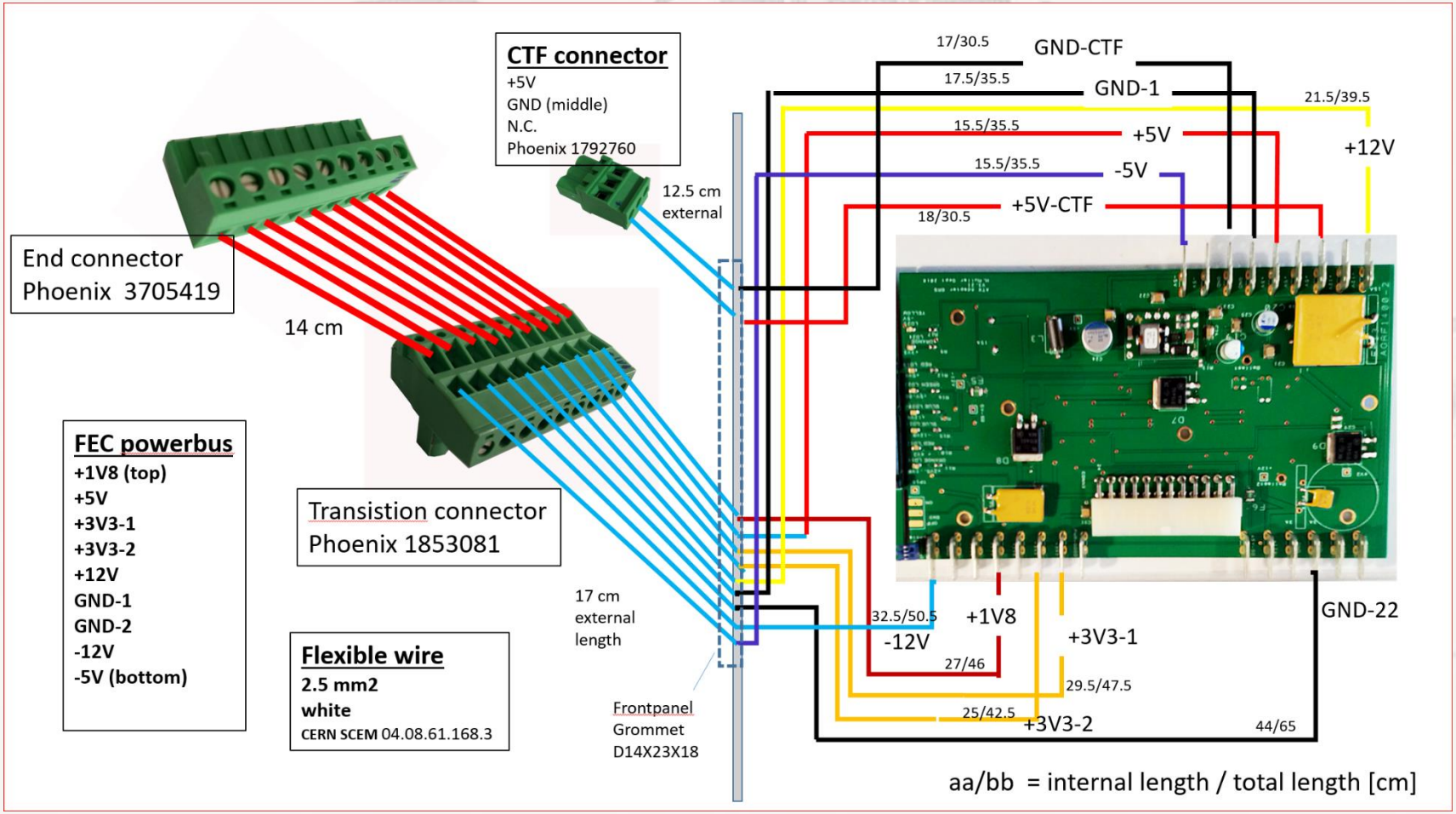


Max Nr. VMM channels

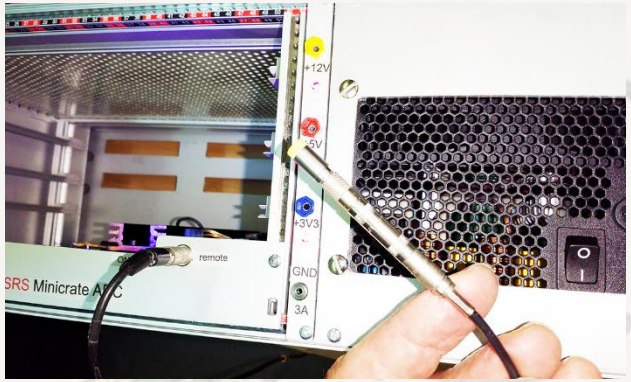
Direct HDMI power:
16 VMM hybrids = 2K
=> 48 Watt direct to VMMs

Master/Slave via Powerbox
32 VMM hybrids = 4K
=> 0 Watt direct
=> 96 Watt Powerbox to VMMs

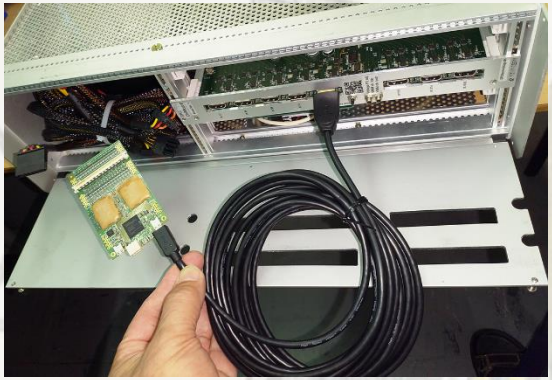
New ATX card wiring
(inside all new SRS crates)



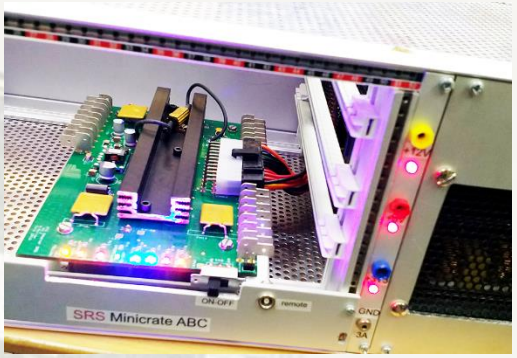
New Minicrate ABC features



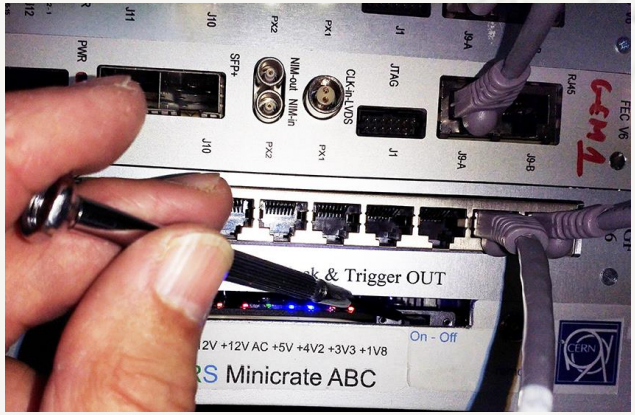
remote ON/OFF/RESET via coax cable



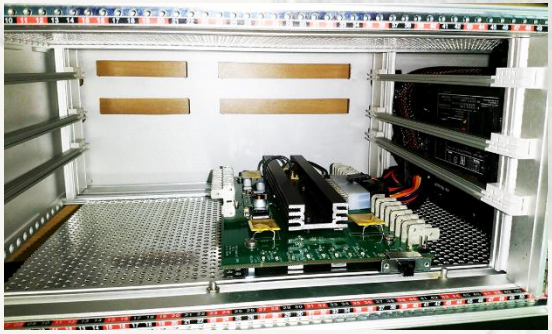
backside swingdoor and standoff feet



New power access panel and
Status LEDs

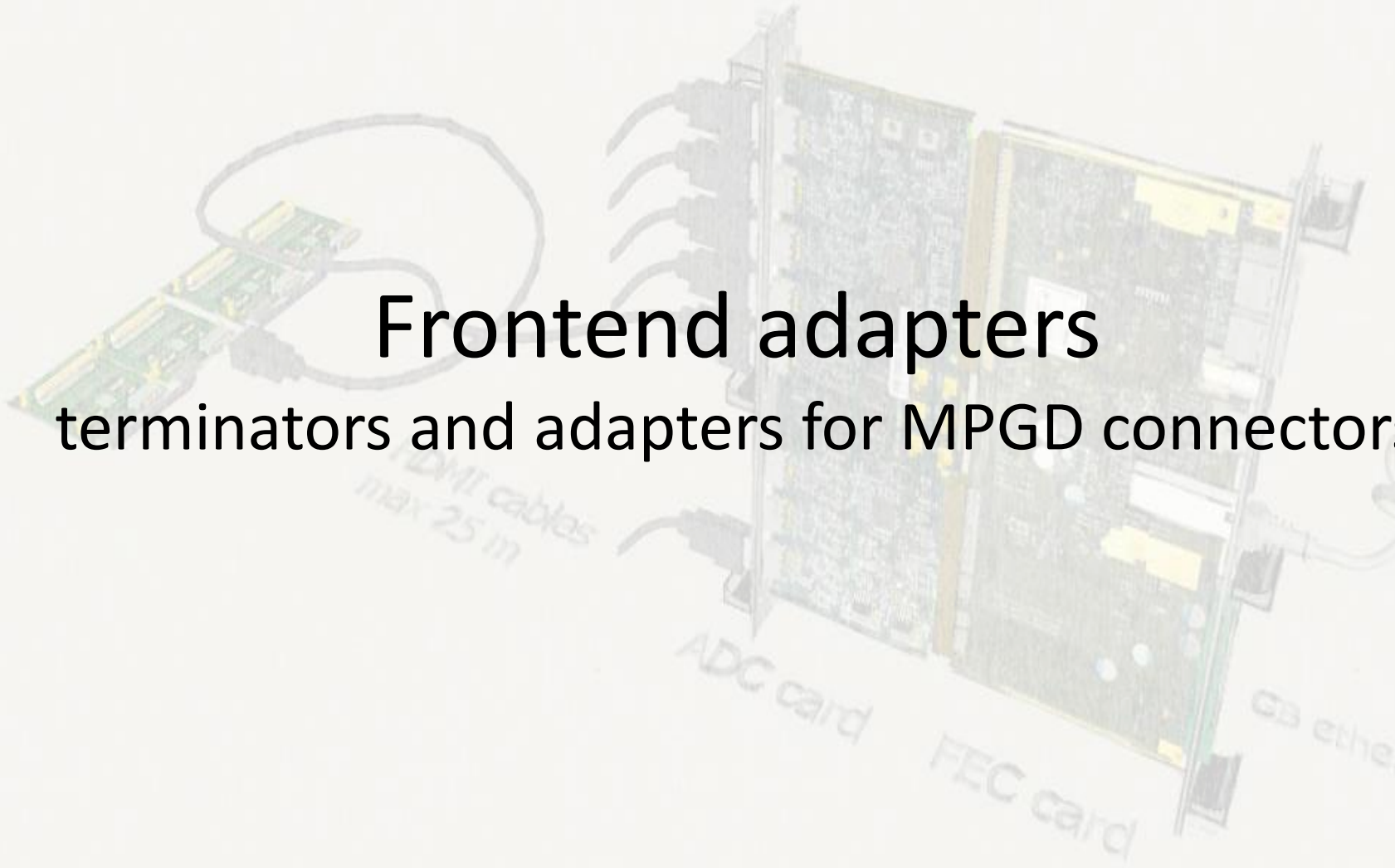


local ON/OFF/RESET switch



3 slots (bottom = CTF)
due to new low-profile ATX adapter

CTF slot and CTF power connector

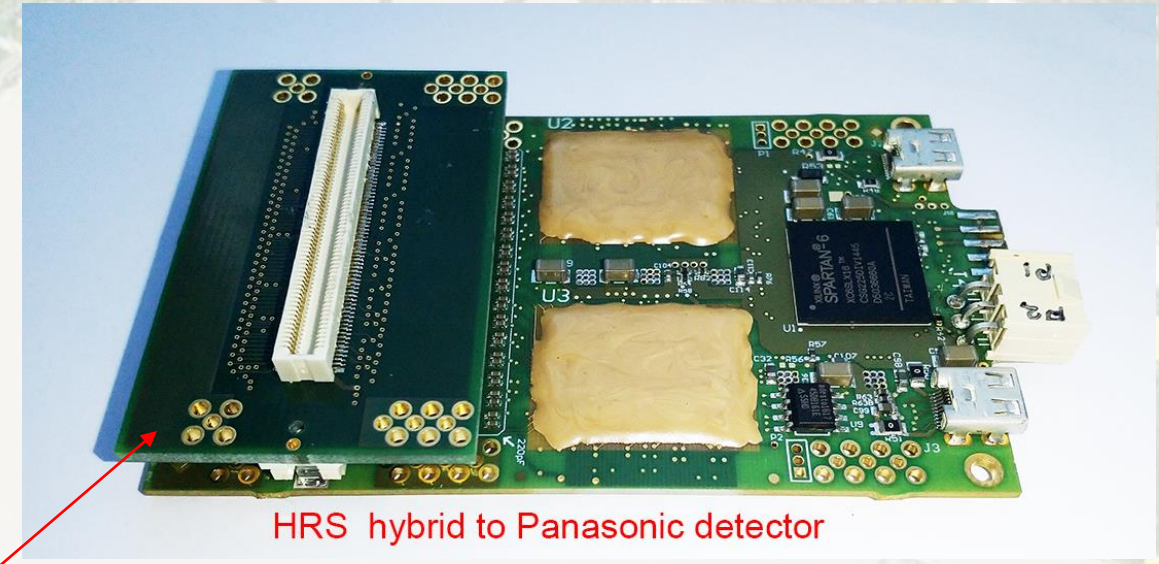


Frontend adapters

terminators and adapters for MPGD connectors

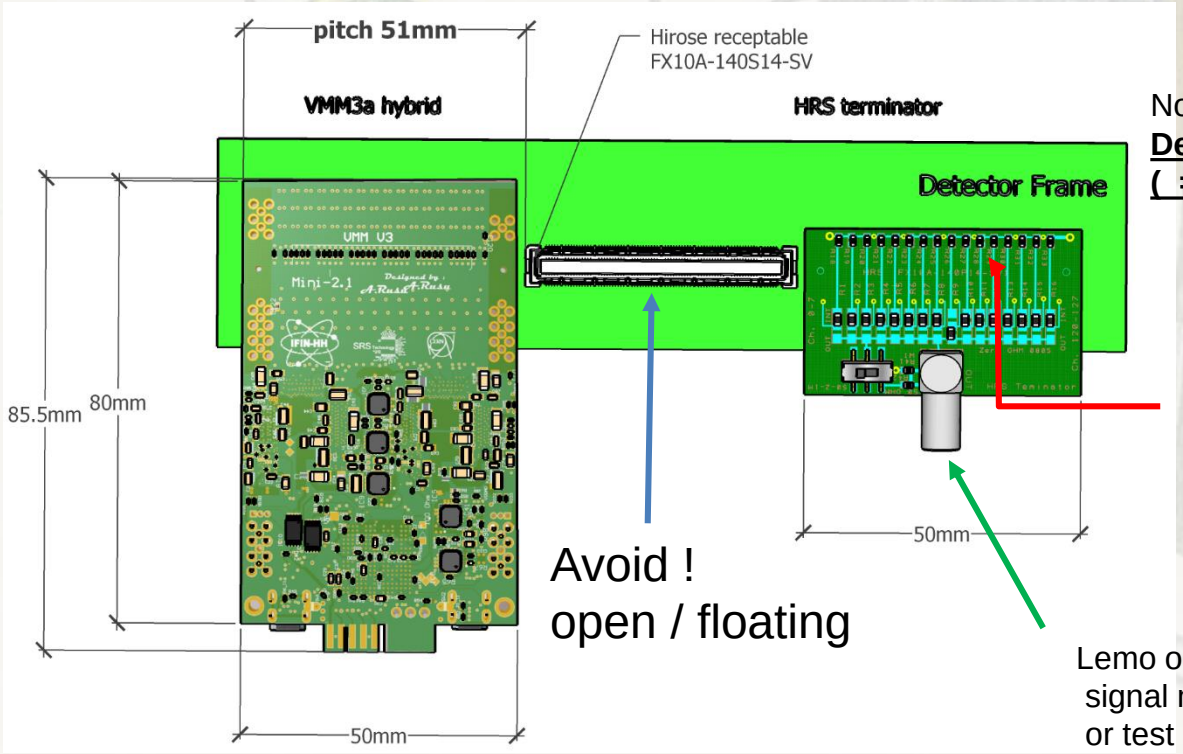
Adapter VMM hybrid (HRS) to legacy Panasonic detector

Credits: A. Rusu



Revised adapter version 1: correct neighbor sequence 2: fits with cooler plate

terminators for unused HRS slots on detector frames



Note: **Exact pitch of HRS connectors on Detector frames is 51.2 mm (= 128 x 0.4 mm detector strips)**

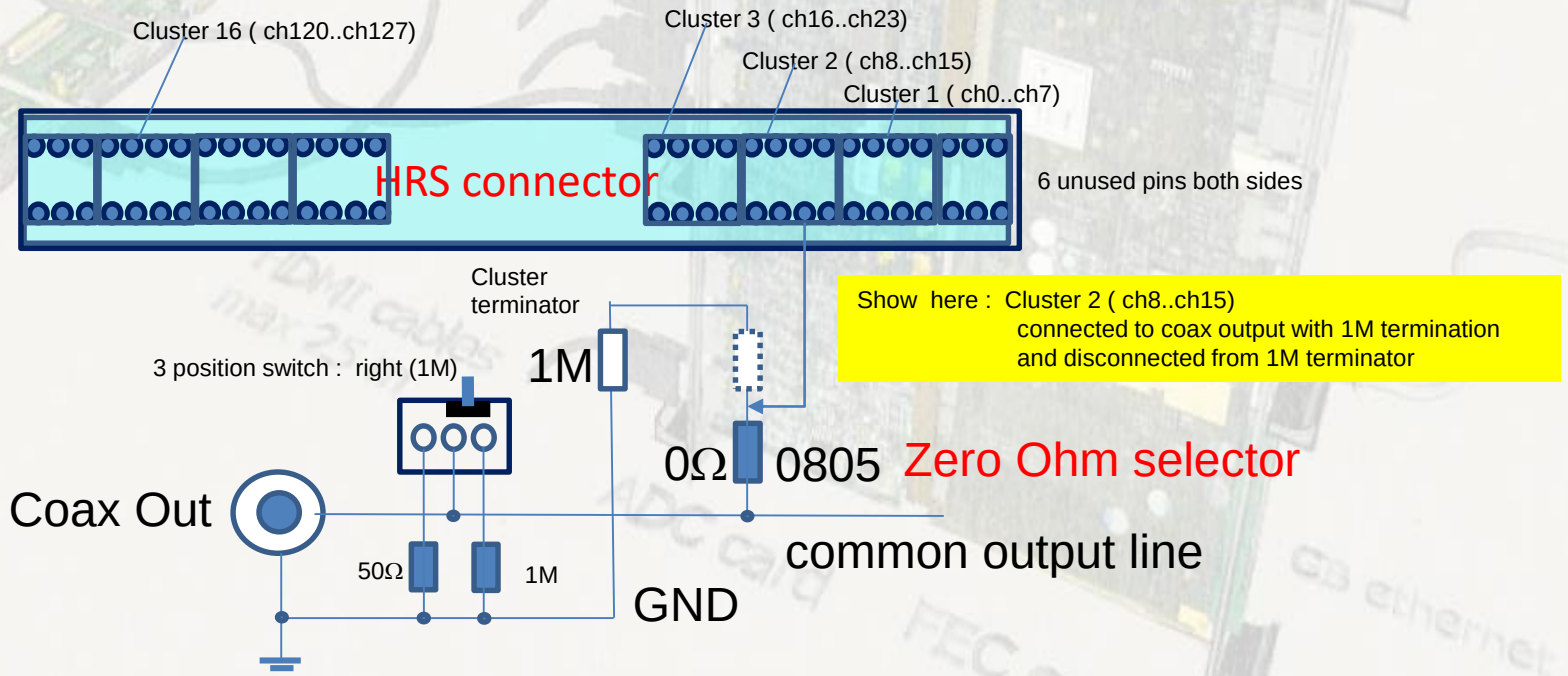
Plugged HRS terminator = defined GND potential on octal channel clusters (1M to GND)

Lemo option to select cluster(s) for signal monitoring with 1M or High Z termination or test pulse injection

TRS terminator configuration Example:

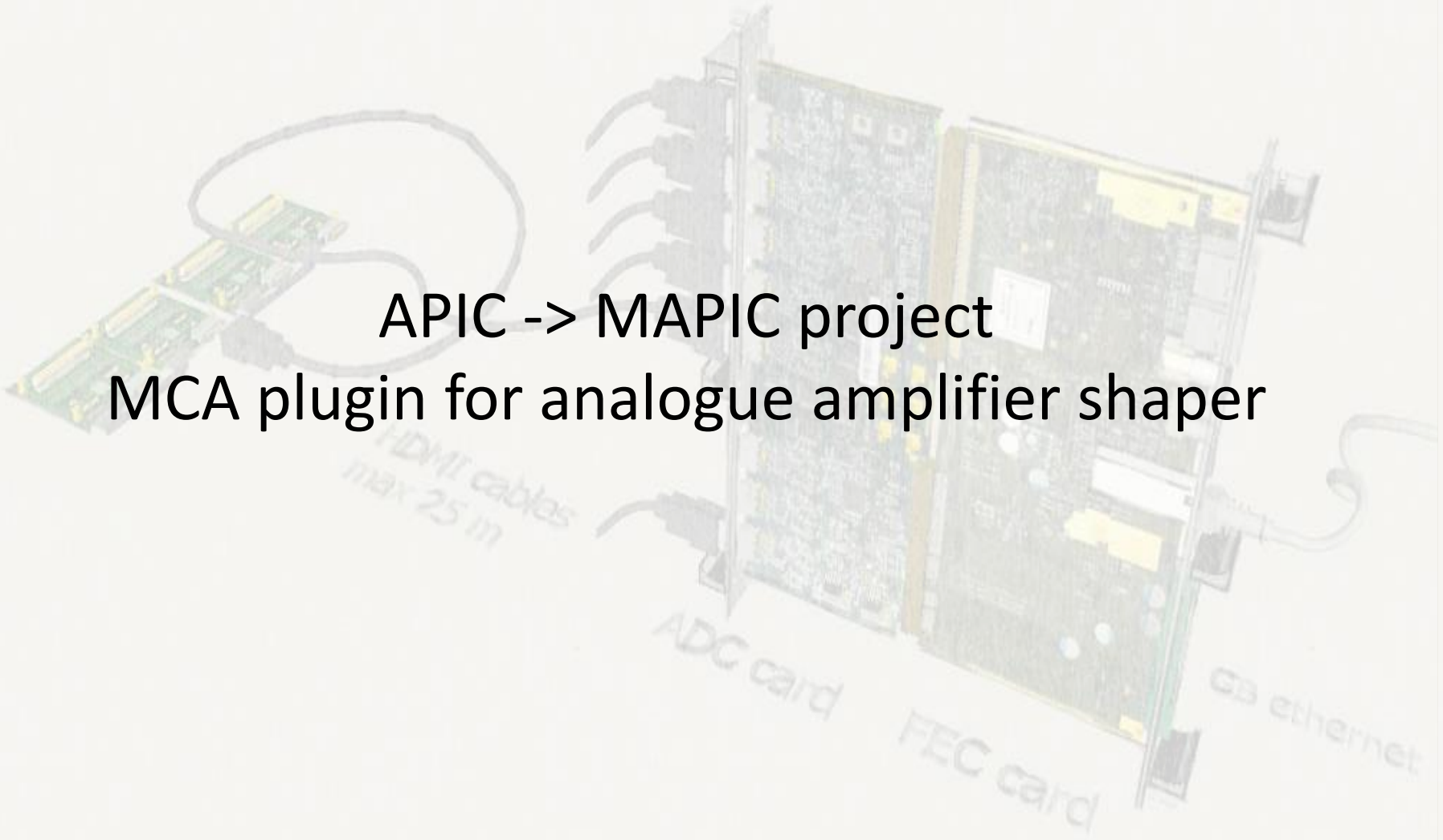
channel cluster 2 ➔ Coax out (1MΩ)

all other channels ➔ 1M term. to GND



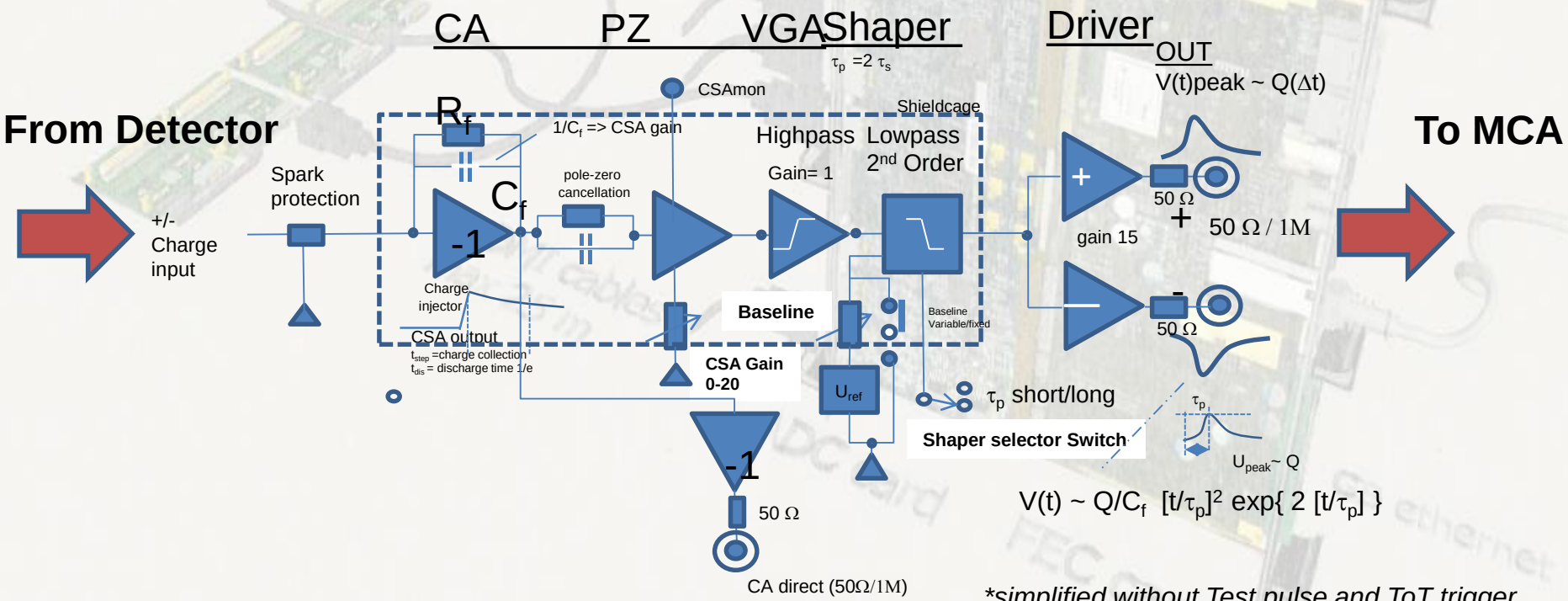
HRS Terminators on NMX detector

Credits: Jerome Samarati



APIC -> MAPIC project
MCA plugin for analogue amplifier shaper

APIC box: preamplifier-shaper chain*



**simplified without Test pulse and ToT trigger*

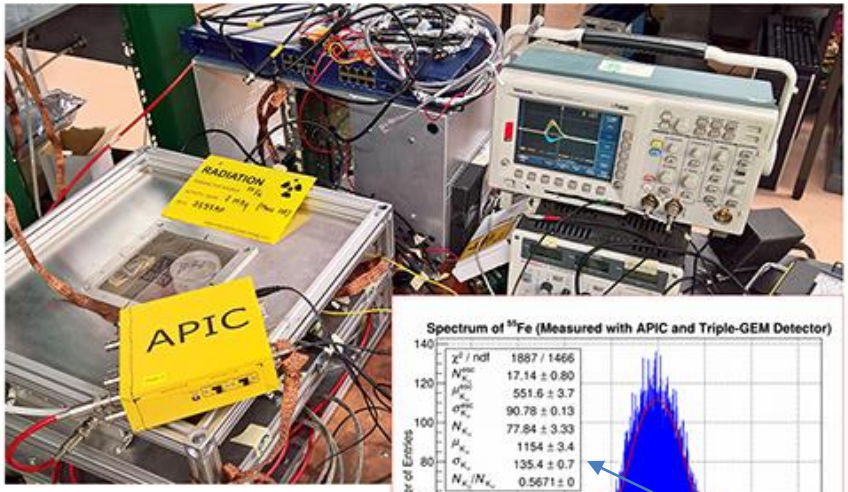
APIC manual: Miniweek Feb. 2018
https://indico.cern.ch/event/702782/contributions/2900690/

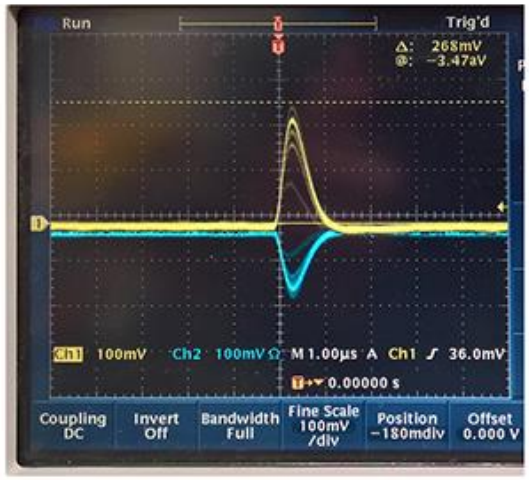
APIC 2017

Add a wireless MCA (Multi Channel Analyzer) function to the yellow APIC box

AIDA 2020 Advanced European Infrastructures for Detectors at Accelerators

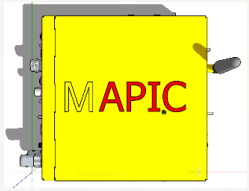
Bottom GEM signal pickup (2017 APIC V3)





Fe55 histogram produced by APIC yellow box
with an external, commercial MCA

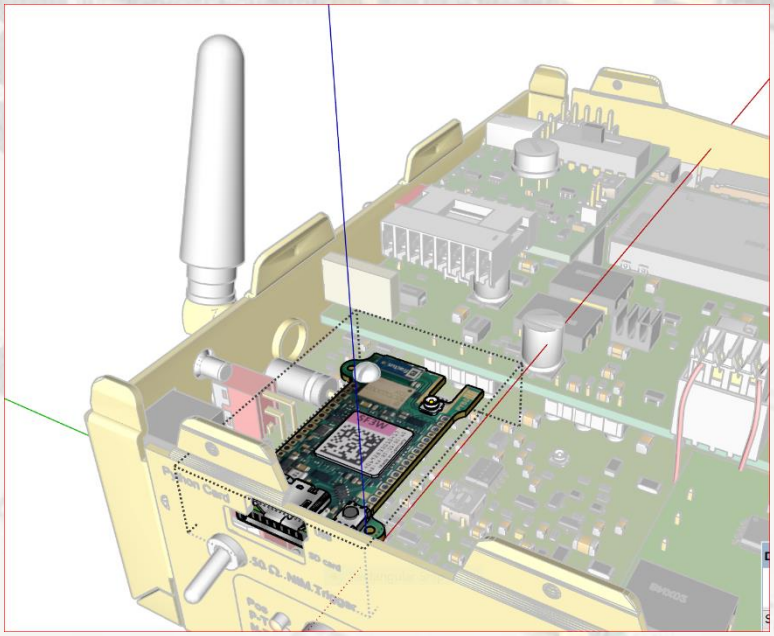
29/04/2019 2018 -APIC V4.x REV. HM017032018



2019 upgrade project APIC => MAPIC
summer student project: MCA card integration inside APIC box

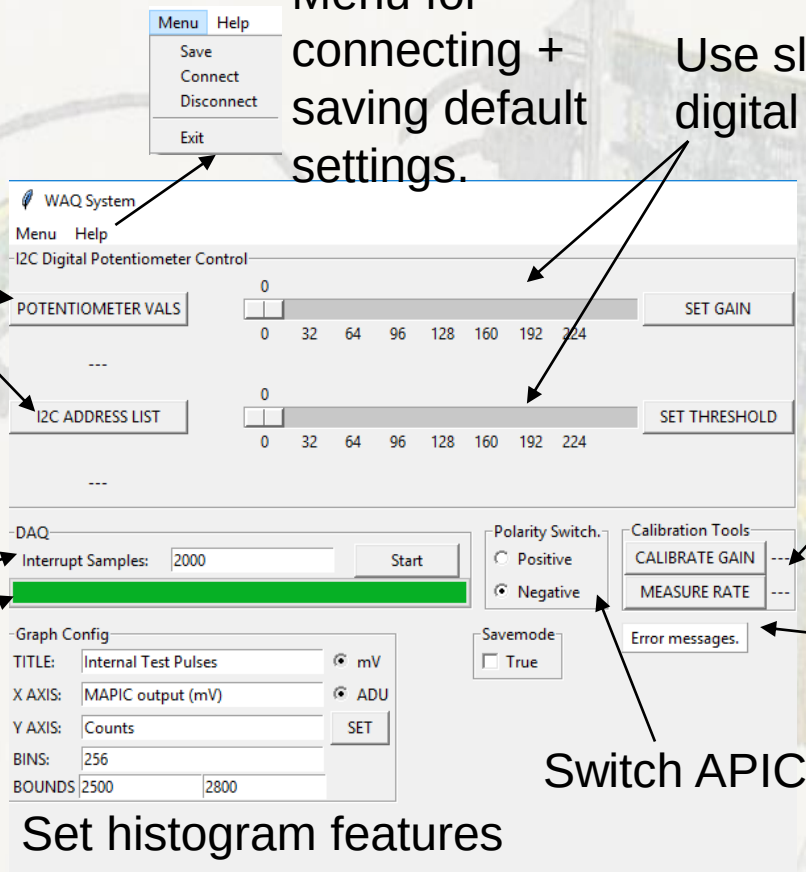
MAPICs is implemented as plugins to the existing APIC

- Python D card (PYBD) STM32F..
- Python D carrier debug/plugin card
- Peak stretcher card (PSC)
- Rainbow cable (PYBD to PSC)
- Wifi Antenna with coax cable



Major software effort completed:
Micro-Python, C-lang, MCU libraries
Python network sockets,
Tinker GUI, Matplotlib

TKinter GUI for MAPIC



Menu for connecting + saving default settings.

Use sliders to set value of the digital potentiometers.

Read digital potentiometer values/addresses on the pulse stretcher via I^2C

Measure rate of pulses + get calibration equation.

Up to 64-bit number of samples from ADC + progress bar

Error messages displayed here

Switch APIC polarity

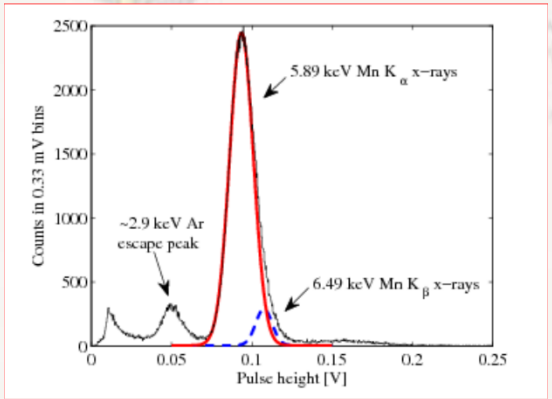
Set histogram features

^{55}Fe Spectrum with MAPIC (wireless)

100,000 samples at a rate of 2kHz. Large number of samples cut into overflow.

What would we expect:

Ahmed, Z. et al. JINST 9 (2014) no.01, P01009 arXiv:1307.6154



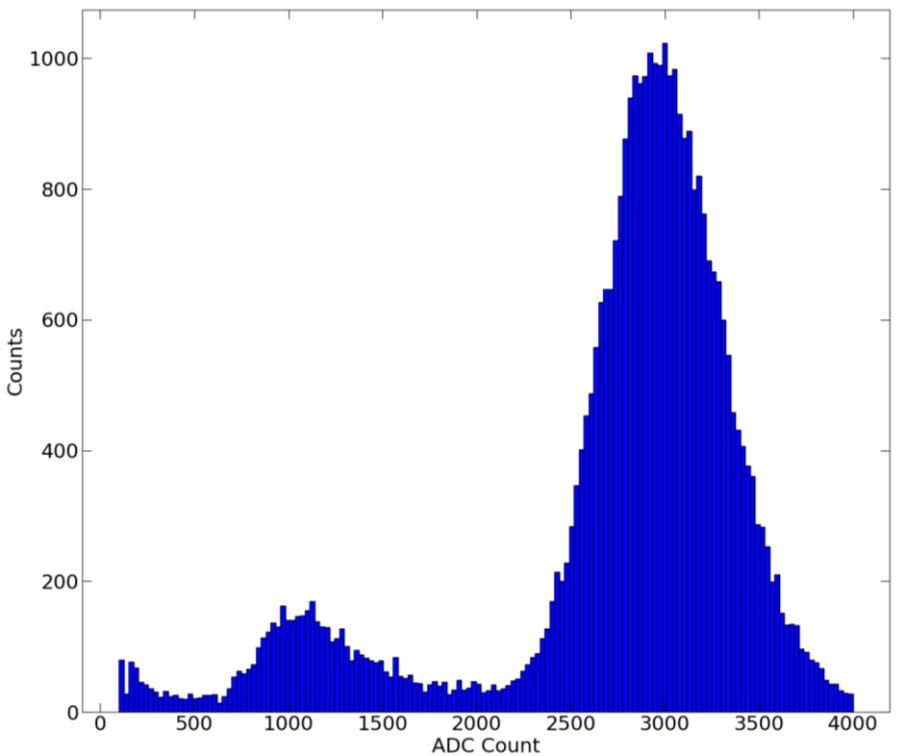
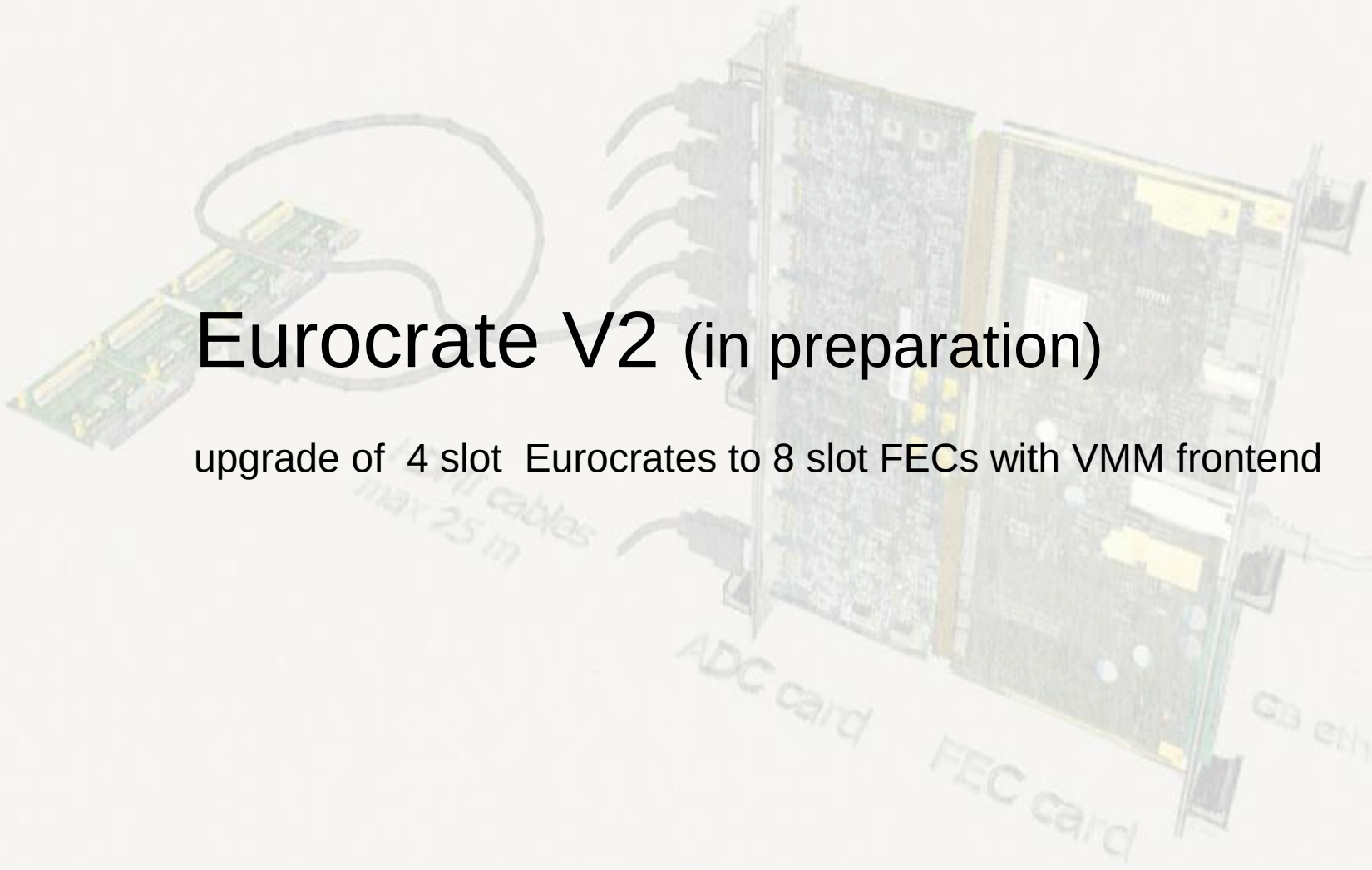


Figure 3: ADC count vs number of counts for ^{55}Fe measured with GEM detector.

MAPIC Project to be continued/ finalized in 2020. All APICs in production now will Be prepared for MAPIC plugin.
Full talk on MAPIC by summerstudent Ryan Griffiths see
https://drive.google.com/open?id=15KHmR0vd-AxUYe12keT9Q9PIRdPeNenS

Eurocrate V2 (in preparation)

upgrade of 4 slot Eurocrates to 8 slot FECs with VMM frontend

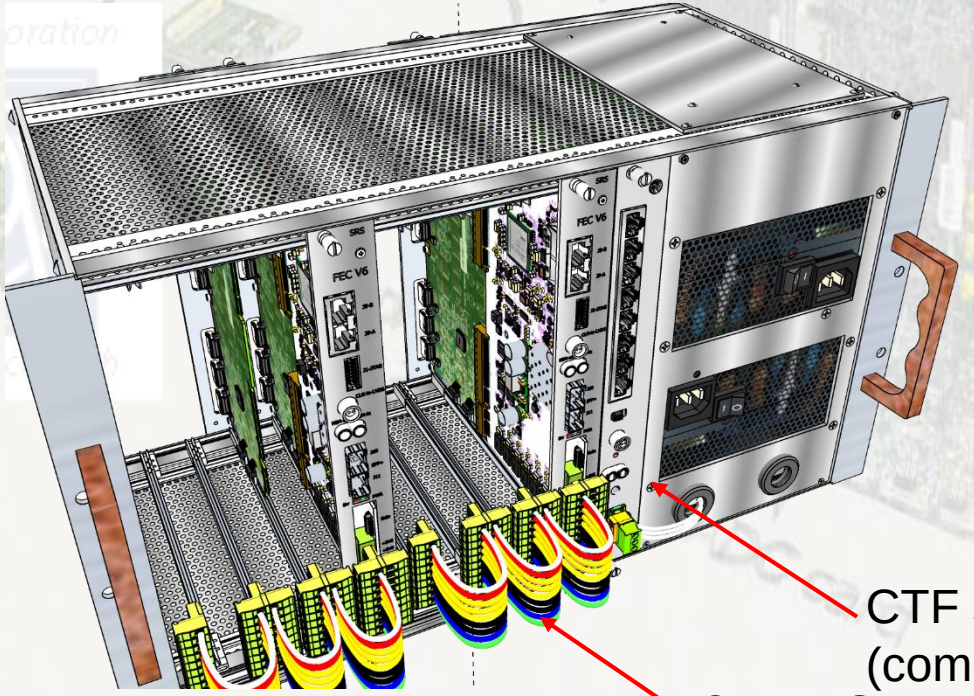


Eurocrate V2

for up to 8 FEC+DVM, 1 CTF and direct HDMI power for VMM

DVMcards inserted from backside

Remote ON/Off on Power backpanel



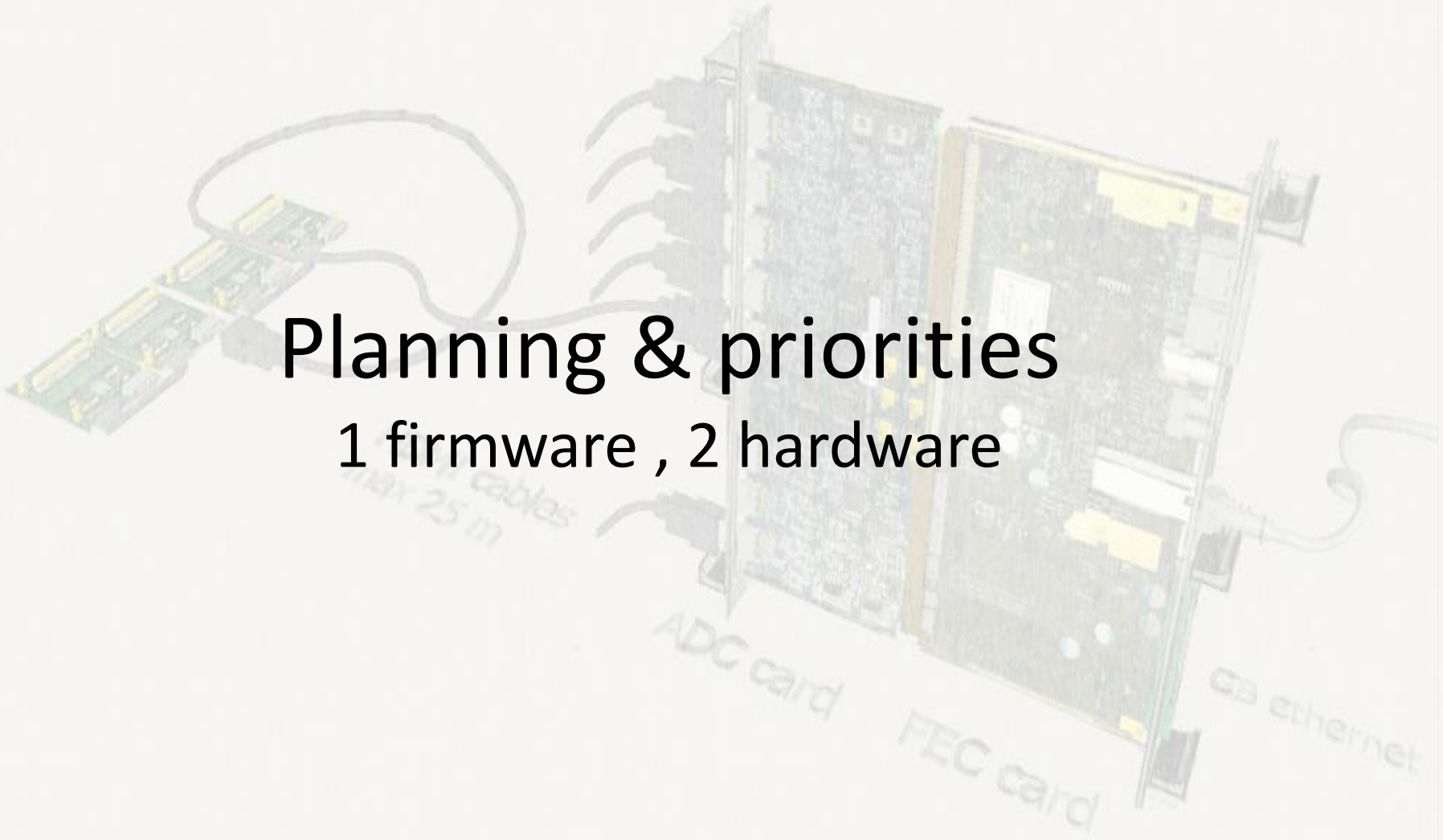
CTF slot
(common clock & trigger up to 8 FECs

8 x FEC
slot

Max Nr. channels

Direct HDMI power:
64 VMM hybrids = 8K
=> max. 192 Watt direct to VMMs

Master/Slave via Powerbox
128 VMM hybrids = 16K
=> 0 Watt direct
=> max. 384 Watt Powerbox to VMMs



Planning & priorities

1 firmware , 2 hardware

1 Firmware to enhance SRS-VMM systems

To-do list FW (draft):

1.) add configuration readback (**system stability**)

2.) add powerup default configuration from ID-Prom (**user friendliness**)

3.) add VMM serial number readback from new ID chip **(tracability)**

4.) add Fast-OR (ART) transmission to Powerbox->FEC **(level-0 Trigger gen.)**

5.) stablilize readout at highest trigger rates (**stable operation up 1 MHz /ch**)

6.) add Master-Slave, readout mode (**2 x No of channels per FEC = 2 x BW**) 1st phase

7.) improve uplink to match 2x320 Mbps rate of VMM (**2 x BW**)

8.) add geographic position readout **(detector consistency)**

9.) add Atlas (non-continuous) trigger mode (**32 bit data frames, higher BW**)

10.) implement spill-buffer mode (**4x trigger rate to DDR3 buffer in FEC**) 2st phase

2 HW for high-rate VMM systems

To-do list HW (draft):

1.) launch Powerbox 2k (**master-slave mode 2x BW**)

2.) add geo. chip to next revision (goes with FW point 8)

3.) add " bad VMM" jumpers (declassified **64 channel hybrids**)

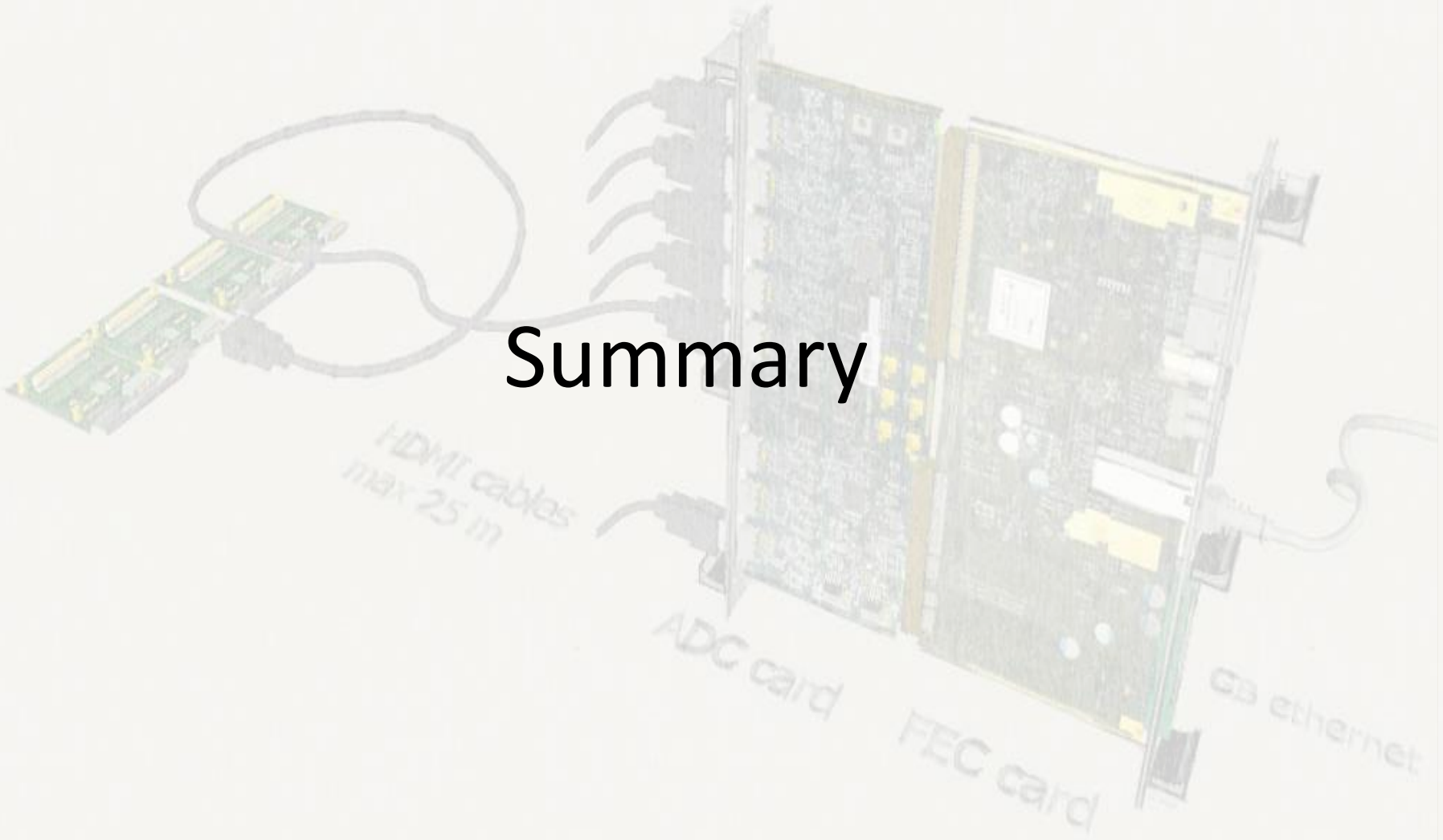
4.) upgrade hybrid from Spartan-6 FPGA to 'state-of-art" FPGA

-> (**higher rate, higher radiation immunity, better support**)

6.) upgrade VMM hybrid components (i.e. LDO's) to higher radiaton levels

(**high radiation frontends**)

Summary



SRS transition to VMM frontend is almost complete

1. 4th revisions VMM hybrid, 4 years: ready for experiments and users
2. VMM cooling was a big issue: has been solved
3. DVMcard was another big issue: HW and FW are ready
4. New SRS crates, very big Issue: commercialization started, certification may follow
5. MPGD connector transition from Panasonic -> HRS: not easy.

   But HRS is MUCH better
6. Adapters sounded easy (but were not): another critical issue solved
7. MAPIC idea started with low credibility and made a big impact ! lets finalize it properly
8. Priorities for full commissioning of VMM frontend well understood, FW + HW

➔ last mile of SRS –VMM after 4 years: keep fingers crossed !

Thank you !

Doubt is an uncomfortable condition, but certainty is a ridiculous one
François-Marie Arouet (Voltaire)