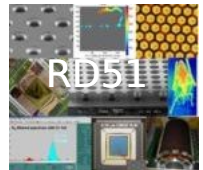
UNIVERSITÄT BONN

GEFÖRDERT VOM
Bundesministerium
für Bildung
und Forschung

VMM and the SRS – update
&
plans in Bonn

Michael Lupberger
(University of Bonn)

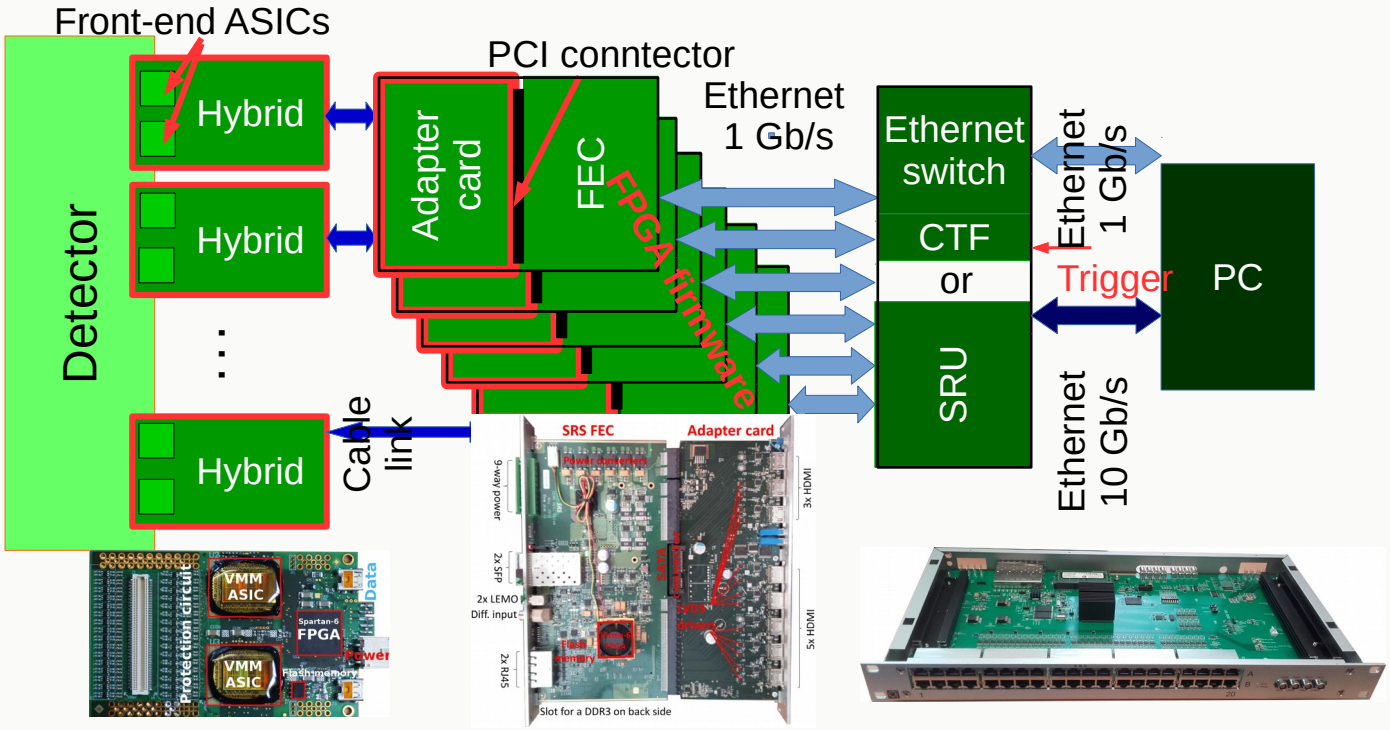
RD51 Collaboration Meeting, CERN
23.10.2019



Introduction: VMM and the SRS

VMM ASIC (developed for ATLAS NSW by BNL) was implemented in SRS
https://doi.org/10.1016/j.nima.2018.06.046

System overview:



Project in transition phase from R&D to production, ongoing activities:

→ final hardware
→ firmware improvements
→ common DAQ software
→ auxiliary services: cooling, powering

Activities in Bonn - overview

New research project NexGRIND at Physics Institite (PI) led by Jochen Kaminski:
Neutron detectors and readout electronics

→ SRS with VMM and Timepix3

→ Continue SRS VMM activities:

- SRS FEC and hybrid Firmware development, support hardware production
- SRS SRU firmware for VMM data
- Need for hardware in our group: O(200) hybrid system for detector development
- Develop cooling for O(200) hybrid detector

→ Continue SRS Timepix3 activities (Markus Gruber's talk)

Interest on VMM for COMPASS tracker upgrade at HISKP (Bernhard Ketzer's group)
Part of my Marie Curie Fellowship GenEl starting early 2020

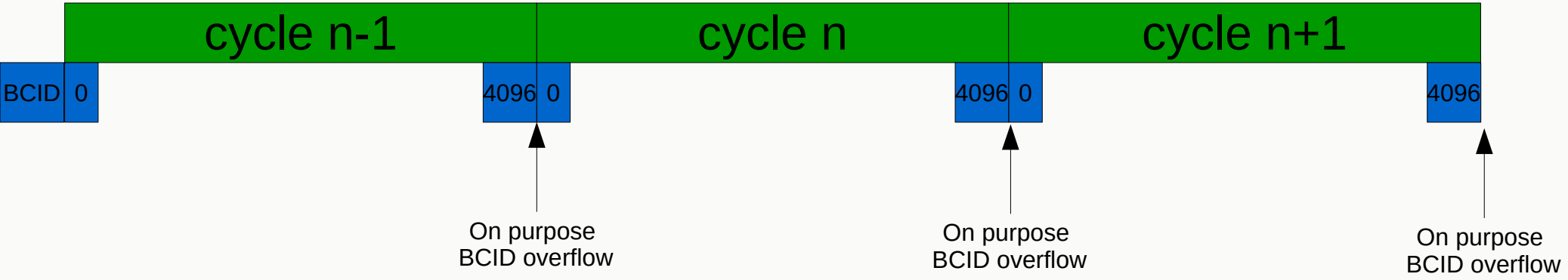
→ SRS with VMM for R&D

- Evaluate noise of VMM and RD51 hybrid in comparison to APV
- Need for hardware: 4(at least) hybrid lab setup

VMM Firmware
Ongoing optimisation

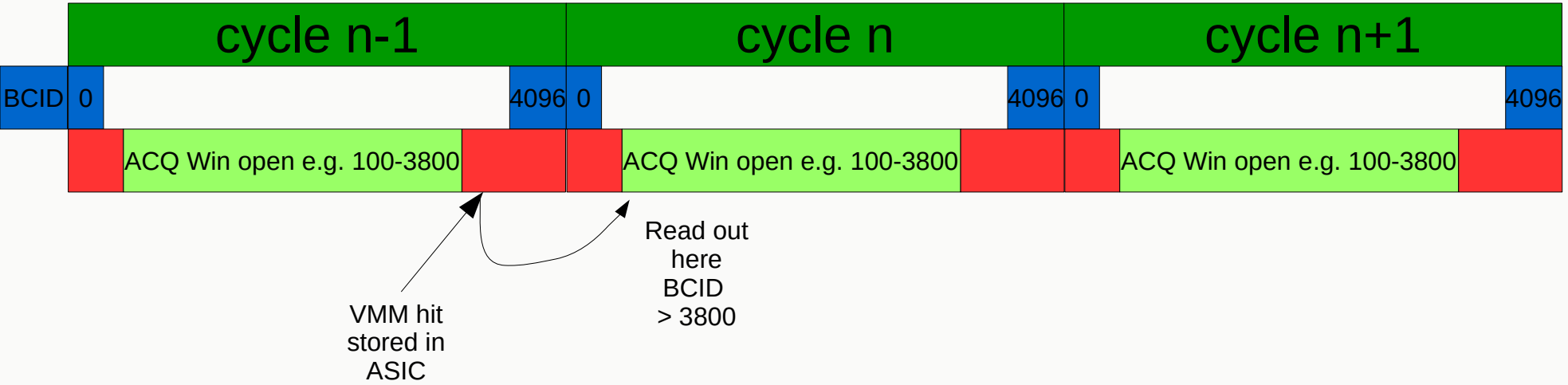
Contineous data taking boundary conditions requires unambiguous time measurement:
Time measurement in VMM: BCID and TDC
TDC: inter BCID cycle time measurment by 8-bit Time To Amplitude Converter (TAC)
→ ok
BCID: 12 bit counter incremented by tunable clock (2.5 MHz – 80 Mhz)
→ overflows after 4096 clock cycles (clk)

⇒ higher order counter needed to keep unambiguous time measurement
→ readout cycle ≤ 4096 clk
Currently: readout cycle = 4096 clk! = BCID overflow



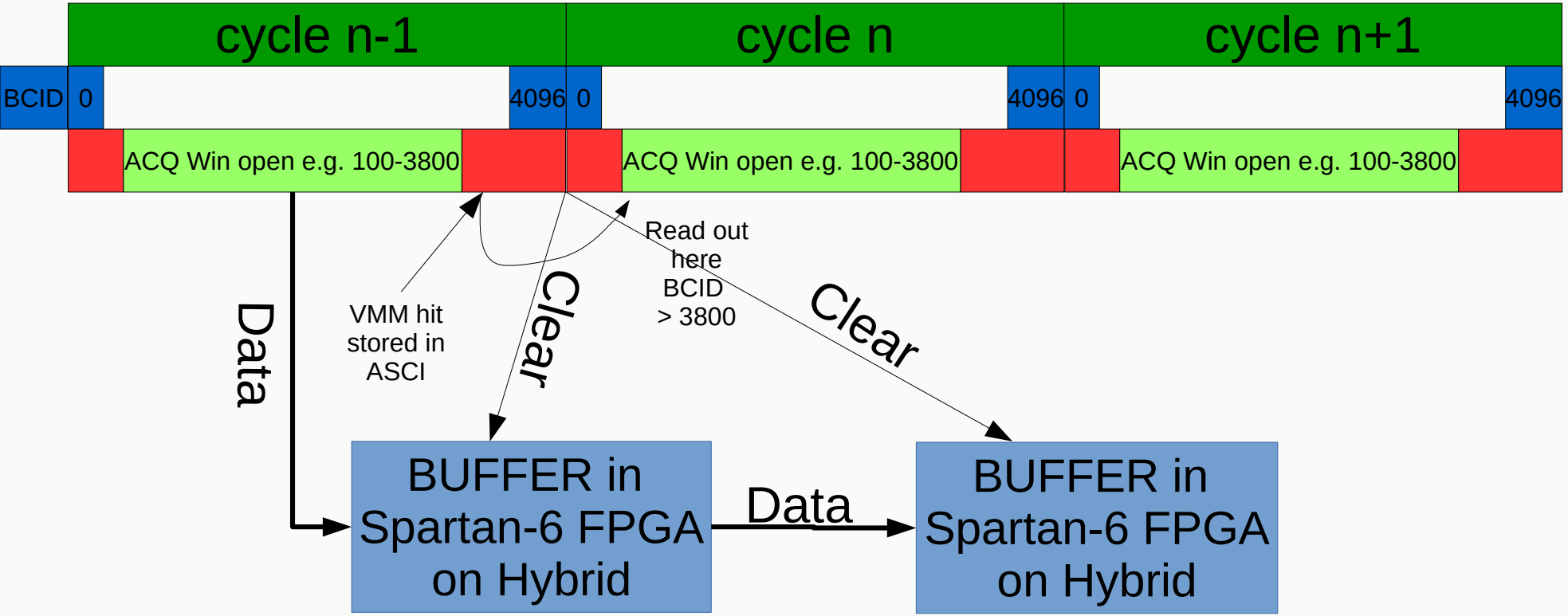
VMM Firmware
Ongoing optimisation

From first safe implementation: remains of sequential data taking:
«Acquisition Window» (ACQ Win): Time when data can be aquired, but not quite:
- VMM is self tirggered, so always aquires data, when enabled
- window generated in firmware, not processing VMM data from outside window
- data forwarding and sending when ACQ Win is closed
- data from end of cycle n-1 could appear in cycle n



VMM Firmware
Ongoing optimisation

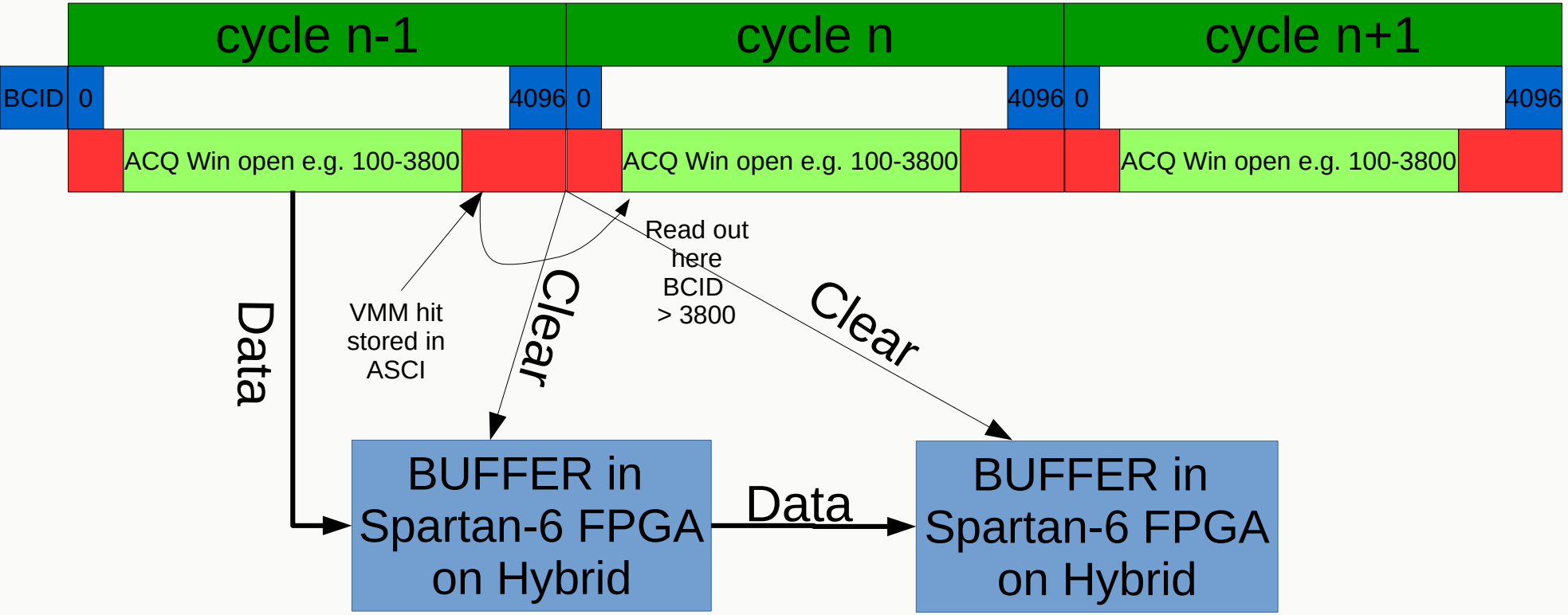
Further problem: Data processing in readout chain



Clear data during processing, to avoid data from cycle n-1 in data from cycle n: does not work

VMM Firmware
Ongoing optimisation

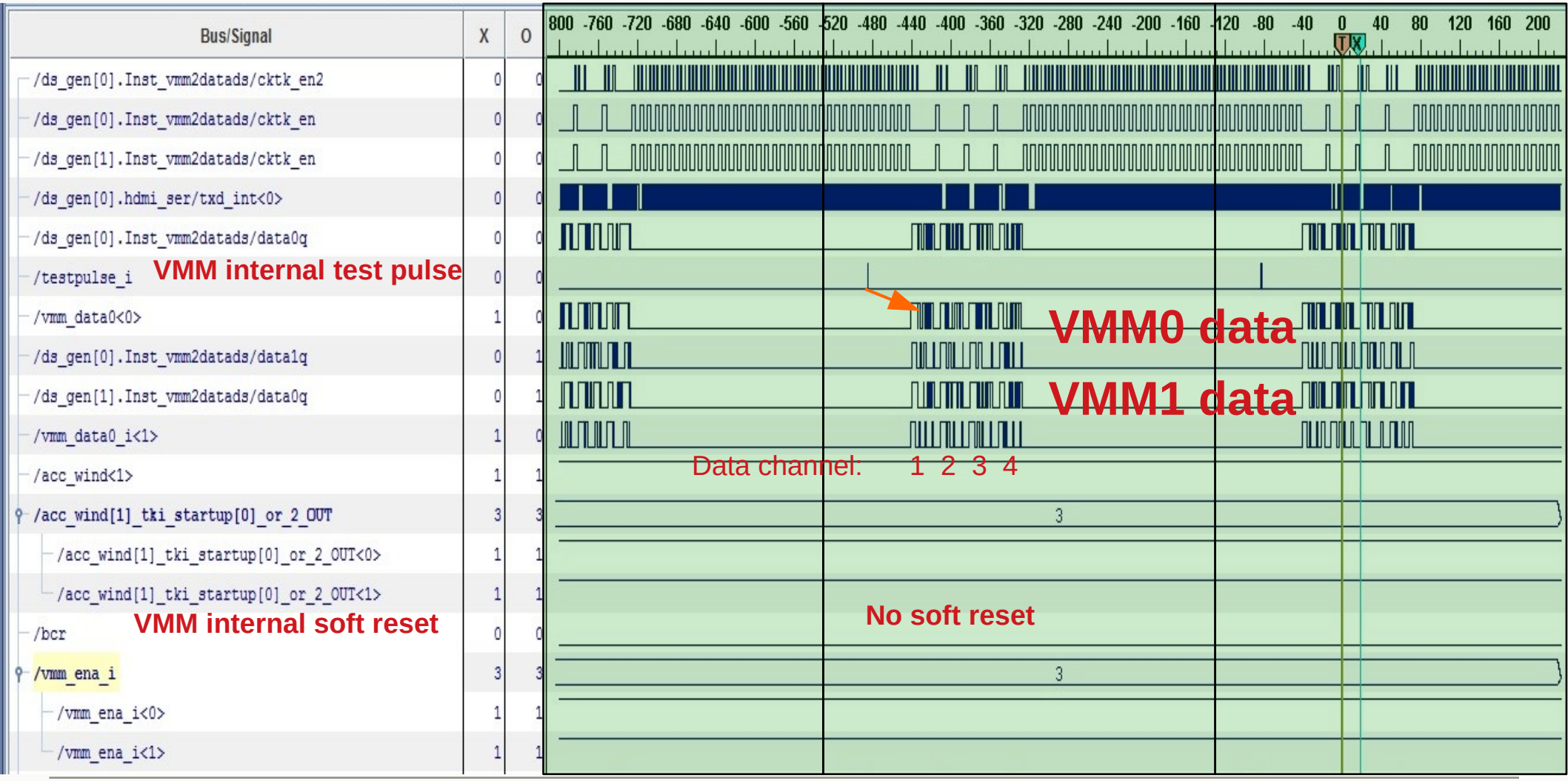
Further problem: Data processing in readout chain



Clear data during processing, to avoid data from cycle n-1 in data from cycle n: does not work → solution: VMM soft reset

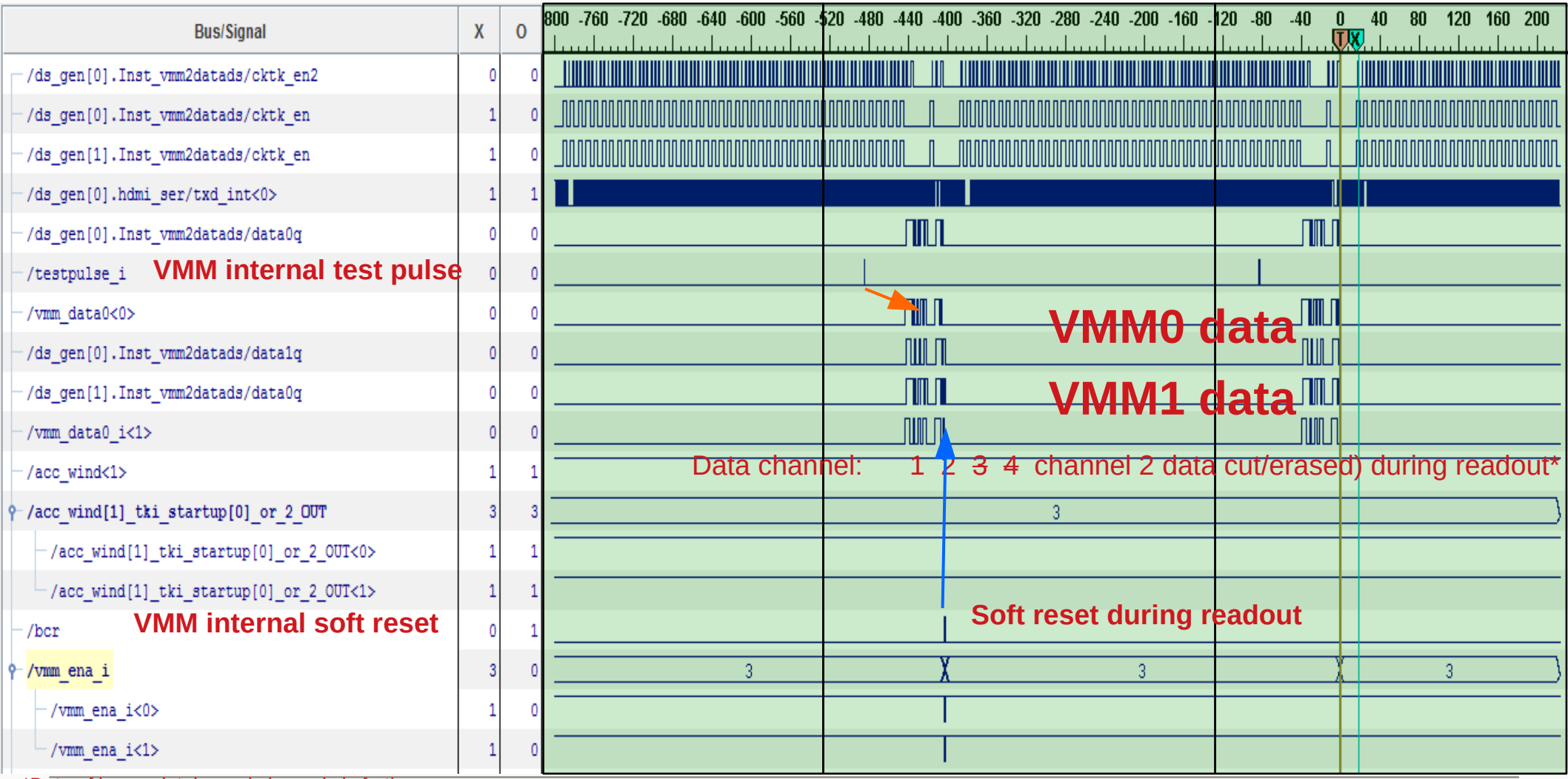
VMM Firmware
Ongoing optimisation

VMM soft reset test: Internal test pulse injected into 4 channels on two VMMs



VMM Firmware
Ongoing optimisation

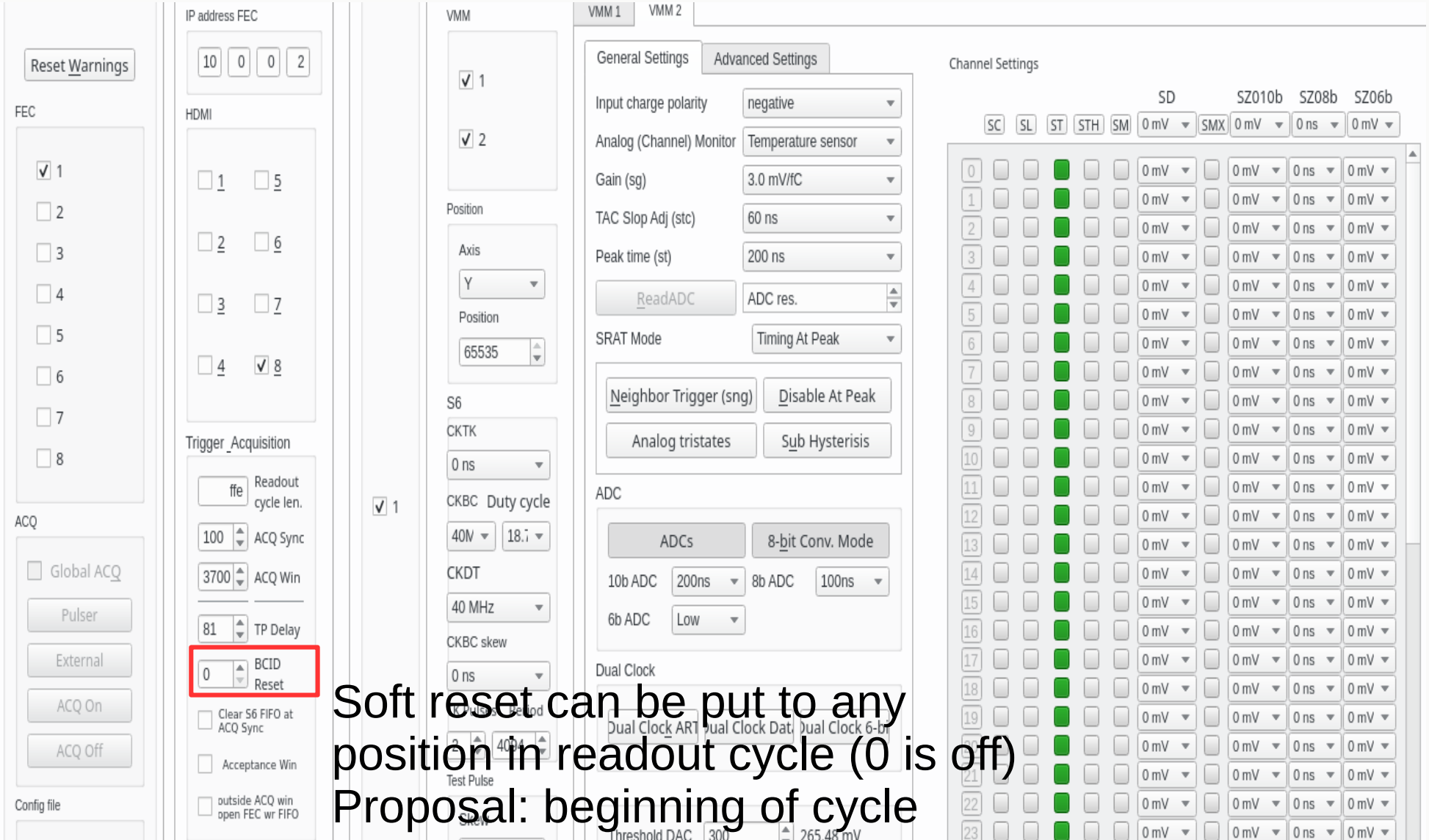
VMM soft reset test: Internal test pulse injected into 4 channels on two VMMs



*Data of incompletely read channels is further processed in firmware (channel 2 in this example)

VMM Firmware
Ongoing optimisation

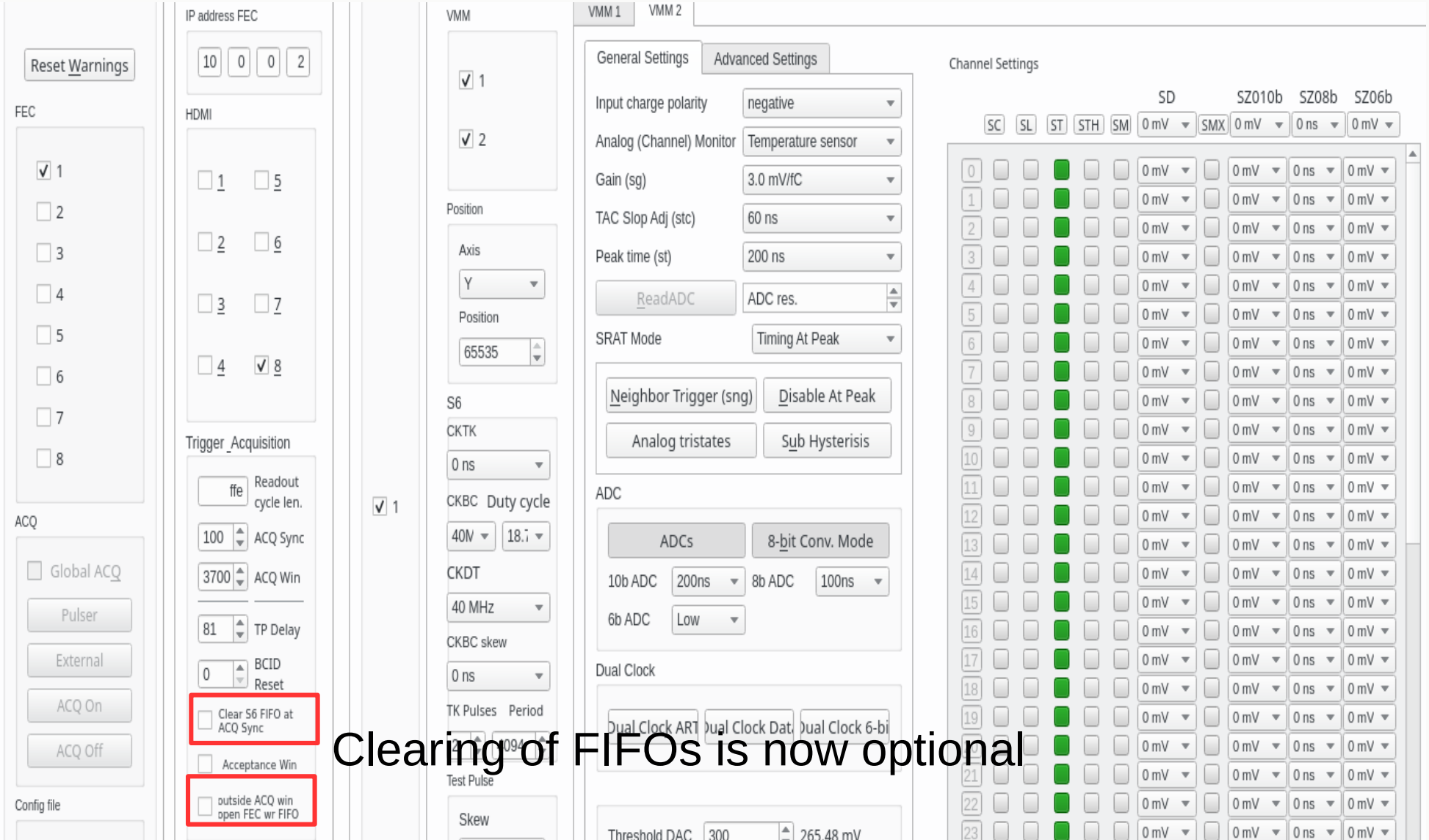
Software implementation of soft reset



Soft reset can be put to any position in readout cycle (0 is off)
Proposal: beginning of cycle

VMM Firmware
Ongoing optimisation

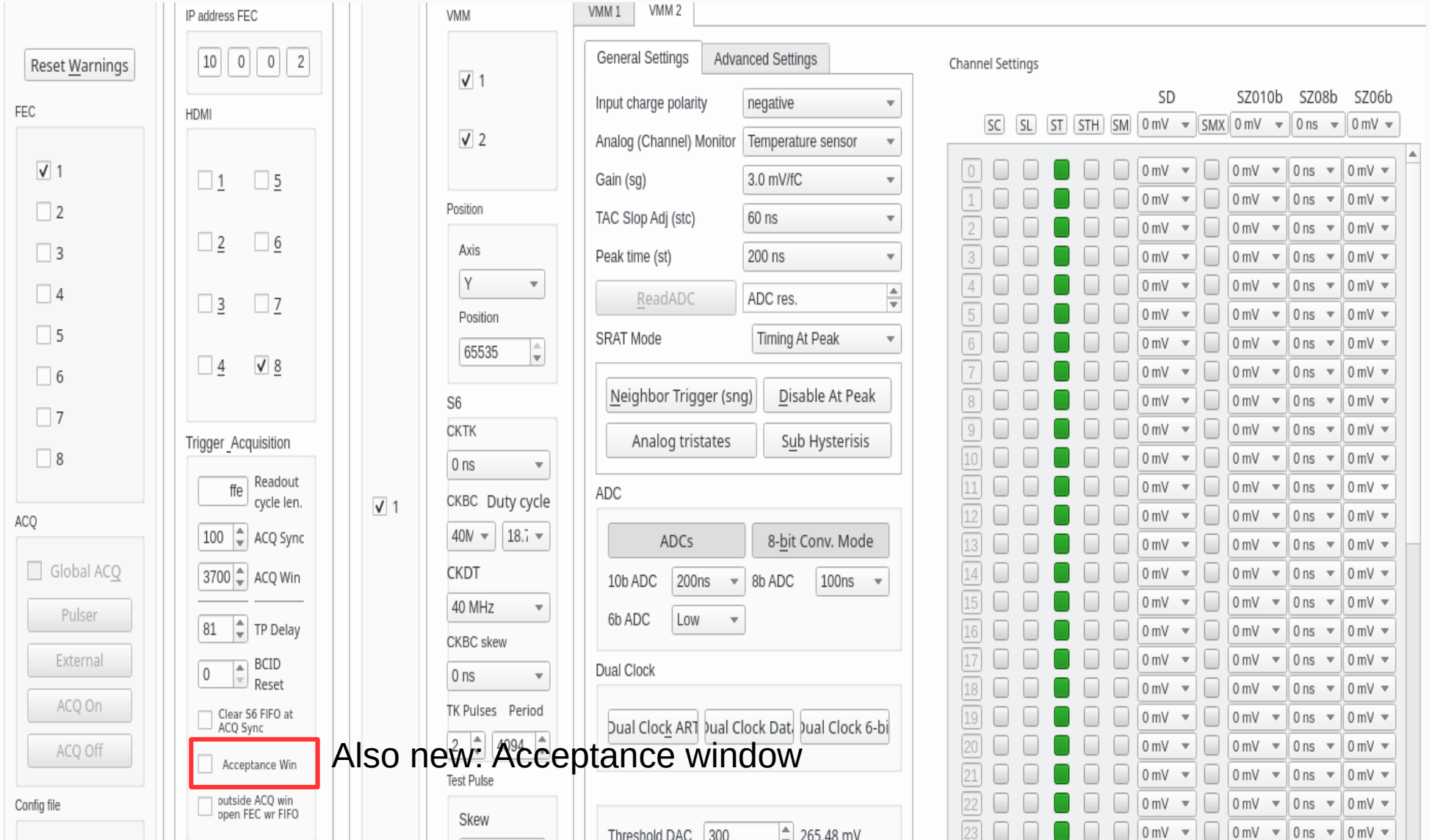
Software implementation of soft reset



Clearing of FIFOs is now optional

VMM Firmware
Ongoing optimisation

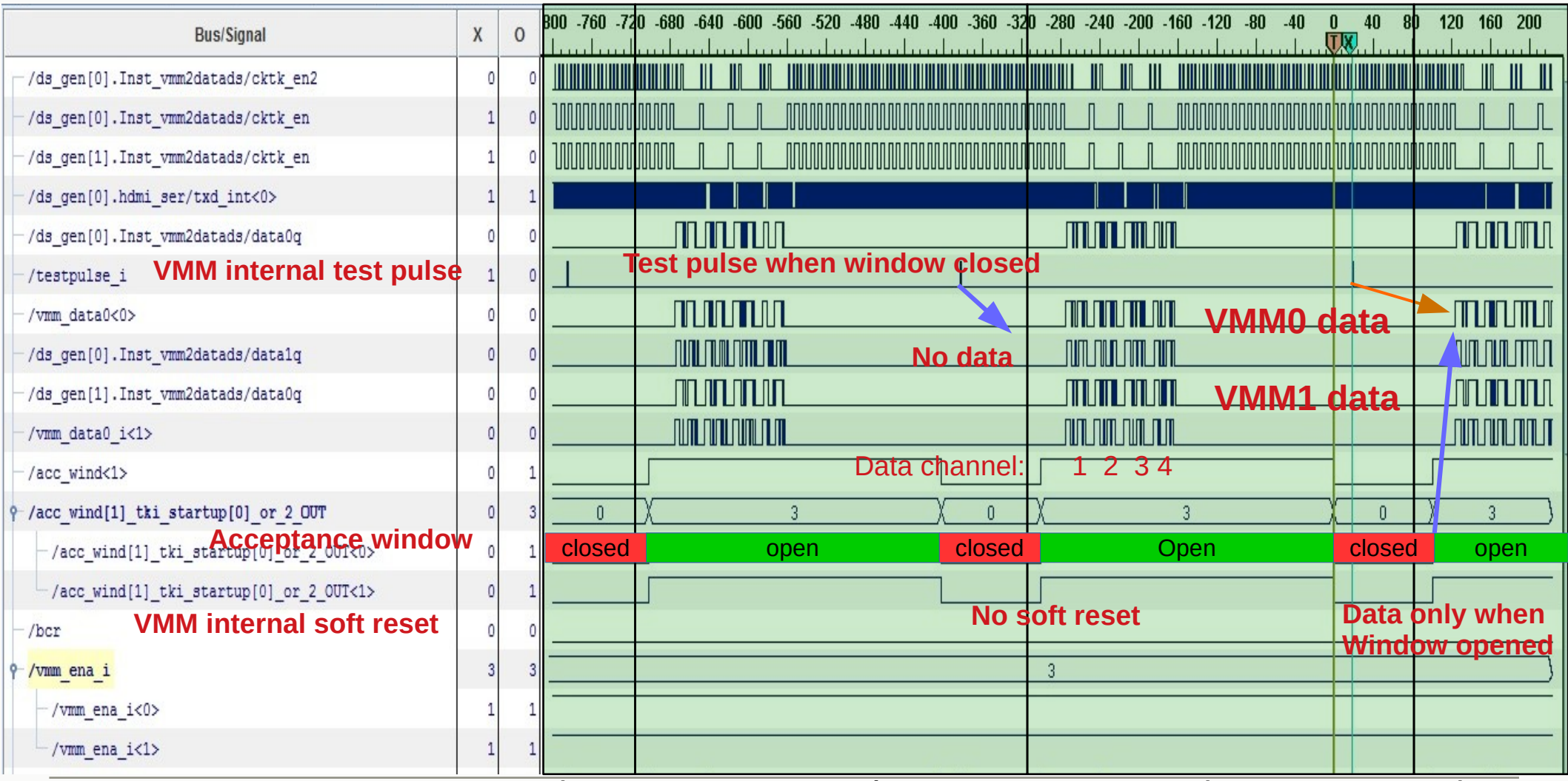
Acceptance window



Also new: Acceptance window

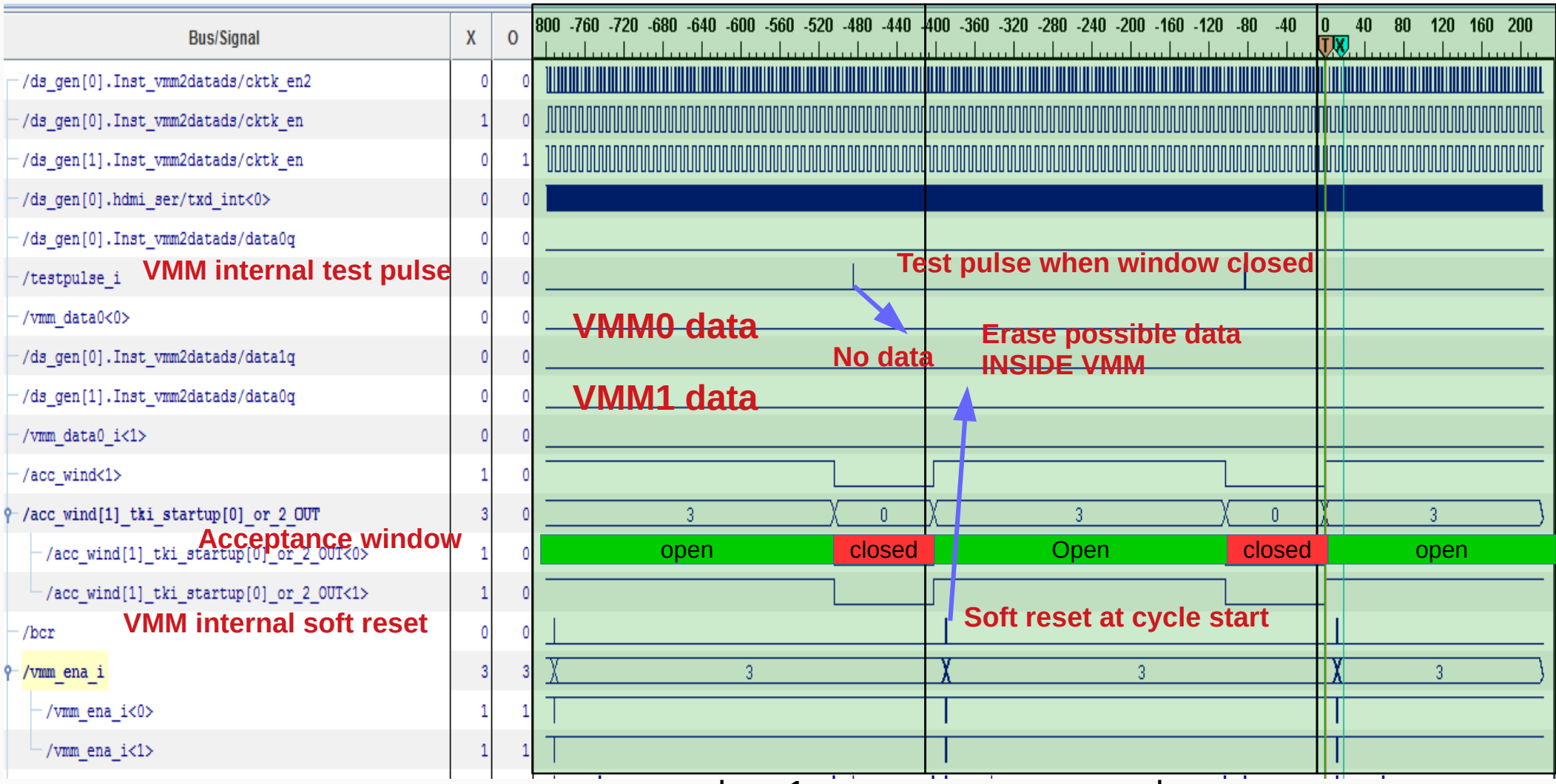
VMM Firmware
Ongoing optimisation

Acceptance window: Digital part of VMM can be disabled (tki)



VMM Firmware
Ongoing optimisation

Acceptance window: Digital part of VMM can be disabled (tki) + soft reset



VMM Firmware
Ongoing optimisation

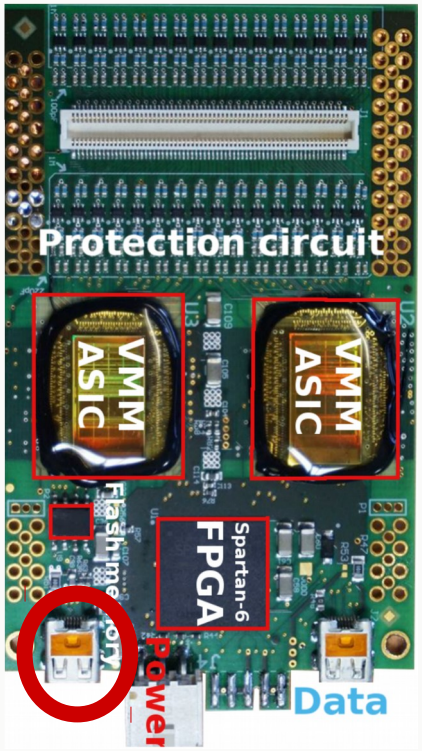
Soft reset allows:
- Erase data inside VMM
- Set BCID counter to 0
⇒ time reset
→ free user definition of readout cycle lenght also < 4096 clk

Acceptance window + Soft reset: only data from defined window in readout cycle
Possible application: data selection in pulsed machine or with respect to trigger

Further firmware imrovement: Defined «End of Run» procedure
ACQ OFF pressed in DAQ = randomn possition in cycle
If a hit is processed in VMM during ACQ OFF (e.g. at high rate)
⇒ Channel dead in next ACQ
Defined «End of Run» procedure = safe finish of current readout cycle

Plans in Bonn

New students in the group:
- Patrick Schwäbig (Master thesis since 16.09.2019): VMM hybrid firmware



- Project 1: Make second HDMI connector on hybrid usable
- Project 2: 200 MHz (DDR) readout of data from VMM to Spartan-6 FPGA

→ full software test bench in Xilinx Isim
⇒ simulation of VMM hybrid in firmware development tool (due to non availability of hardware)

- Finn Jaekel (Master thesis from 28.10.2019):
VMM hybrid production Quality Control → Hybrid mass testing

- Master student hat HISKP: Feasibility of VMM for COMPASS tracker upgrade

- Still looking for a PhD student to work on SRS VMM + GEM detector

Advertisement for internship

Internship research project:
Development of gaseous detectors and their readout electronics for neutron science
→ work on/training on VMM readout and SRS in general, also detectors

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Group webpage: www.lhc-ilc.physik.uni-bonn.de

RISE 2020 – Offer for an internship

Development of gaseous detectors and their readout electronics for neutron science

Markus is official supervisor as the program requires a PhD student

Advertisement for internship

Program: DAAD RISE
DAAD: German academic exchange service
RISE: Research Internships in Science and Engineering
https://www.daad.de/rise/en/rise-germany/find-an-internship/

Eligible:
Undergraduate student studying at a North American, British or Irish University in biology, chemistry, computer science, physics, earth sciences or engineering
What:
750€/month, health insurance, accident and personal liability insurance, travel costs
When/how long:
Start between 15 May and 9 July 2020, duration between 10 weeks and 90 days
Deadlines:
Database open from 1st November, application deadline 15 December 2019
Letters of recommendation until 22 December
Application portal:
https://www.daad.de/rise/en/rise-germany/find-an-internship/application-portal/