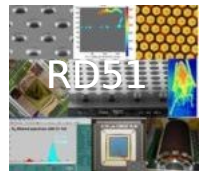
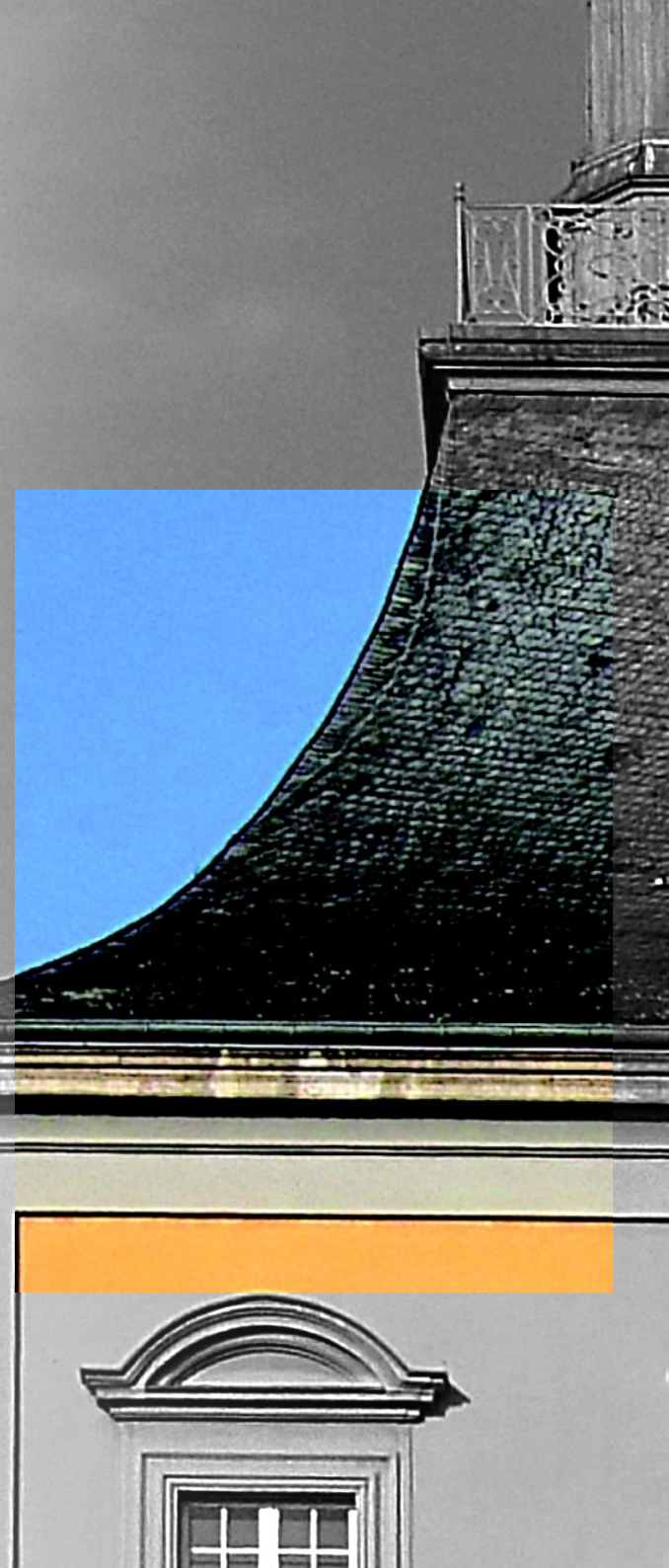




VMM and the SRS – update & plans in Bonn

Michael Lupberger
(University of Bonn)

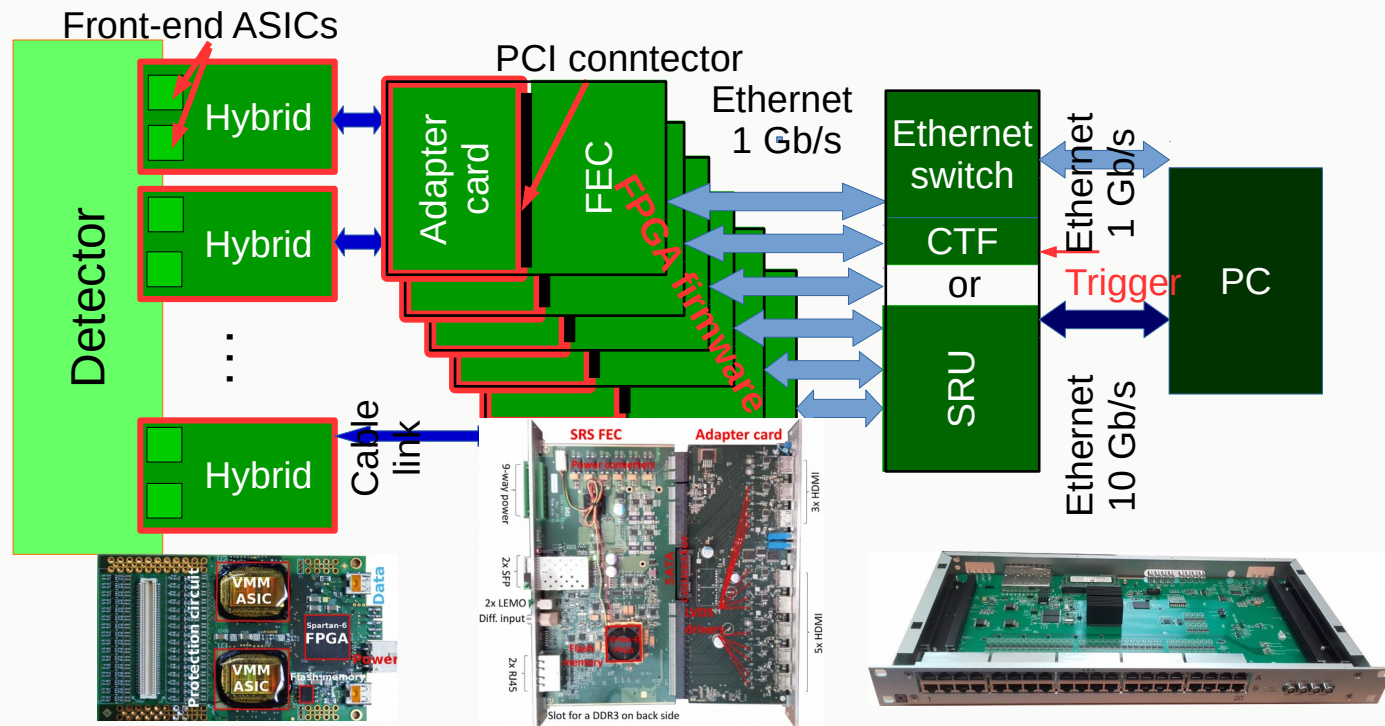
RD51 Collaboration Meeting, CERN
23.10.2019



Introduction: VMM and the SRS

VMM ASIC (developed for ATLAS NSW by BNL) was implemented in SRS
<https://doi.org/10.1016/j.nima.2018.06.046>

System overview:



Project in transition phase from R&D to production, ongoing activities:

- final hardware
- firmware improvements
- common DAQ software
- auxiliary services: cooling, powering

Activities in Bonn - overview

New research project NexGRIND at Physics Institute (PI) led by Jochen Kaminski:
Neutron detectors and readout electronics

- SRS with VMM and Timepix3
- Continue SRS VMM activities:
 - SRS FEC and hybrid Firmware development, support hardware production
 - SRS SRU firmware for VMM data
 - Need for hardware in our group: O(200) hybrid system for detector development
 - Develop cooling for O(200) hybrid detector
- Continue SRS Timepix3 activities (Markus Gruber's talk)

Interest on VMM for COMPASS tracker upgrade at HSKP (Bernhard Ketzer's group)
Part of my Marie Curie Fellowship GenEl starting early 2020

- SRS with VMM for R&D
 - Evaluate noise of VMM and RD51 hybrid in comparison to APV
 - Need for hardware: 4(at least) hybrid lab setup

VMM Firmware

Ongoing optimisation

Continuous data taking boundary conditions requires unambiguous time measurement:
Time measurement in VMM: BCID and TDC

TDC: inter BCID cycle time measurement by 8-bit Time To Amplitude Converter (TAC)

→ ok

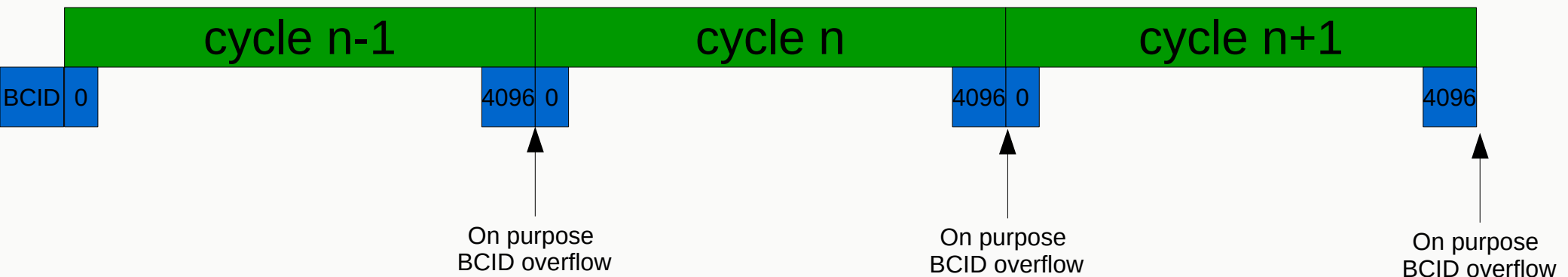
BCID: 12 bit counter incremented by tunable clock (2.5 MHz – 80 MHz)

→ overflows after 4096 clock cycles (clk)

⇒ higher order counter needed to keep unambiguous time measurement

→ readout cycle \leq 4096 clk

Currently: readout cycle = 4096 clk! = BCID overflow



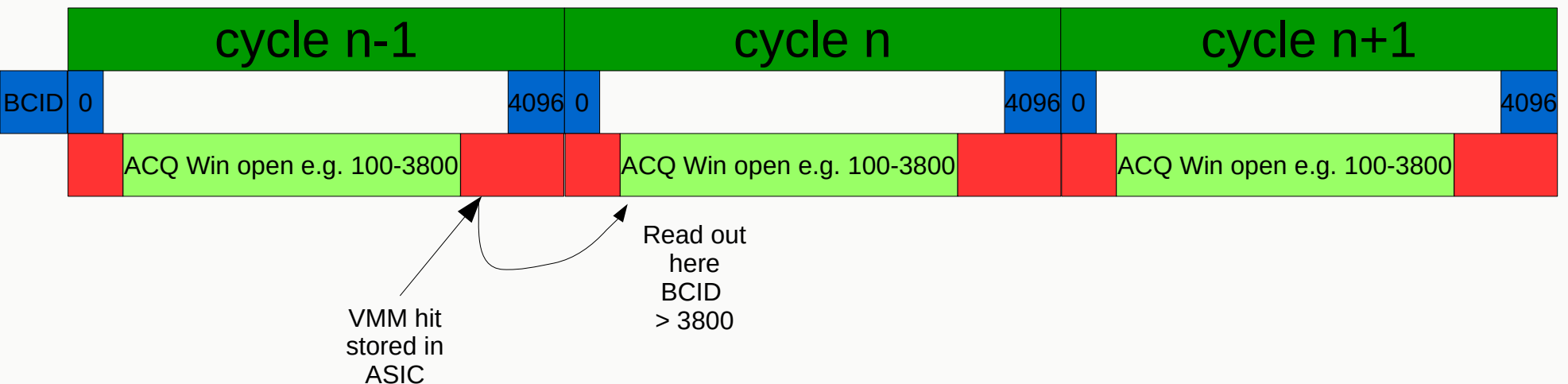
VMM Firmware

Ongoing optimisation

From first safe implementation: remains of sequential data taking:

«Acquisition Window» (ACQ Win): Time when data can be aquired, but not quite:

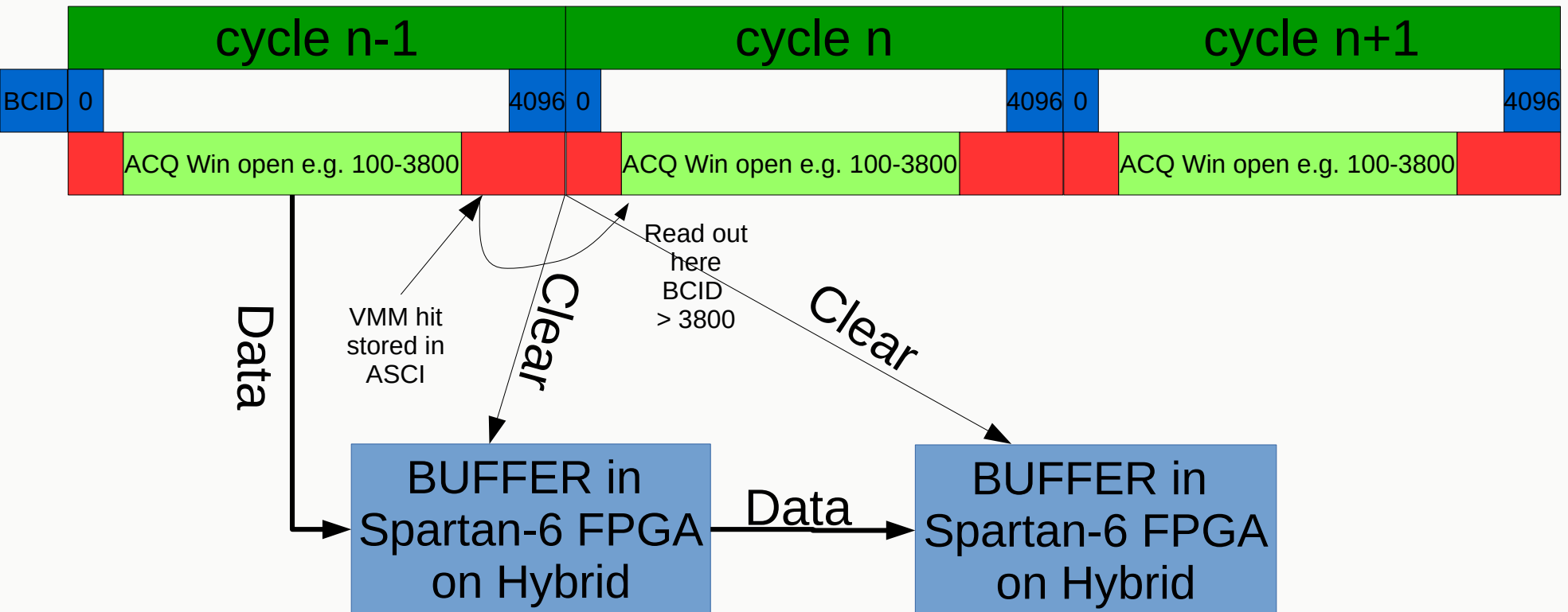
- VMM is self triggered, so always aquires data, when enabled
- window generated in firmware, not processing VMM data from outside window
- data forwarding and sending when ACQ Win is closed
- data from end of cycle n-1 could appear in cycle n



VMM Firmware

Ongoing optimisation

Further problem: Data processing in readout chain

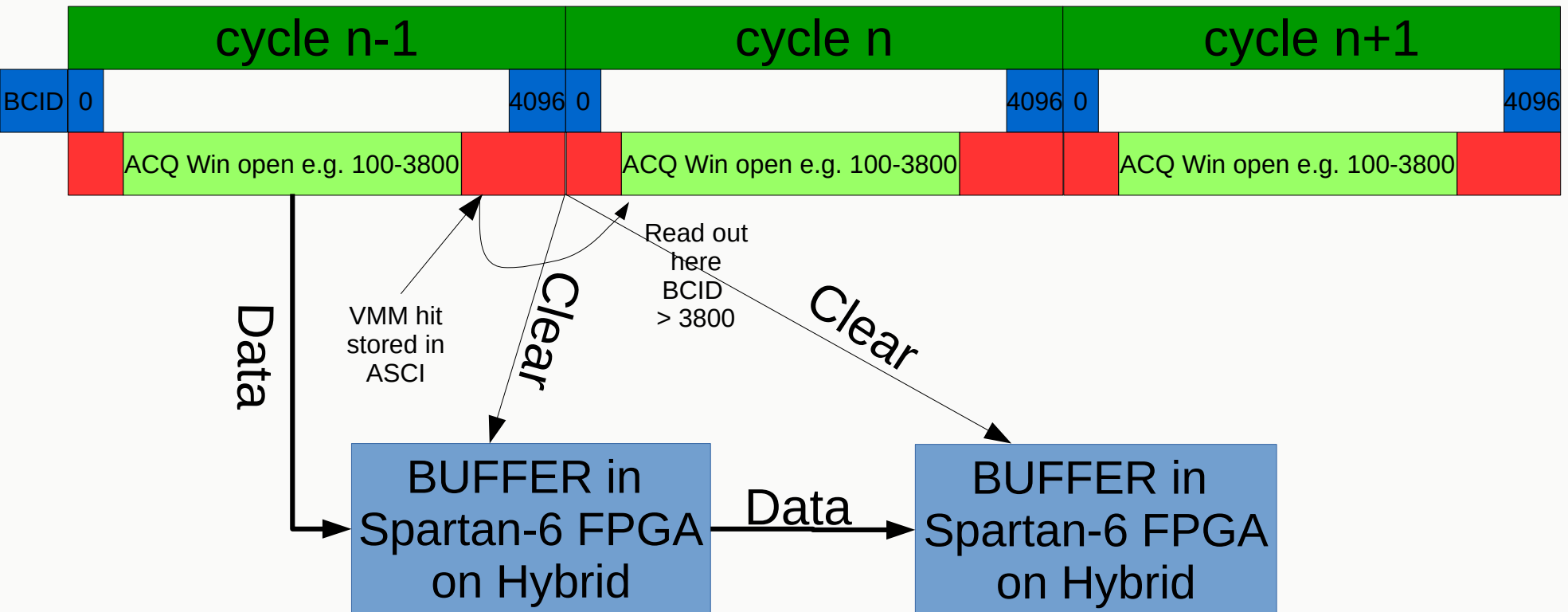


Clear data during processing, to avoid data from cycle n-1 in data from cycle n: does not work

VMM Firmware

Ongoing optimisation

Further problem: Data processing in readout chain

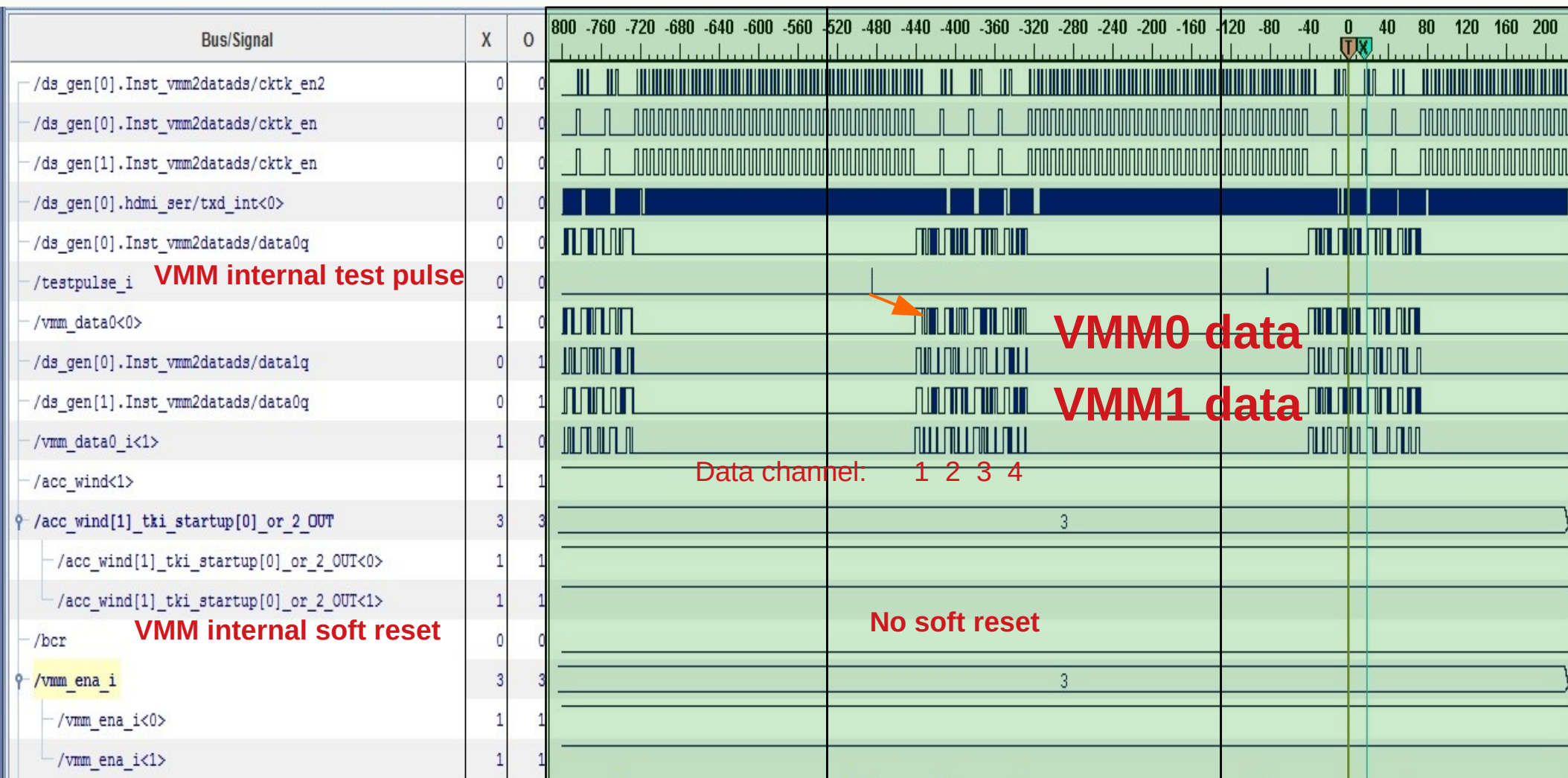


Clear data during processing, to avoid data from cycle n-1 in data from cycle n:
does not work → solution: VMM soft reset

VMM Firmware

Ongoing optimisation

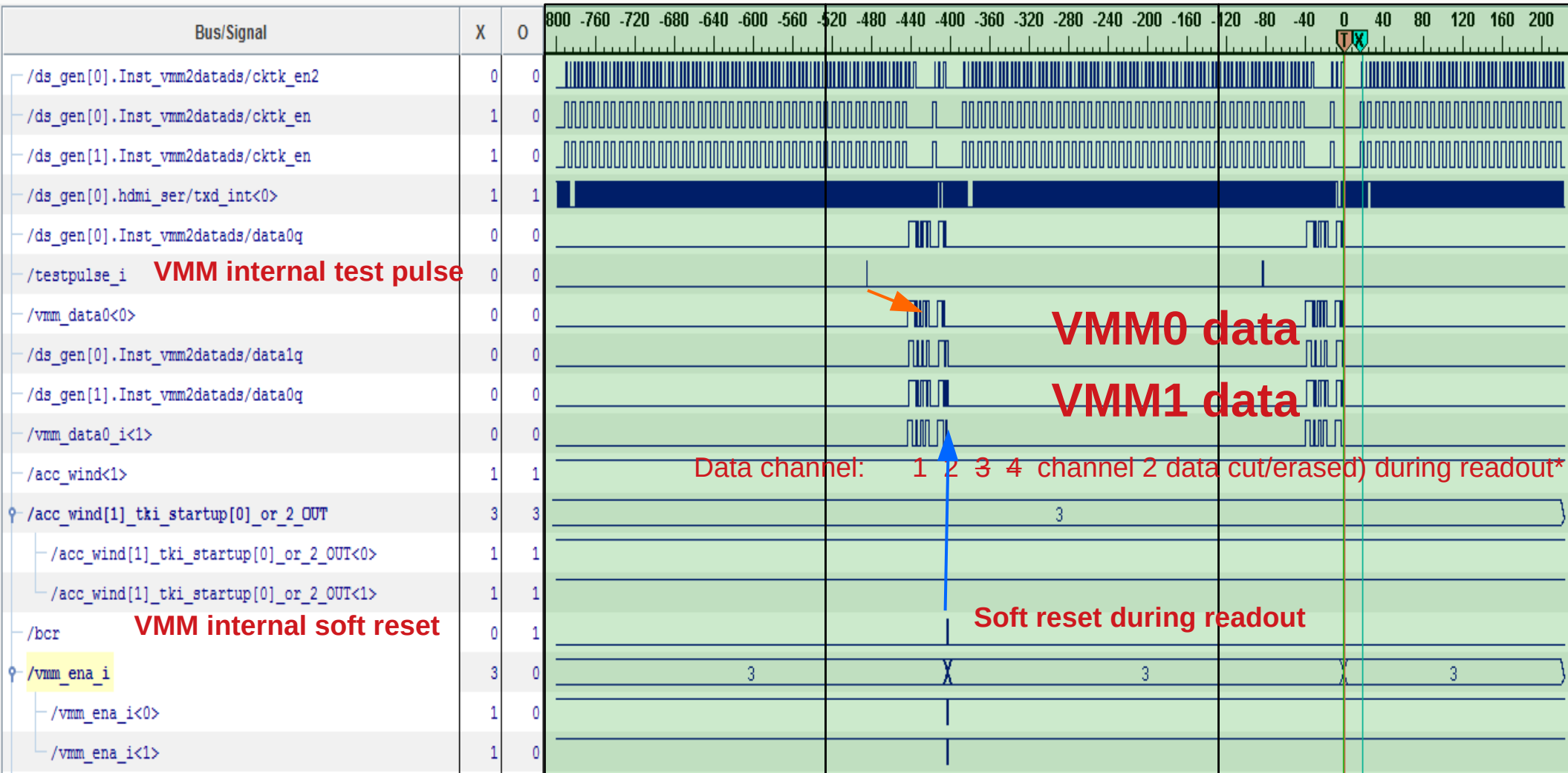
VMM soft reset test: Internal test pulse injected into 4 channels on two VMMs



VMM Firmware

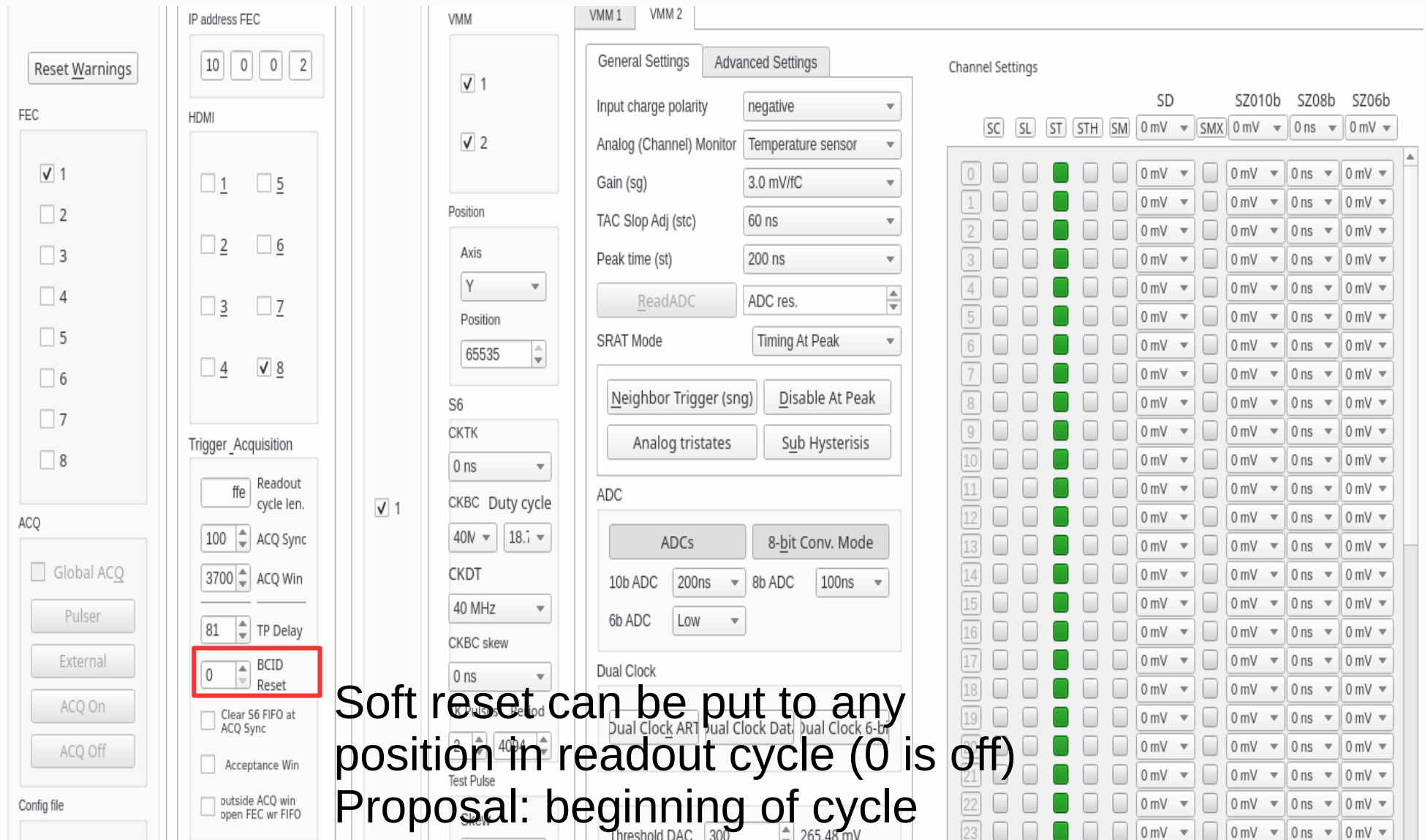
Ongoing optimisation

VMM soft reset test: Internal test pulse injected into 4 channels on two VMMs



*Data of incompletely read channels is further processed in firmware (channel 2 in this example)

Software implementation of soft reset



The screenshot displays the VMM Firmware configuration interface, divided into several panels:

- Reset Warnings:** A button labeled "Reset Warnings".
- FEC:** A list of checkboxes numbered 1 through 8. Checkboxes 1 and 8 are checked.
- HDMI:** A grid of checkboxes for channels 1-8. Checkboxes 1, 2, 3, 4, 5, 6, and 7 are unchecked, while checkbox 8 is checked.
- Trigger Acquisition:**
 - Readout cycle len.: ffe
 - ACQ Sync: 100
 - ACQ Win: 3700
 - TP Delay: 81
 - BCID Reset: 0 (highlighted with a red box)
 - Buttons: "Clear S6 FIFO at ACQ Sync", "Acceptance Win", "outside ACQ win open FEC wr FIFO".
- VMM:**
 - Buttons: "VMM 1", "VMM 2".
 - Checkboxes: 1 and 2 are checked.
 - Position: Axis (Y), Position (65535).
 - S6: CKTK (0 ns), CKBC Duty cycle (40V, 18.i), CKDT (40 MHz), CKBC skew (0 ns).
 - Buttons: "Neighbor Trigger (sng)", "Disable At Peak", "Analog tristates", "Sub Hysteresis".
- Advanced Settings:**
 - Input charge polarity: negative
 - Analog (Channel) Monitor: Temperature sensor
 - Gain (sg): 3.0 mV/fC
 - TAC Slop Adj (stc): 60 ns
 - Peak time (st): 200 ns
 - Buttons: "ReadADC", "ADC res."
 - SRAT Mode: Timing At Peak
 - ADCs: 10b ADC (200ns), 8b ADC (100ns), 6b ADC (Low)
 - Dual Clock: Dual Clock ART, Dual Clock Dat, Dual Clock 6-bit
- Channel Settings:**
 - Buttons: SC, SL, ST, STH, SM.
 - SD: 0 mV
 - SMX: 0 mV
 - SZ010b: 0 ns
 - SZ08b: 0 mV
 - SZ06b: 0 mV
 - Table with 24 rows (0-23) and 12 columns of settings.

Soft reset can be put to any position in readout cycle (0 is off)
 Proposal: beginning of cycle

Software implementation of soft reset

The screenshot displays the VMM Firmware configuration interface, divided into several panels:

- Reset Warnings:** A button labeled "Reset Warnings".
- FEC:** A list of checkboxes numbered 1 through 8, with checkbox 1 checked.
- HDMI:** A grid of checkboxes numbered 1 through 8, with checkbox 8 checked.
- Trigger Acquisition:** Settings for "Readout cycle len." (ffe), "ACQ Sync" (100), "ACQ Win" (3700), "TP Delay" (81), "BCID Reset" (0), and two optional checkboxes: "Clear S6 FIFO at ACQ Sync" and "outside ACQ win open FEC wr FIFO", both of which are highlighted with red boxes.
- VMM:** A section for "VMM 1" and "VMM 2" with checkboxes 1 and 2 checked. It includes a "Position" dropdown set to "Y" and a "Position" input field with the value "65535".
- Advanced Settings:** A sub-panel with "General Settings" and "Advanced Settings" tabs. It includes:
 - Input charge polarity: negative
 - Analog (Channel) Monitor: Temperature sensor
 - Gain (sg): 3.0 mV/fC
 - TAC Slop Adj (stc): 60 ns
 - Peak time (st): 200 ns
 - SRAT Mode: Timing At Peak
 - Buttons: Neighbor Trigger (sng), Disable At Peak, Analog tristates, Sub Hysteresis
 - ADC: ADCs, 8-bit Conv. Mode, 10b ADC (200ns), 8b ADC (100ns), 6b ADC (Low)
 - Dual Clock: Dual Clock ART, Dual Clock Dat, Dual Clock 6-bi
 - Threshold DAC: 300, 265.48 mV
- Channel Settings:** A table with columns for "SD", "SZ010b", "SZ08b", and "SZ06b". Each column has a dropdown menu. The table has 24 rows, each with a row number and several checkboxes. The "ST" column checkboxes are all checked.

Clearing of FIFOs is now optional

Acceptance window

The screenshot displays the VMM Firmware configuration interface, divided into several panels:

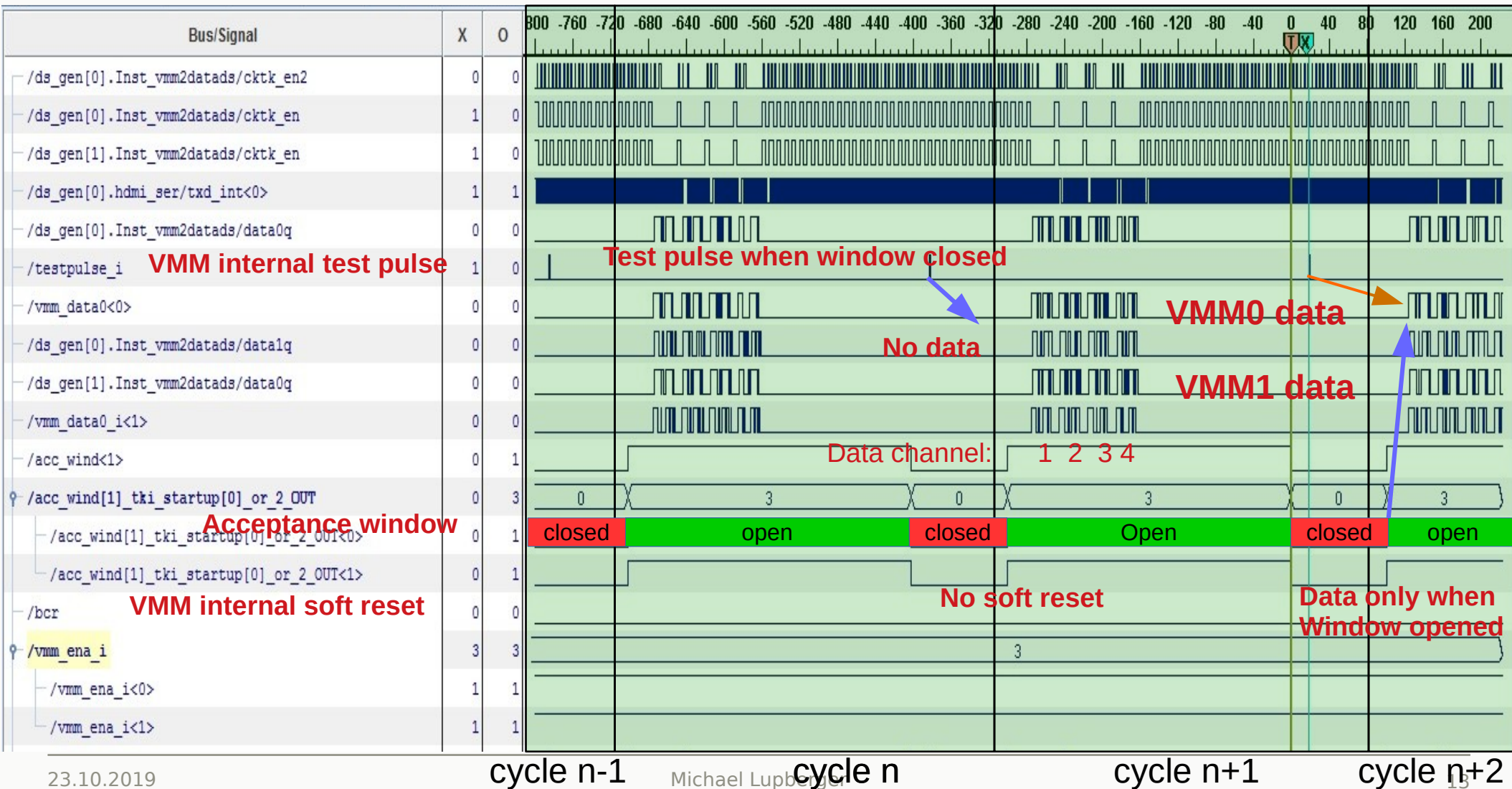
- FEC:** A list of checkboxes numbered 1 through 8. Checkboxes 1 and 8 are checked.
- HDMI:** A grid of checkboxes numbered 1 through 8. Checkboxes 1, 2, 3, 4, 5, 6, and 7 are unchecked, while checkbox 8 is checked.
- Trigger Acquisition:** Includes fields for 'Readout cycle len.' (ffe), 'ACQ Sync' (100), 'ACQ Win' (3700), 'TP Delay' (81), and 'BCID Reset' (0). A checkbox for 'Acceptance Win' is highlighted with a red box.
- VMM:** Contains 'VMM 1' and 'VMM 2' checkboxes (both checked), 'Position' (Axis: Y, Position: 65535), 'S6' (CKTK: 0 ns, CKBC Duty cycle: 40V, 18.i, CKDT: 40 MHz, CKBC skew: 0 ns, TK Pulses Period: 2, 1094), and 'Test Pulse' (Skew).
- General Settings / Advanced Settings:** Includes 'Input charge polarity' (negative), 'Analog (Channel) Monitor' (Temperature sensor), 'Gain (sg)' (3.0 mV/fC), 'TAC Slop Adj (stc)' (60 ns), 'Peak time (st)' (200 ns), 'ReadADC' button, 'ADC res.' field, 'SRAT Mode' (Timing At Peak), 'Neighbor Trigger (sng)' and 'Disable At Peak' buttons, 'Analog tristates' and 'Sub Hysteresis' buttons.
- ADC:** Includes 'ADCs' and '8-bit Conv. Mode' buttons, and fields for '10b ADC' (200ns), '8b ADC' (100ns), and '6b ADC' (Low).
- Channel Settings:** A table with columns for 'SD', 'SZ010b', 'SZ08b', and 'SZ06b'. Each column has a dropdown menu. Below the columns is a grid of checkboxes for channels 0 through 23. Channels 1 through 23 have their checkboxes checked.

Also new: Acceptance window

VMM Firmware

Ongoing optimisation

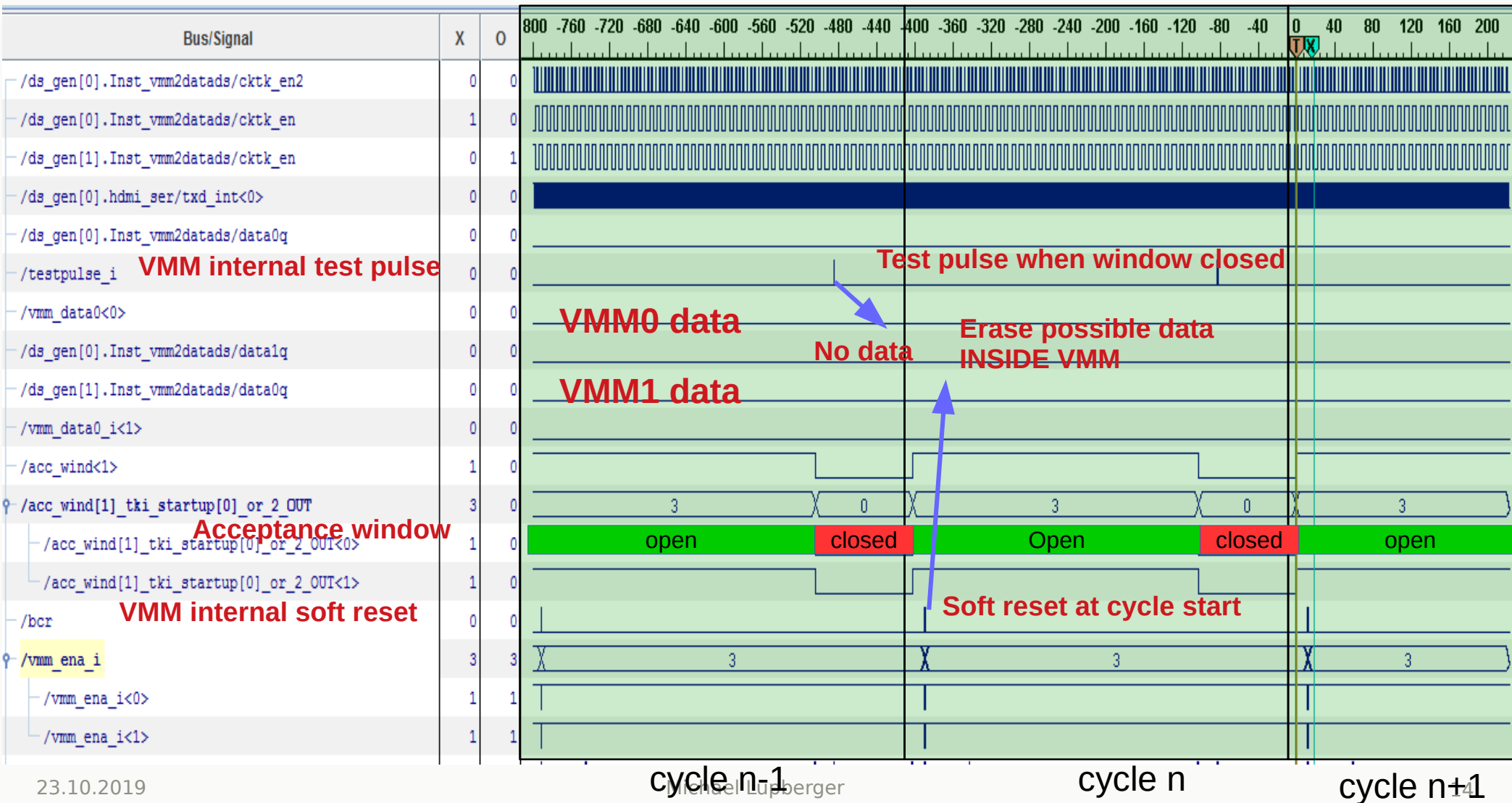
Acceptance window: Digital part of VMM can be disabled (tki)



VMM Firmware

Ongoing optimisation

Acceptance window: Digital part of VMM can be disabled (tki) + soft reset



VMM Firmware

Ongoing optimisation

Soft reset allows:

- Erase data inside VMM
- Set BCID counter to 0

⇒ time reset

→ free user definition of readout cycle length also < 4096 clk

Acceptance window + Soft reset: only data from defined window in readout cycle
Possible application: data selection in pulsed machine or with respect to trigger

Further firmware improvement: Defined «End of Run» procedure

ACQ OFF pressed in DAQ = random position in cycle

If a hit is processed in VMM during ACQ OFF (e.g. at high rate)

⇒ Channel dead in next ACQ

Defined «End of Run» procedure = safe finish of current readout cycle

New students in the group:

- Patrick Schwäbig (Master thesis since 16.09.2019): VMM hybrid firmware

- Project 1: Make second HDMI connector on hybrid usable
- Project 2: 200 MHz (DDR) readout of data from VMM to Spartan-6 FPGA

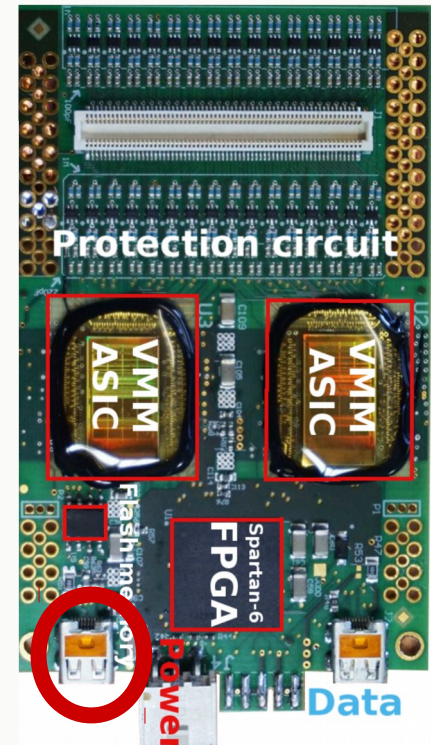
→ full software test bench in Xilinx Isim

⇒ simulation of VMM hybrid in firmware development tool
(due to non availability of hardware)

- Finn Jaekel (Master thesis from 28.10.2019):
VMM hybrid production Quality Control → Hybrid mass testing

- Master student hat HISKP: Feasibility of VMM for COMPASS tracker upgrade

- Still looking for a PhD student to work on SRS VMM + GEM detector



Advertisement for internship

Internship research project:

Development of gaseous detectors and their readout electronics for neutron science

→ work on/training on VMM readout and SRS in general, also detectors



Markus Gruber, M. Sc. (Physics)

Physikalisches Institut der Universität Bonn

Nussallee 12, D-53115 Bonn, Germany

eMail: gruber@physik.uni-bonn.de

Institute page: www.pi.uni-bonn.de

Group webpage: www.lhc-ilc.physik.uni-bonn.de



RISE 2020 – Offer for an internship

Development of gaseous detectors and their readout electronics for neutron science

Markus is official supervisor as the program requires a PhD student

Advertisement for internship

Program: DAAD RISE

DAAD: German academic exchange service

RISE: Research Internships in Science and Engineering

<https://www.daad.de/rise/en/rise-germany/find-an-internship/>

Eligible:

Undergraduate student studying at a North American, British or Irish University in biology, chemistry, computer science, physics, earth sciences or engineering

What:

750€/month, health insurance, accident and personal liability insurance, travel costs

When/how long:

Start between 15 May and 9 July 2020, duration between 10 weeks and 90 days

Deadlines:

Database open from 1st November, application deadline 15 December 2019

Letters of recommendation until 22 December

Application portal:

<https://www.daad.de/rise/en/rise-germany/find-an-internship/application-portal/>