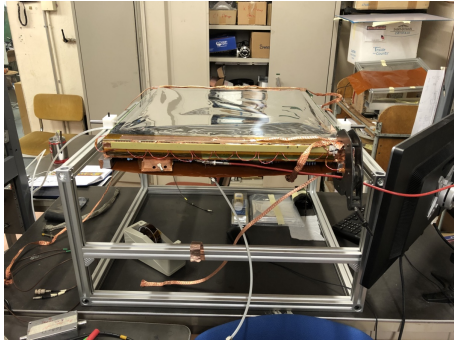# ESS VMM3a news

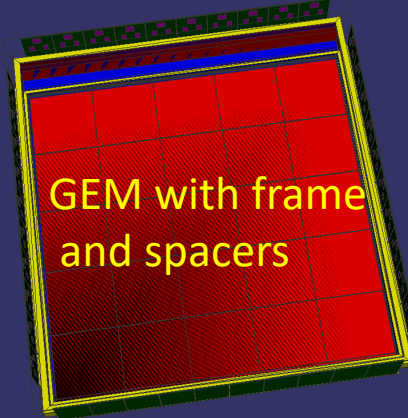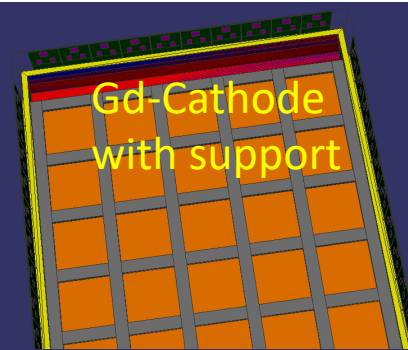## RD51 Collaboration Meeting

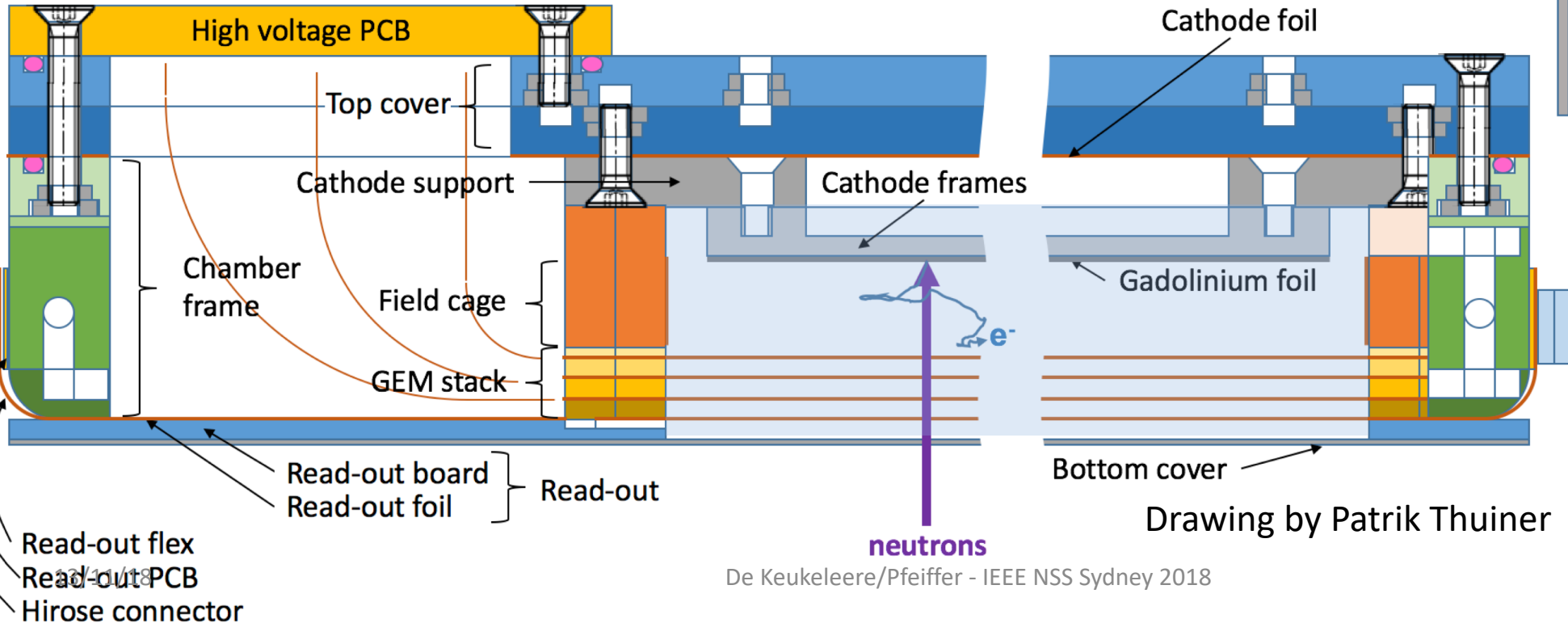October 21st to 23rd
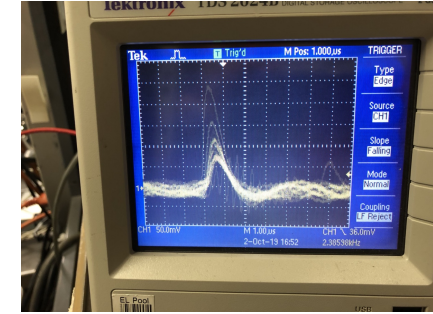
Dorothea Pfeiffer (ESS)

Jerome Samarati (ESS)

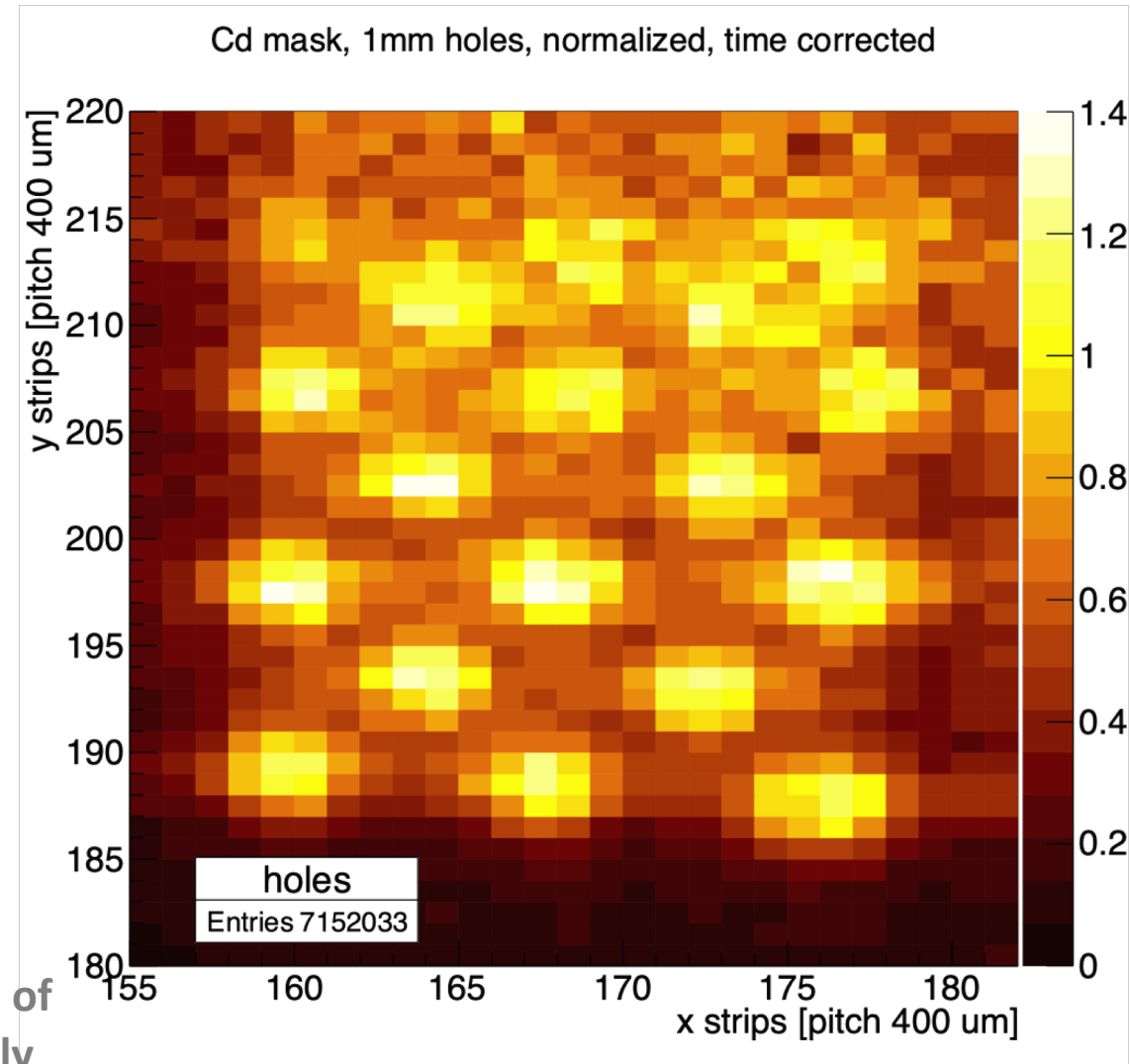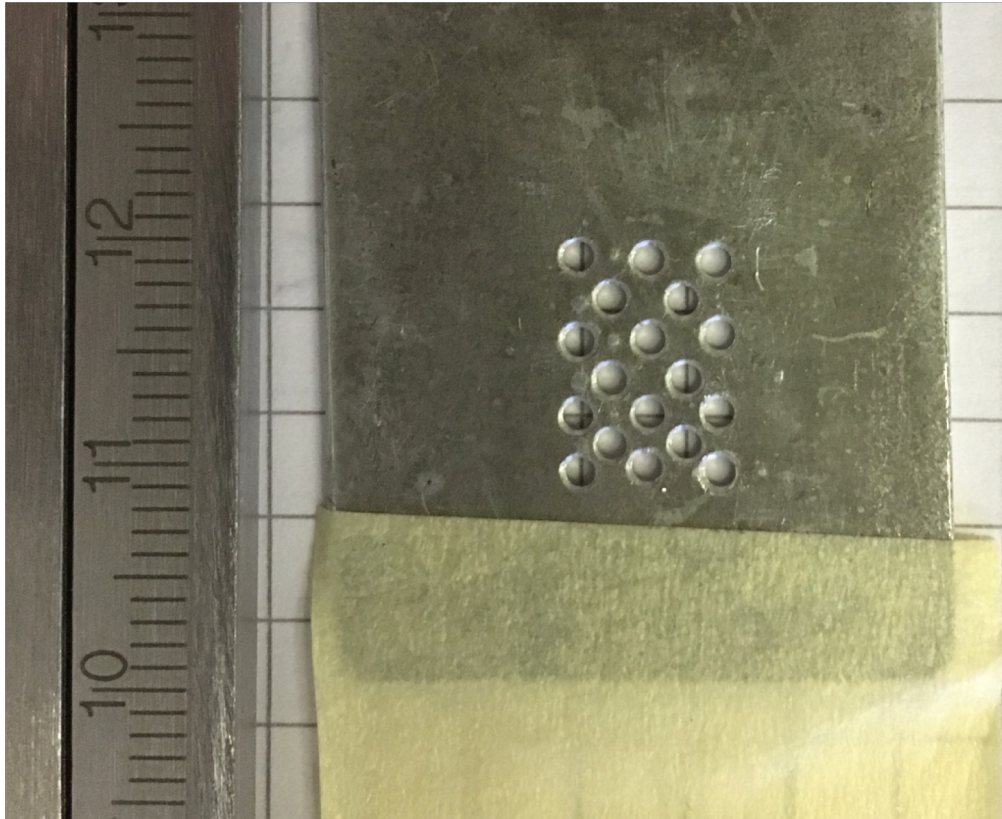Richard Hall-Wilton (ESS)

VMM3a
Gd-GEM for NMX

- Detector Demonstrator Zita

- 80 VMM3a per detector (5120 channels per detector)

- Will start tests with Xrays, neutrons and VMM3a (one detector quadrant) in October

High voltage PCB

Top cover

Cathode support

Cathode frames

Cathode foil

Chamber frame

Field cage

Gadolinium foil

GEM stack

e⁻

Read-out board
Read-out foil

Read-out

Bottom cover

neutrons

Drawing by Patrik Thuiner

Read-out flex
Read-out PCB
Hirose connector

Gd-Cathode with support

GEM with frame and spacers

De Keukeleere/Pfeiffer - IEEE NSS Sydney 2018

VMM3a
NMX detector test at BNC July 2018

Cd mask, 1mm holes, normalized, time corrected

- Beam focused on lower three rows of Cd mask
- Clearly resolved holes with minimum separation (centre to centre) of about 2.0 mm horizontally, 1.6 mm vertically, and 1.3 mm diagonally
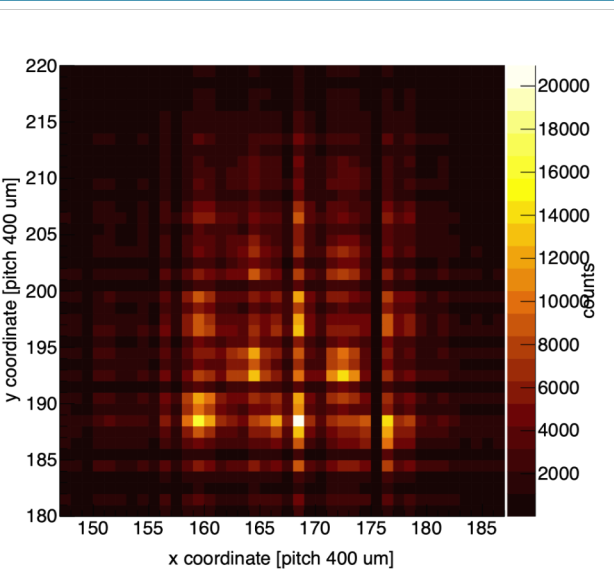
VMM delivering quality data from demonstrator
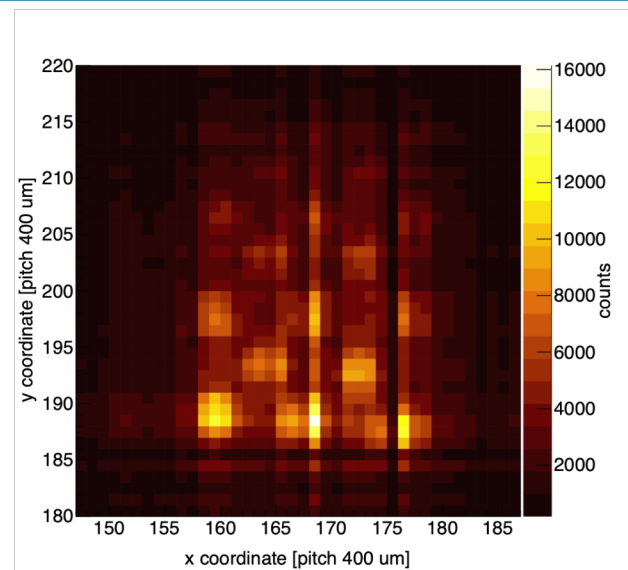
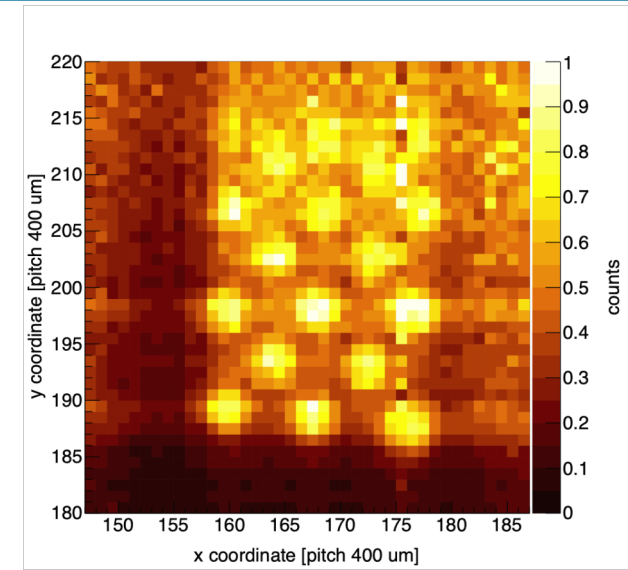# NMX detector test at BNC July 2018
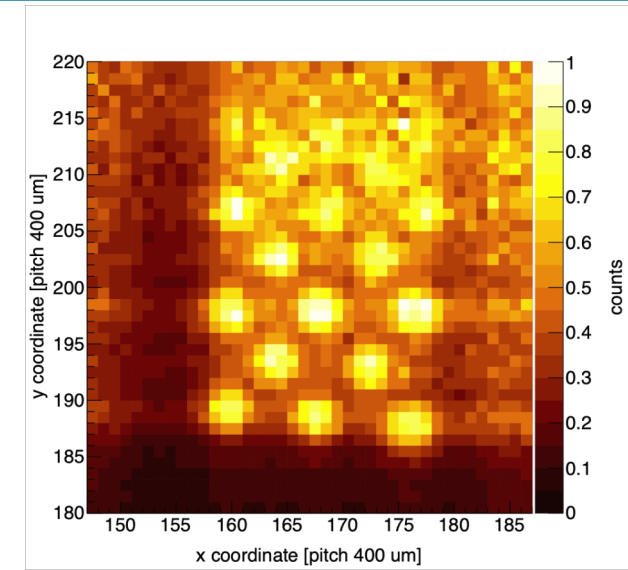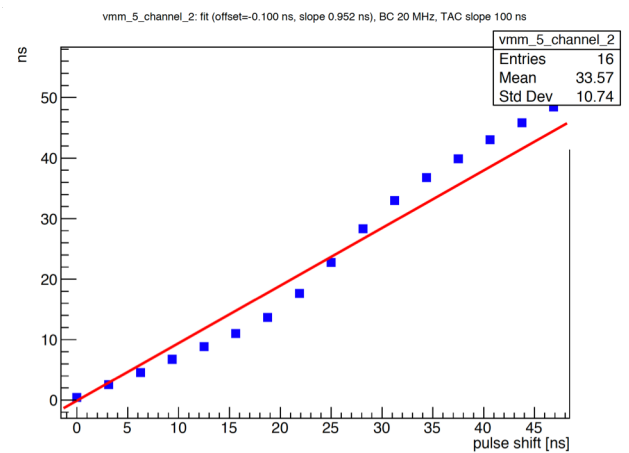# Time calibration and normalization

uTPC, no time calib

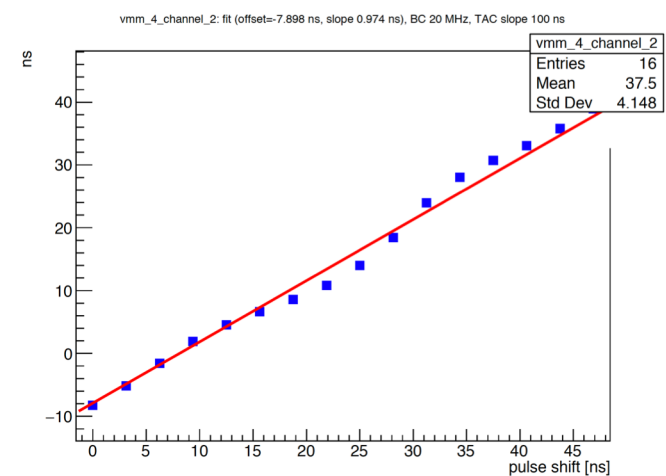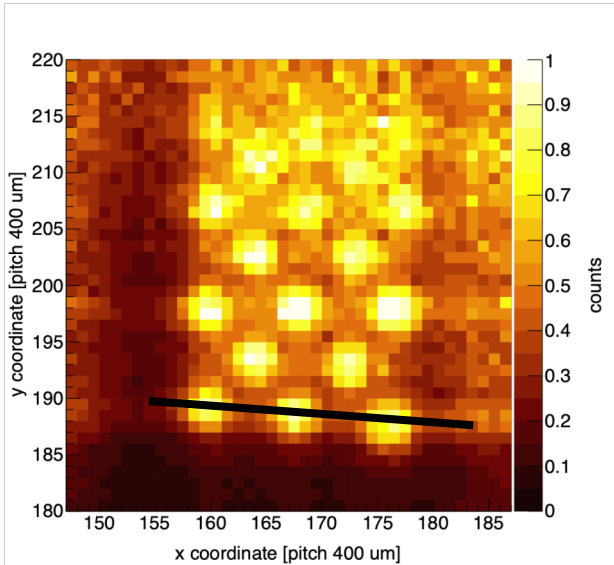uTPC, with time calib

uTPC, no time calib, normalized

uTPC, time calib, normalized

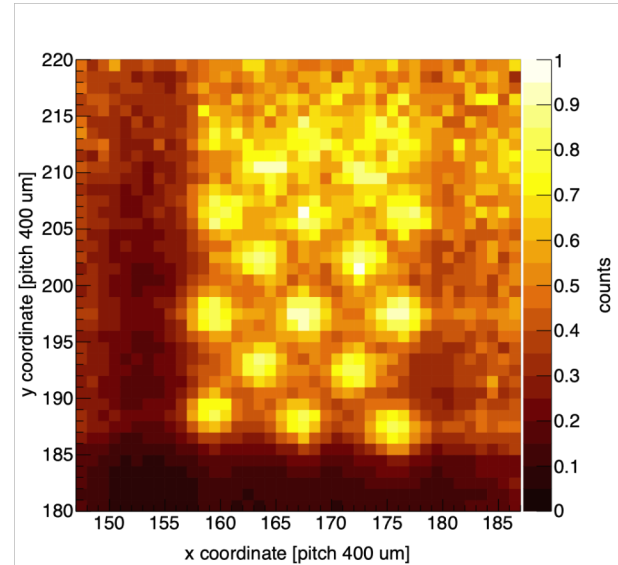- **For center-of-mass like algorithms, ADC calibration necessary**
- **For utpc like algorithms, also time calibration**
- **Both implemented in slow control, DAQ and reconstruction**

NMX detector test at BNC July 2018
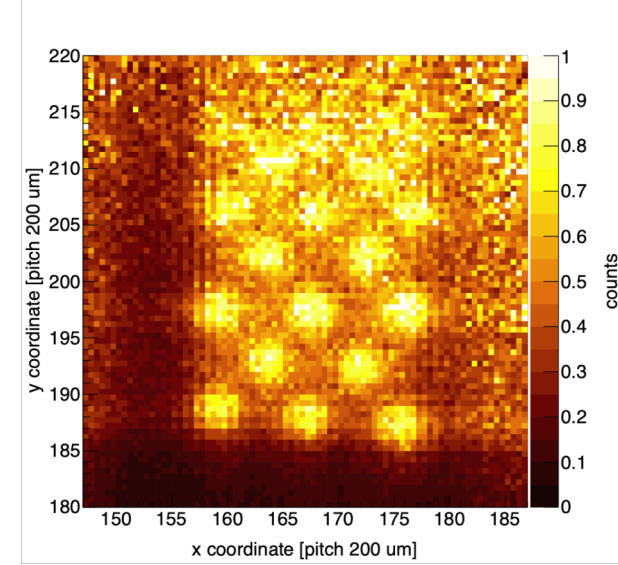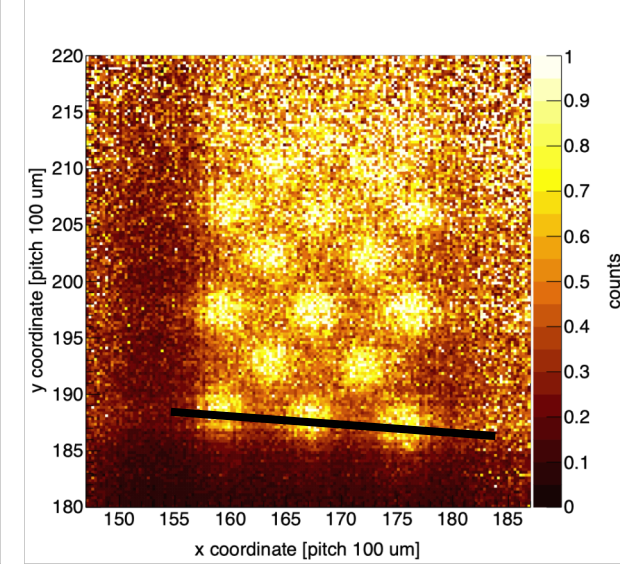# Improved analysis
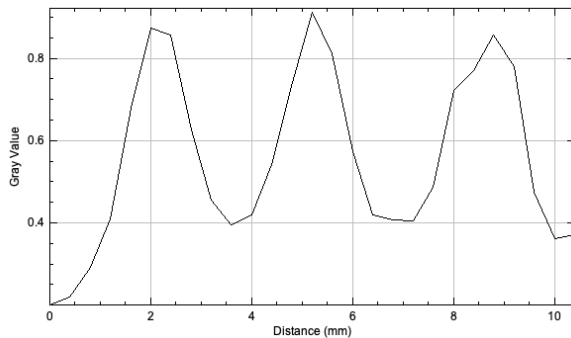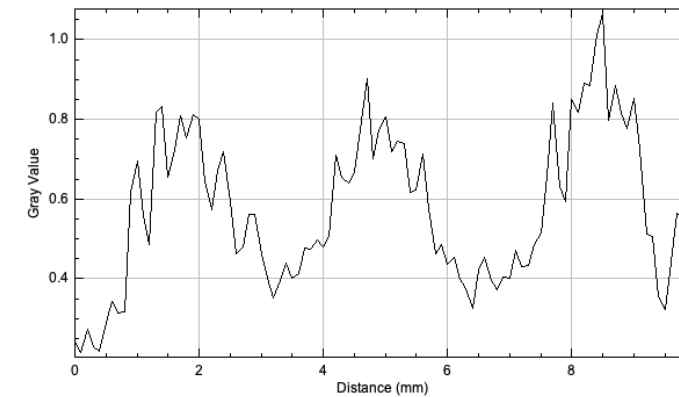

uTPC,
400 um pixel size

Weighted uTPC,
400 um pixel size

Weighted uTPC,
200 um pixel size

Weighted uTPC,
100 um pixel size

Ongoing work on algorithms and detector settings

Crystal diffraction sample: Triose phosphate isomerase
w/ 2-phosphoglycolate (2PG) inhibitor
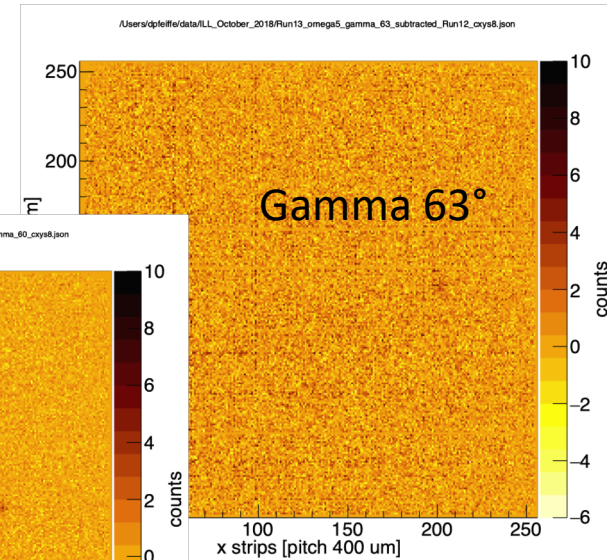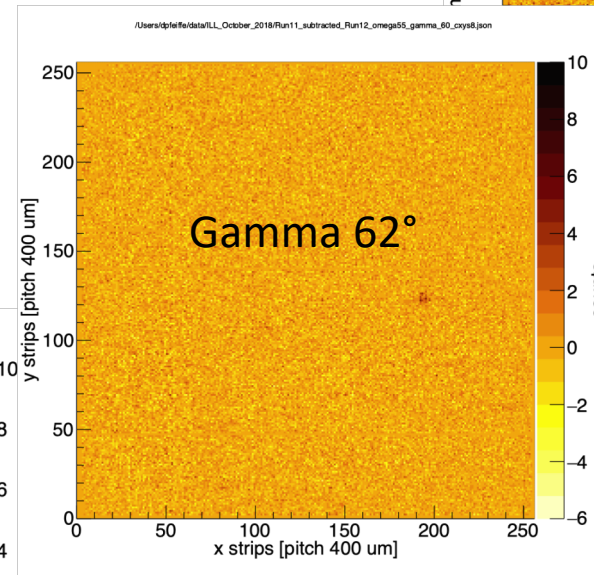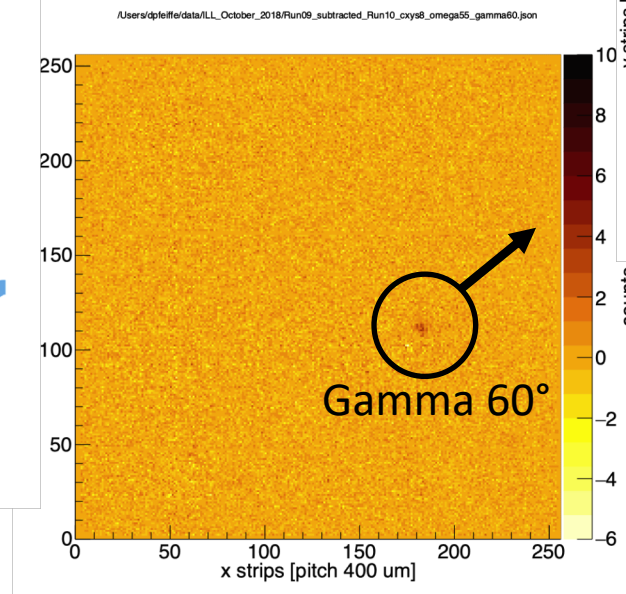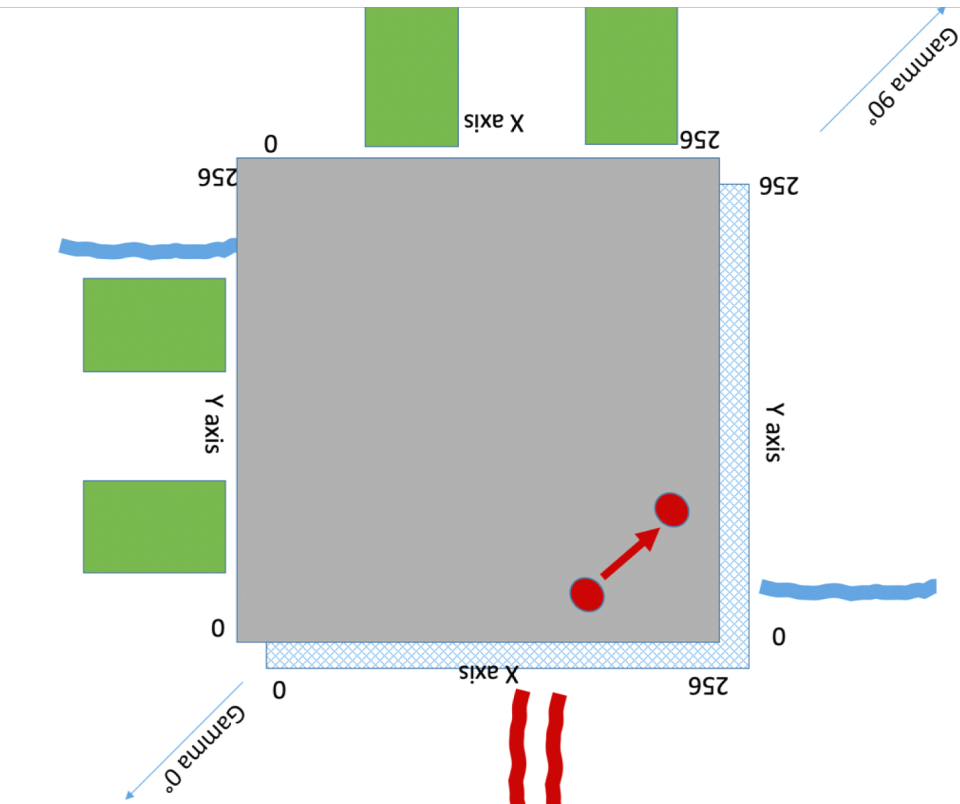
Crystal orientation Omega 55°

VMM3a performance sufficient to resolve weak reflections

VMM3a
Multiblade test at Utgard December 2018

- Successful test of VMM3a hybrid with MB
- MB: Charge injection into:
  - Wires (negative polarity, AC coupled)
  - strips (positive polarity, DC coupled)
- Successfully read out with VMM3a via analog monitoring output and digital data in continuous mode
- Gain 1 mV/fC , 200 ns shaping time

Injecting charge into strips of
MultiBlade Boron-10 detector
Signal on monitoring output

Injecting charge into wires of
MultiBlade Boron-10 detector
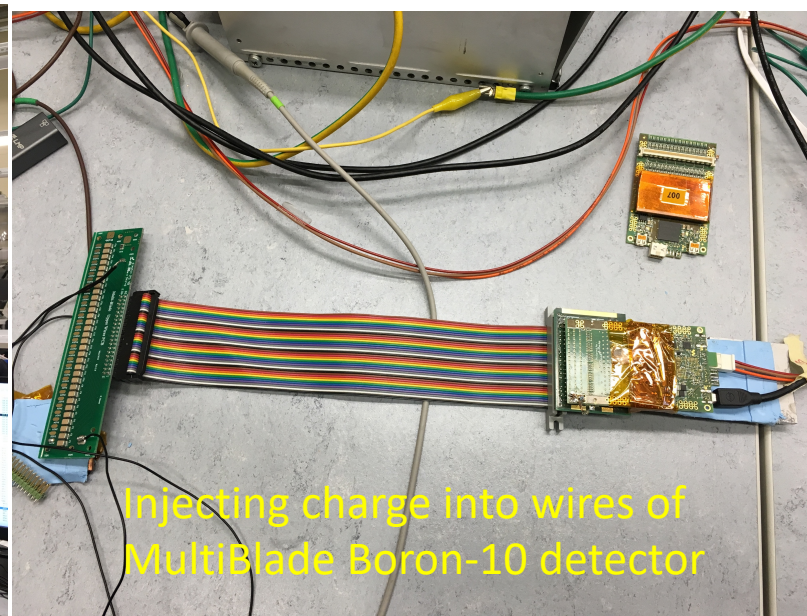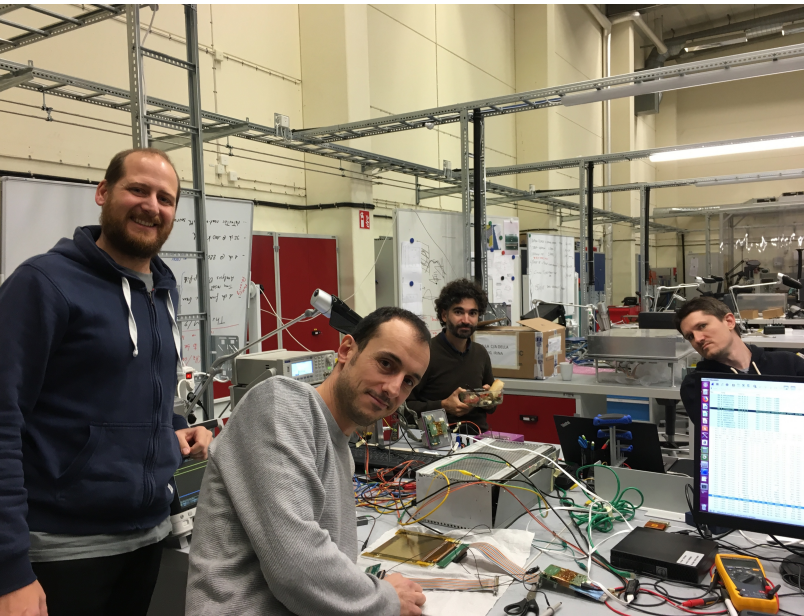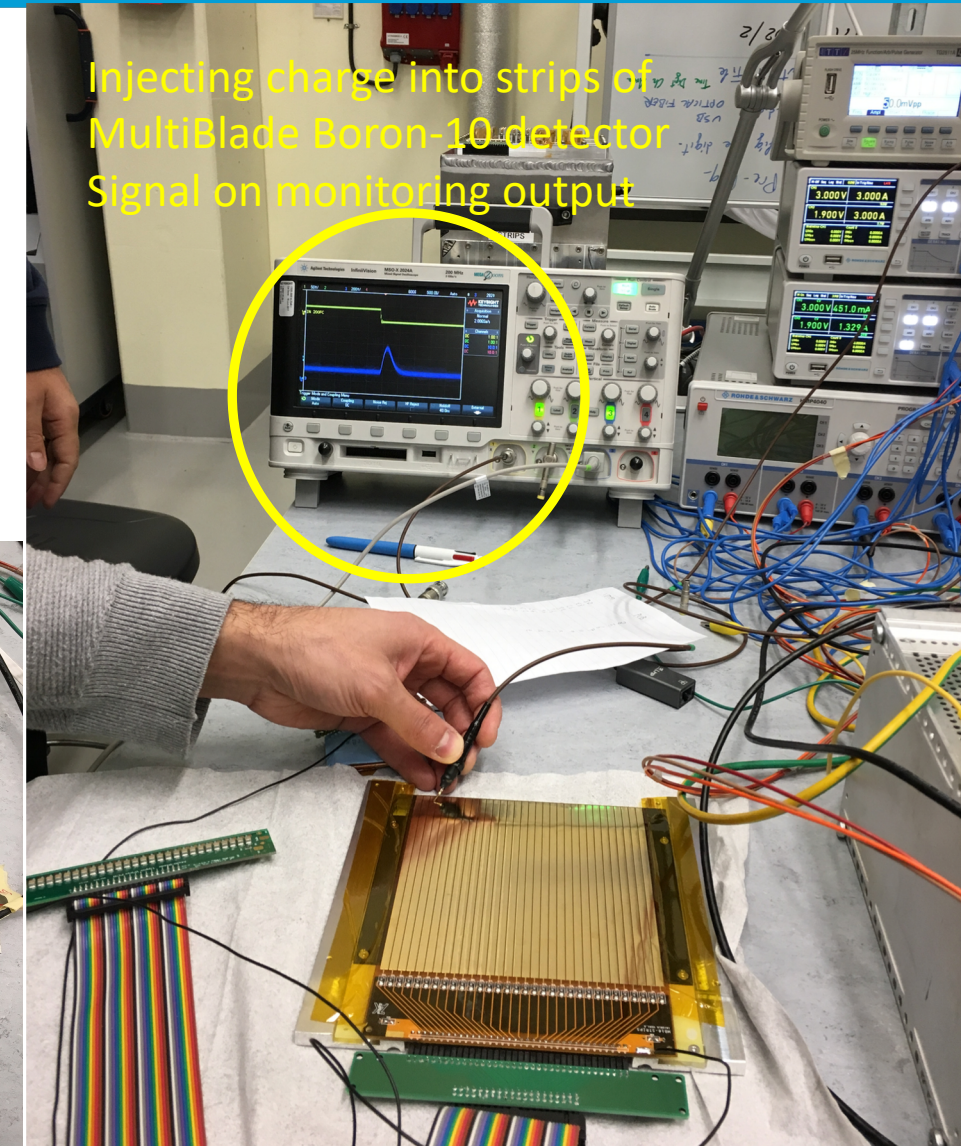
Multiblade Adapter
for RD51 VMM3a hybrid

6.36 cm

0.85 cm

2.67 cm

1.28 cm

2.85 cm
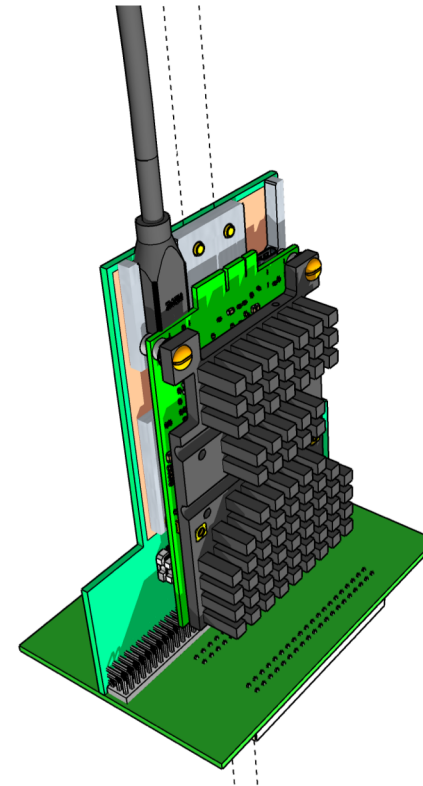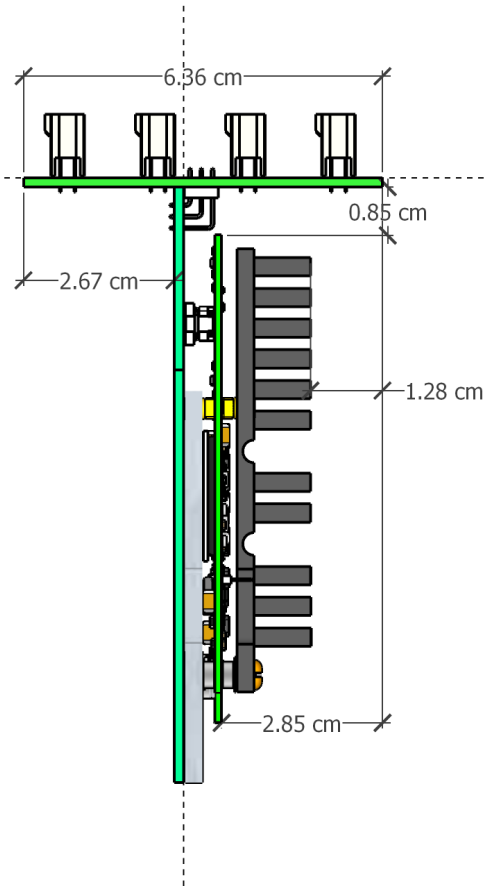
Designed by Hans Muller

VMM3a
Multigrid test at STF Summer 2019

- Started in May to test VMM3a together with Multigrid

- Huge team effort between detector group (Ramsey, Alex, Isabell, Doro) and DMSC (Morten, Martin)

- As expected, biggest challenges at the beginning: Mapping and noise

Setup with MG , VMM3a and SRS

VMM3a hybrids with adapter for MG
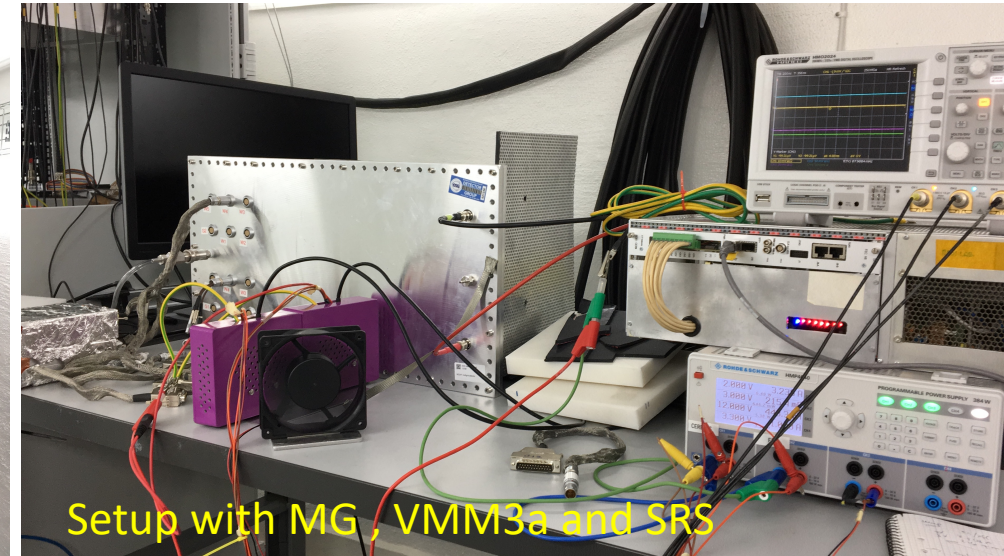
VMM3a
Multigrid test at STF Summer 2019

- Analog matching of VMM to MG succesful

- After solving mapping and noise issue, successful reconstruction of source position

- Wires and grids read out with VMM3a gain of 1mV/fC

- Optimization: Matching of detector gain to VMM3a gain to use full range of 10 bit ADC

VMM works on MultiGrid detector!

neutrons

Multi-grid MG.24

AmBe source inside ESS moderator
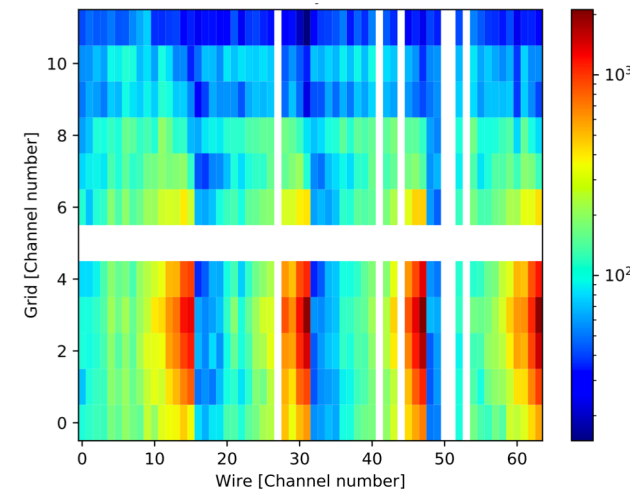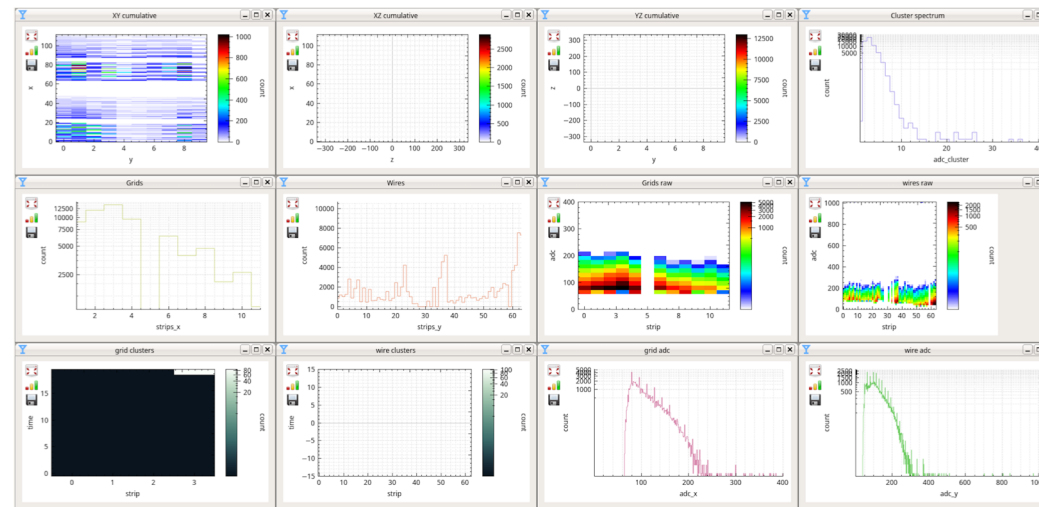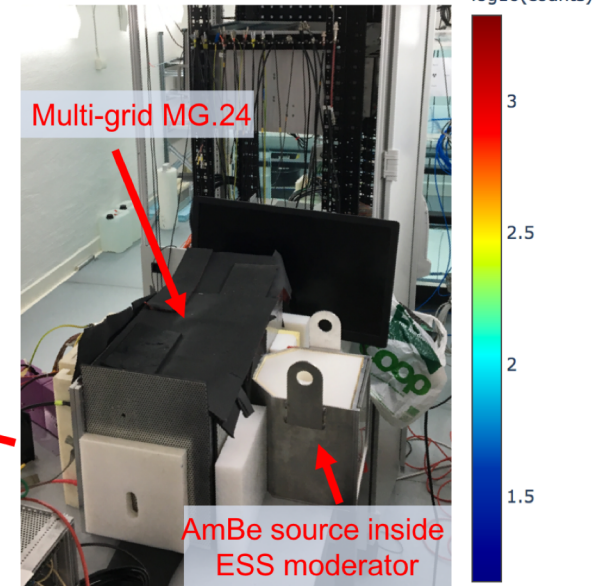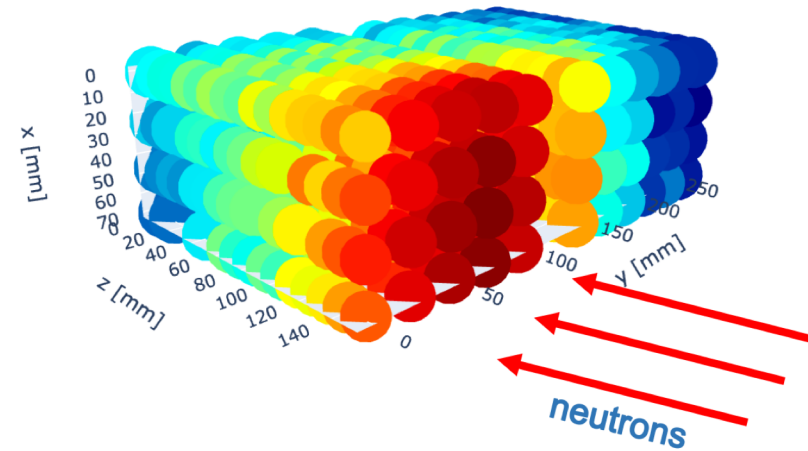
Schematic drawing of ESS Readout

Steven Alcock, Detector Group, 2nd July 2019
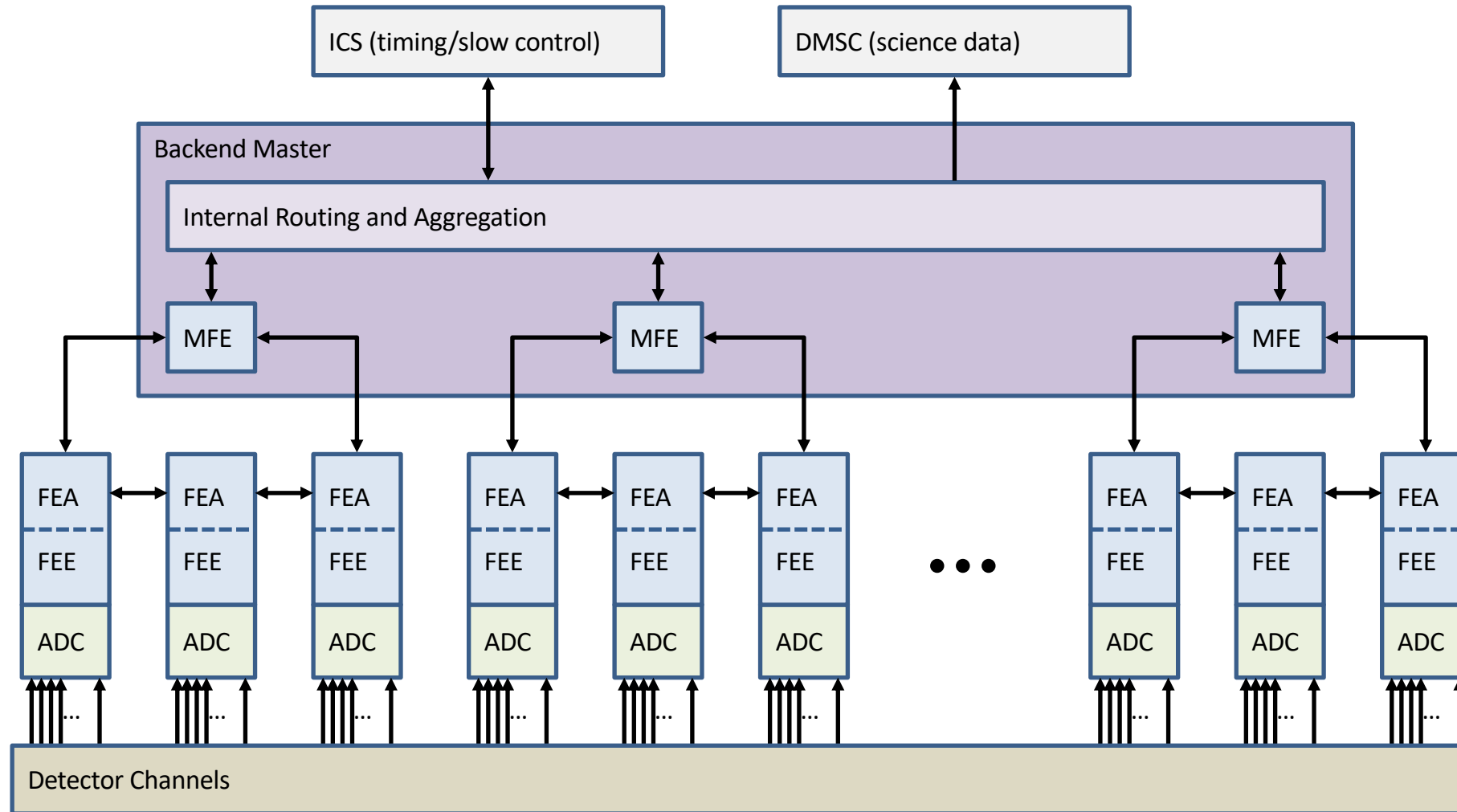
Timing distribution in rings

- Front ends (FEA/FEE) connected to Master (MFE) via 8b/10b encoded SFP+ links.
- ESS clock used to generate these links – can be recovered and forwarded by each front end (similar concept to Synchronous Ethernet).
- The ESS timestamp can therefore be forwarded to all the front ends, forming a single distributed synchronous system.
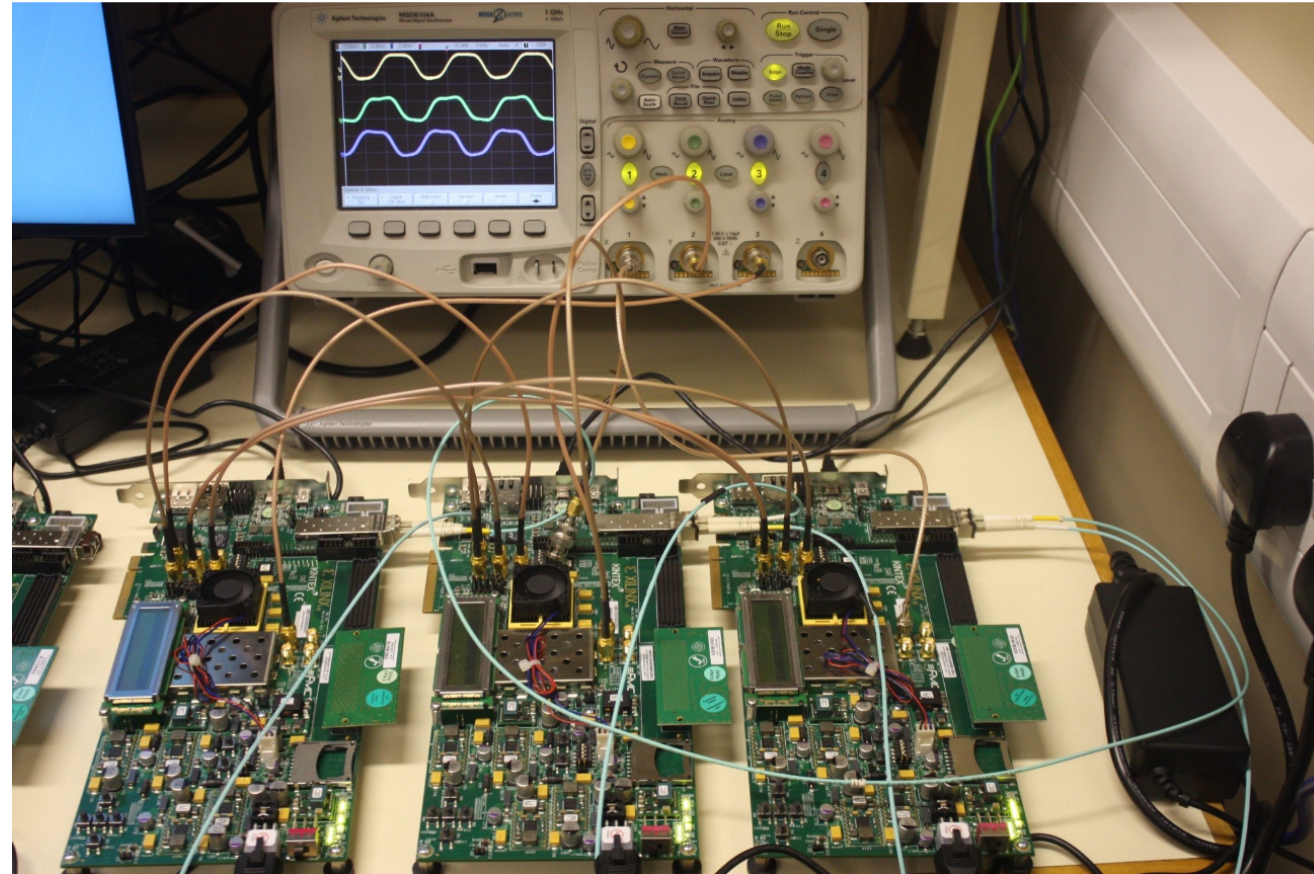
FE user interface

- FEA (front end assister) firmware communicates with the ring/backend
- FEE (front end user firmware) communicates with frontend ASIC like VMM3a or ADC
- FEA and FEE part of firmware communicate via AXI4 streams
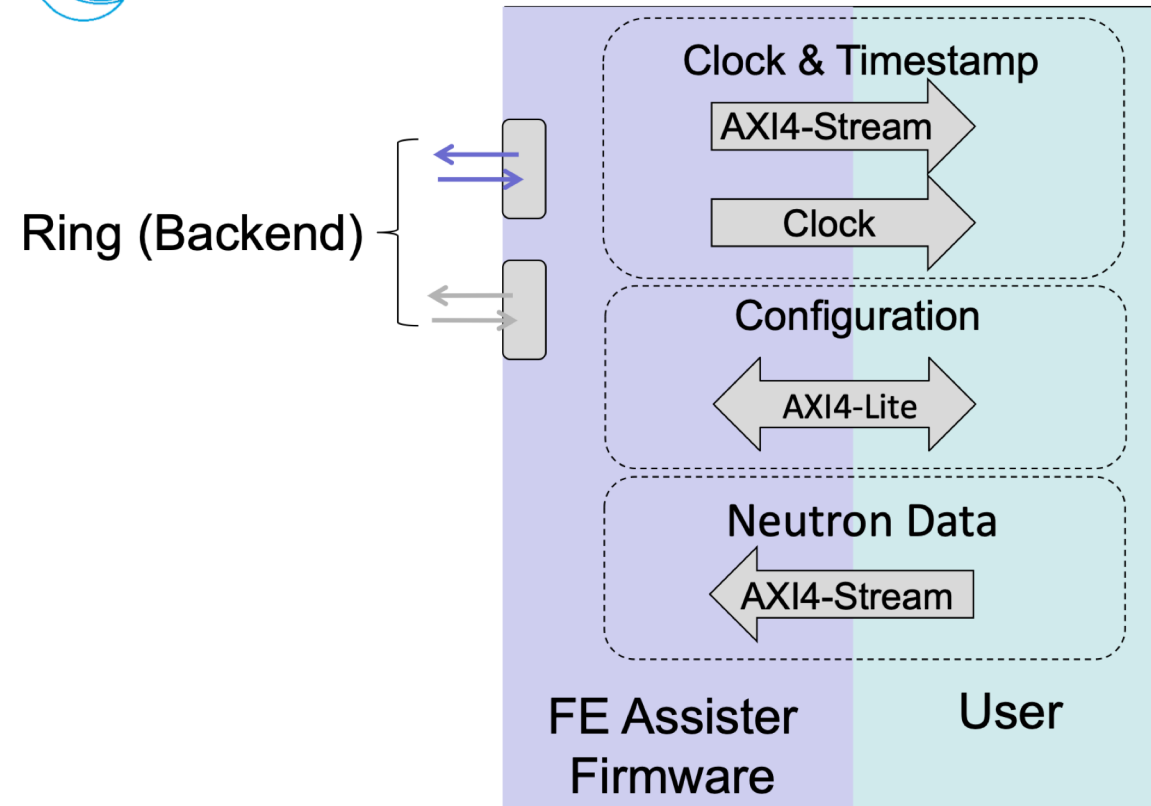
For FE integration models see
BrightnESS Deliverable Report: D4.1 – *Integration Plan for Detector Readout*, Scott Kolya et.al. 2017

Frontend (FEE) and assister (FEA): hardware and firmware modules

- Frontend FEE with firmware communicating with ASIC
- Frontend assister FEA with firmware to communicate with ring
- Could be in one FPGA and one card, or two FPGAs and two cards
- Advantages for two card solution: RD51 hybrid already exists, form factor of FEE card can stay small, heat dissipated on FEA card away from FEE

Two separate cards

One card containing FEE and FEA

FEE card to communicate with ASIC

FEA card to communicate with ring

Start immediately
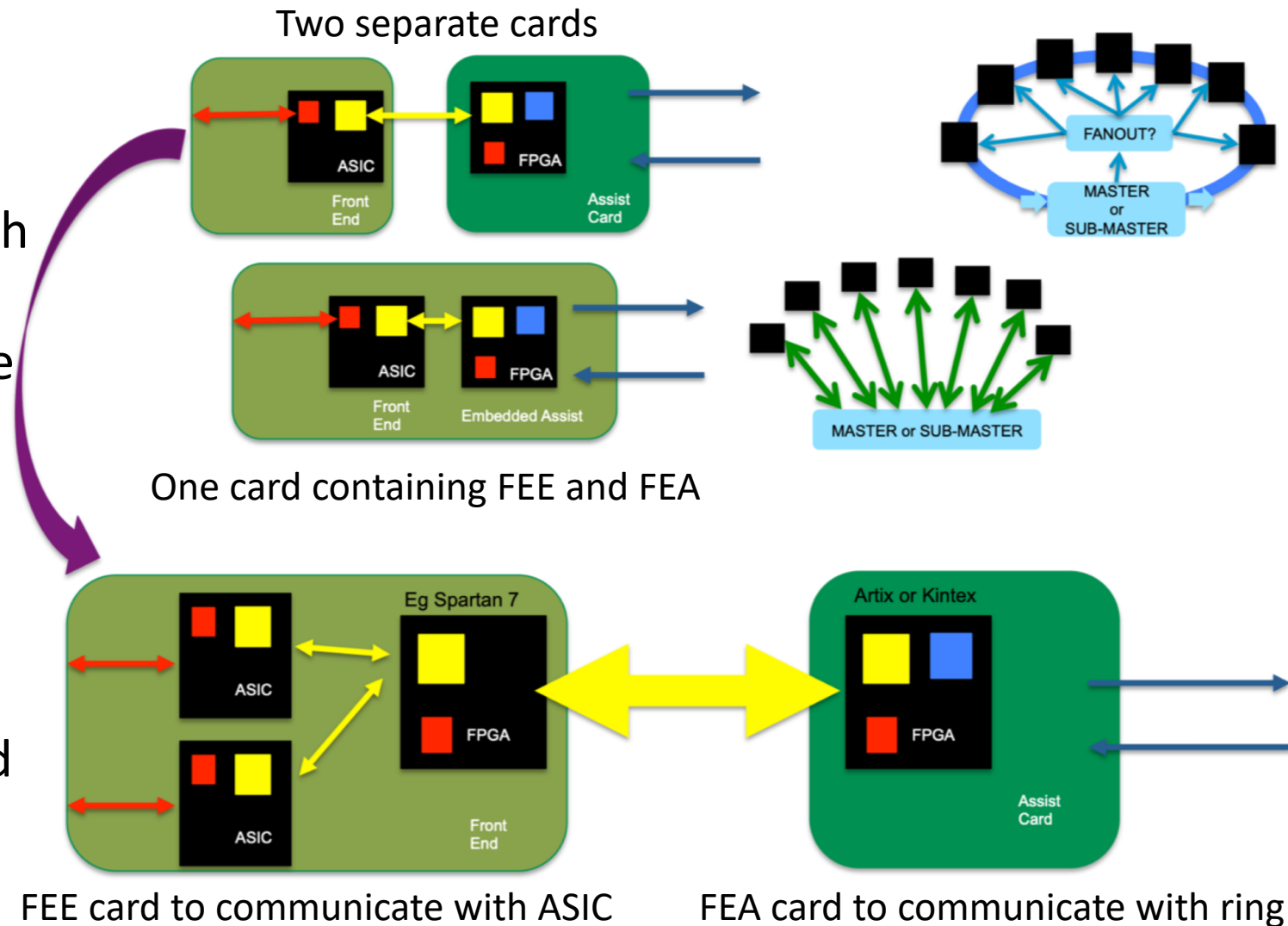
- Use existing RD51 VMM3a hybrid with Spartan 6
- RD51 hybrid firmware objectives:
  - Support high rate operations (part of general high rate optimizations of whole readout chain)
  - Structure, clean up and document
- Use FPGA development board as assister platform
- Develop firmware for assister Artix7 FPGA

LVDS via HDMI

SFP+ x 2

"FEC+DCARD"-like FIRMWARE

ASSISTER FIRMWARE
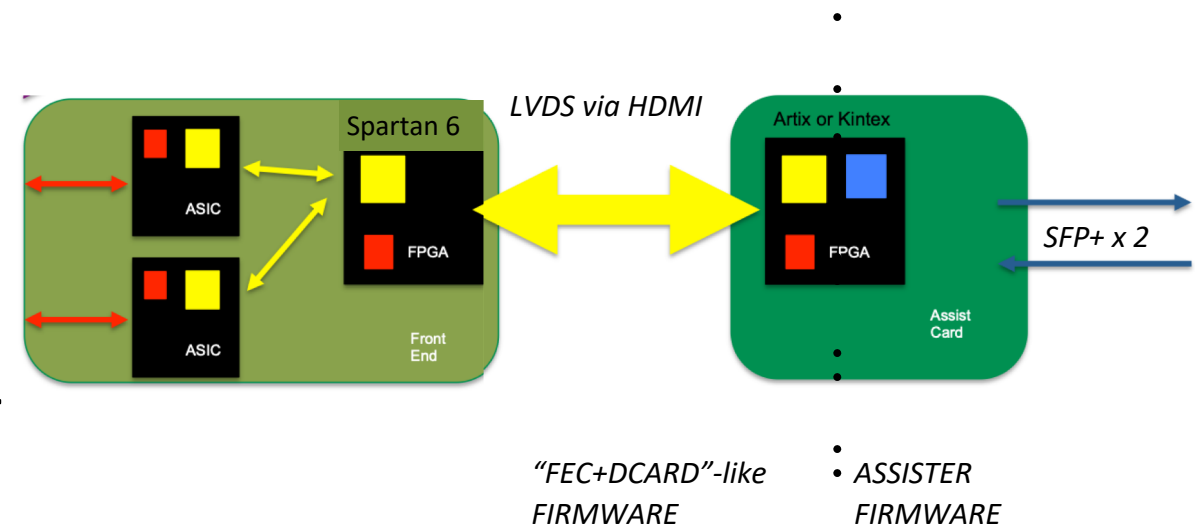
Step 1b (use dedicated assister hardware):

Within the next six months

- Use dedicated assister hardware
- Assister layout for beam monitor readout already exists, can be modified for RD51 hybrid

LVDS via HDMI

SFP+ x 2

"FEC+DCARD"-like FIRMWARE

ASSISTER FIRMWARE
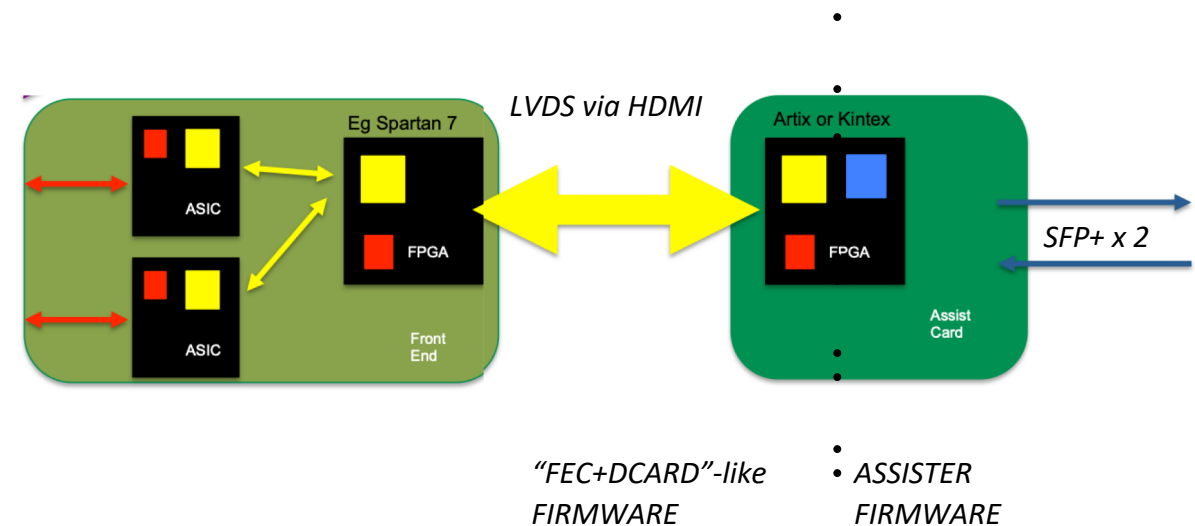
Step 1c (upgrade RD51 hybrid with Spartan7 or Artix7):

More longterm

- Explore options to upgrade RD51 hybrid to use Series 7 FPGA
- Have hybrid design modified by Alex
- Port firmware to Series 7 FPGA

LVDS via HDMI

SFP+ x 2

"FEC+DCARD"-like FIRMWARE

ASSISTER FIRMWARE
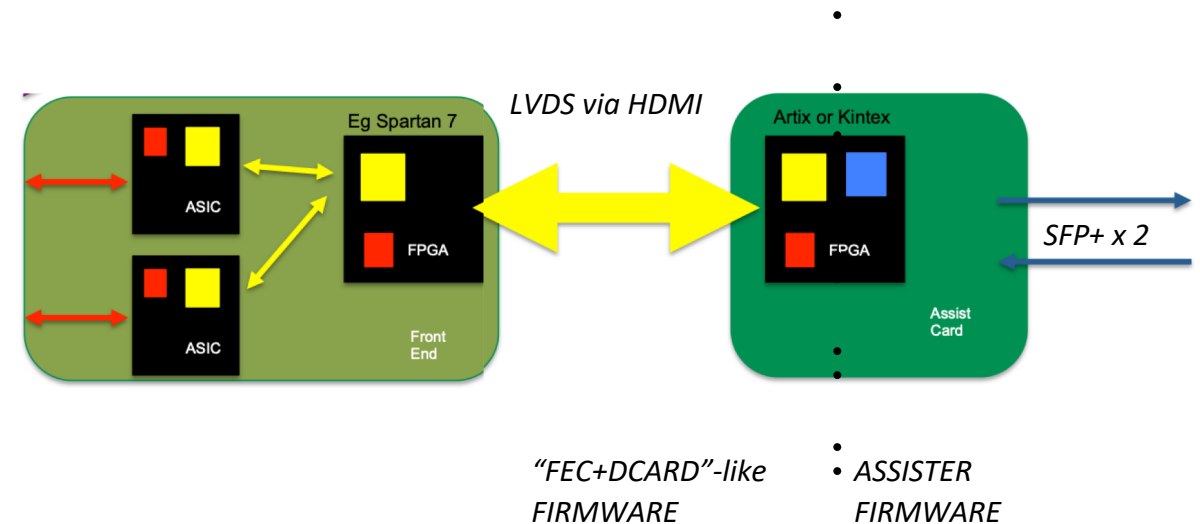
Team for changes

To be discussed, who would like to join
- Hans (RD51)
- Alex (SRS Technologies)
- Steven, Doro (ESS)
- Michael, students (Bonn)
- Chinese student funded by RD51/ESS

ESS VMM3a status

- Order for 56 hybrids out (46 for ESS, 10 for Bonn)
- Hybrids produced from one single wafer
- Outcome will determine yields and quality
- Yield said to be > 80%, but assume 50% for excellent quality
- Lower quality chips can be used for other purposes.
- We should allow for upgrades
- We should allow for spares … these are always in short supply. x%? 50%? 100%? (not decided yet)

ESS VMM3a expected numbers

- NMX: 5120 strips/detector: 240 VMM
- ESTIA: 2 VMM/cassette, 40 cassettes: 80 VMM (or twice for upgrade) = 160 VMM
- FREIA: 2 VMM/cassette, 40 cassettes: 80 VMM
- CSPEC: <13000 grids, 5200 wires. 300 VMM
- TREX: 9000 grids, 8000 wires. 270 VMM
- Lab systems: ca. 100 VMM
- Total: 650? 25 or 50 wafers = 2500 or 5000 chips?
- How do we store extra wafers?
- Future:???: VOR: 16000 grids, 6000 wires. 350 VMM.